Design and Implementation of Millimeter-Wave Power Amplifiers on CMOS

presented by

Byron Neil Wicks
BE(Hons)(Elec)(Melb) BSc(Math)(Melb)

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National Information and Communication Technology Australia
Department of Electrical & Electronic Engineering
The University of Melbourne
Australia

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Dedicated to my family, friends, and teachers,

thank you.

Abstract

This thesis develops the theory and design techniques used to implement Complementary Metal–Oxide–Semiconductor (CMOS) millimetre-wave power amplifiers for use in integrated wireless transceivers allowing low cost, power efficient, high data rate and highly integrated transceivers for communication and radar applications.

Although technology is constantly improving and knowledge is continually advancing the full integration of a power amplifier on die remains a challenge for millimetre wave transceivers. This is due to several causes: the reduction in supply voltage with the scaling of CMOS technology; the limited power gain of the active devices at millimetre-wave frequencies; and the high parasitic losses of the submicron CMOS process.

From the theory developed in this thesis several power amplifiers have been designed, implemented and tested including a millimeter-wave automotive power amplifier, a 75 – 95 GHz wideband power amplifier and a 60-GHz Doherty power amplifier.

Declaration

This is to certify that

(i) This thesis comprises only my original work towards the PhD,

(ii) Due acknowledgement has been made in the text to all other material used,

(iii) This thesis is less than 100,000 words in length, exclusive of tables, maps, bibliographies and appendices.

Byron Neil Wicks, January, 2009

Acknowledgement

This dissertation would not have been possible without the support of a great many people throughout my education, whether explicitly mentioned here or not, and to these people I am indebted.

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Chapter 1
Introduction

1.1 Motivation

The continual advancement of Complementary Metal–Oxide–Semiconductor (CMOS) technology with Moore's Law has seen it consistently replacing more expensive exotic processes at centimeter wavelength frequencies, the portion of the spectrum ranging from 3-GHz to 30-GHz. As the CMOS process scales the transistors implemented in the process have increased in speed and are now able to operate in the millimeter wavelength frequencies, the portion of the spectrum ranging from 30-GHz to 300-GHz, and it is only a matter of time before CMOS becomes a viable alternative for millimeter wave applications.

The ability to implement transceivers in the millimetre wave spectrum with CMOS technology is set to be a boon to RF designers, allowing for new classes of cost efficient devices to be created. The motivation for this thesis originates from two of theses applications; high data rate wireless communication; and vehicular imaging.

1.1.1 High Data Rate Wireless Communication

Consumers are demanding improved connectivity of their devices, including DVD players, portable games, digital cameras, digital audio and visual (A/V) players, personal computers, digital video recorders and high definition televisions (HDTVs), at high data rates, low cost and which connect seamlessly with minimal effort by the user. The millimetre wave spectrum promises to facilitate the realization of this vision, allowing users to connect between devices wirelessly and automatically.

A typical scenario for this technology is a consumer who visits a kiosk in a shopping centre and buys a movie, downloading it wirelessly to his portable A/V device. On returning home the portable A/V device would seamlessly connect to a HDTV, and surround sound system, turn them on automatically and play the rented movie. There would be no wires,

no switches or complex operating procedures required in order to be able to connect all of these devices.

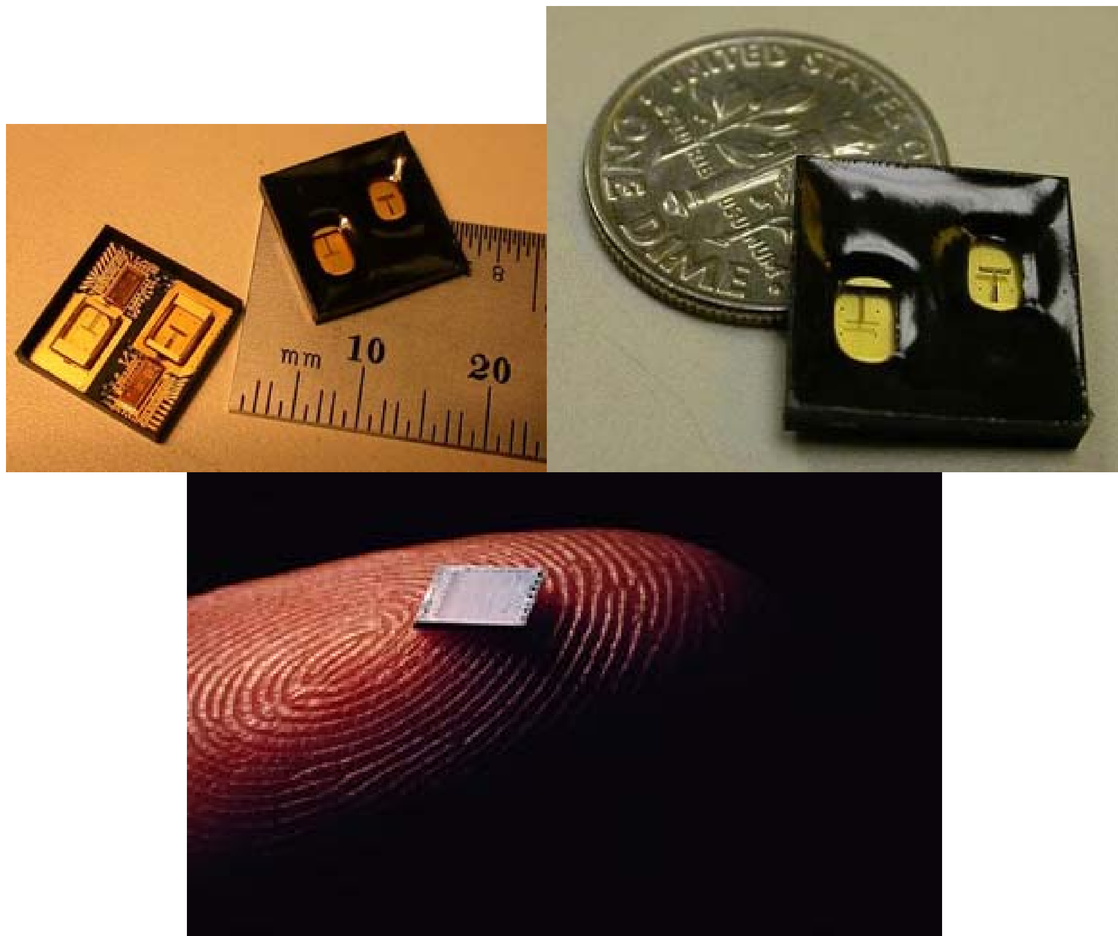

Figure 1 – Possible visions of a 60-GHz transceiver solution [27].

The Federal Communications Commission (FCC) and various international regulatory bodies have released up to 7 GHz of continuous bandwidth in the millimetre wave spectrum around the 60-GHz channel. This spectrum allocation is ideally suited to deliver the high data rate wireless communication services for both device connectivity and wireless personal area networks (WPAN).

1.1.2 Vehicular Radar

Currently, automobile accidents are estimated to account for over 1.2 million fatalities and 50 million injuries annually [82]. There is now political pressure to reduce this carnage and the European Union and several countries are introducing targets to reduce road deaths by

50%. Studies [36] have shown that up to 50% of vehicle collisions could be avoided if vehicles were fitted with radar that assisted, with braking, lane departure and, driving in inclement weather. In order to facilitate the deployment of these technologies regulatory bodies including the FCC have allocated spectra at 24-29 GHz, 46.7-46.9 GHz and 76-78 GHz. Currently automotive radar systems are only equipped on luxury automobiles due to prohibitively high cost. In order for theses systems to be universally deployed across the entire price range of automobiles a low cost solution is urgently required.

1.1.3 Cost Efficiency

Ultimately, for electronic devices, economic consideration decides the technology used in implementation and in order to achieve low costs with a high level of integration CMOS process technology is utilized. The CMOS process is the standard and most cost effective process for building digital circuits. Implementing radio frequency (RF) components of a device on CMOS would allow a high level of integration by combining the digital, mixed signal and RF components of the system to be integrated onto a single substrate allowing for a system-on-chip (SoC) or on a single package allowing for a system-in-a-package (SiaP). Transmitting at millimeter wave frequencies is also advantageous for the form factor of the antenna, as the size of the antenna is inversely proportional to the propagation frequency, and at millimeter wavelengths is in the order of millimeters enabling new packing options including integration of the antenna on the transceiver die, a feat not possible for current centimeter wave transceivers.

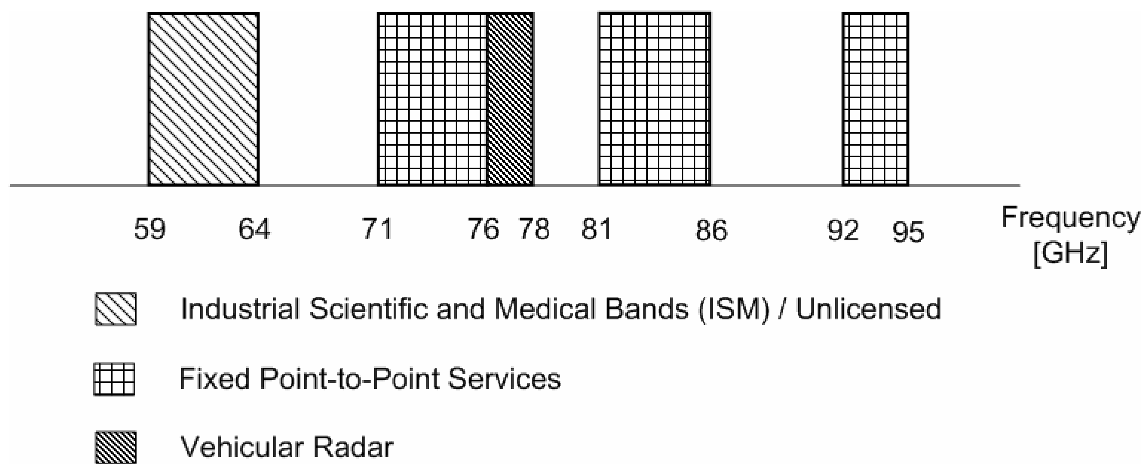

Figure 2 – The United States (FCC) millimetre wave spectrum allocation below 100 GHz.

Unfortunately, the CMOS process is inferior in terms of noise, power handling, substrate and coupling loss and transistor cut-off frequency to the more expensive silicon and type III-V element compounds such as Silicon Germanium (SiGe), Indium Phosphide (InP) and Gallium Arsenide (GaAs), traditionally used to implement millimeter-wave devices. As CMOS was designed primarily for the implementation of digital circuits, it is thus optimized for their implementation. Compared to these more traditional RF processes CMOS has greater process variability, lower carrier mobility and lower device breakdown voltages that pose challenges to the RF designer.

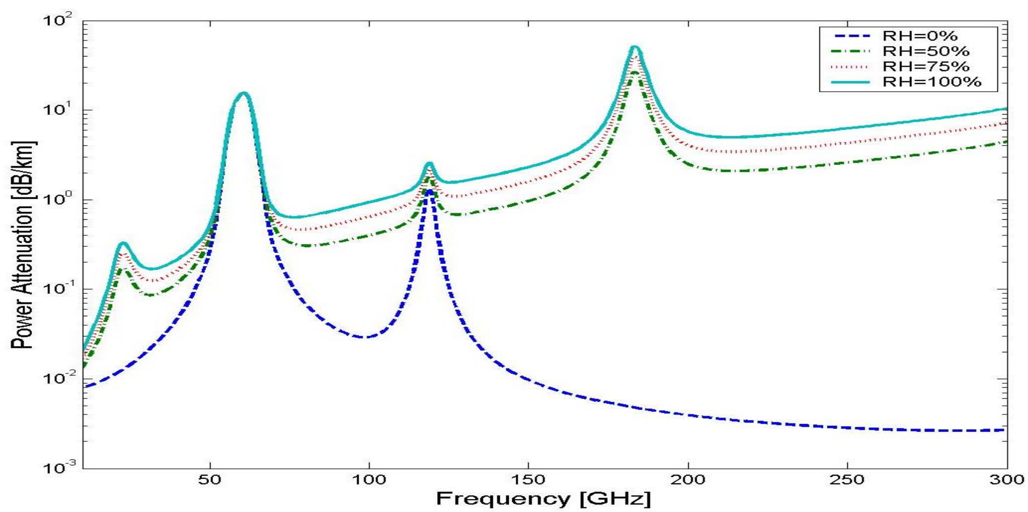

Figure 3 – Power Attenuation by Frequency [79]

1.2 Introduction to the Millimetre Wave Spectrum

Designing a transceiver for operation in the millimeter wave spectrum gives rise to a unique set of advantages and challenges. The millimeter wave channel has high path attenuation, as shown in Figure 3, due to the signal being absorbed by the oxygen molecules in the air and higher attenuation due to walls and floors. In the 60-GHz region of the spectrum this attenuation is severe and limits the range of any device that employs the 60GHz frequency to approximately 20 meters or a single room. This is in contrast to various other wireless local area network (WLAN) technologies, such as IEEE 802.11b/a/g, that utilize lower frequencies and allow for greater range. Far from being a drawback, the large attenuation experienced by devices in the millimeter wave spectrum serves as an advantage for WPANs by increasing security, reducing interference from other wireless sources and allowing more

WPANs to occupy the same building. As a consequence of the attenuation the FCC regulations [25] allow a significantly more powerful signal to be transmitted than with other consumer wireless regulations.

1.3 Objective

The objectives of this thesis focus on the implementation of millimeter wave power amplifiers (PAs) in 130-nm CMOS technology and their integration into millimeter wave transceivers.

A power amplifier is a circuit for increasing the current, voltage and power of a signal by harnessing supplementary power from a power supply and producing a significant output signal with one or more power amplifiers located on the transmit path of a transceiver. Each power amplifier has a unique set of requirements, including frequency, bandwidth, efficiency, linearity and cost, as dictated by the target application.

1.4 Contributions

This thesis develops the theory and design techniques used to implement CMOS millimeter-wave power amplifiers and facilitates the development of low cost, power efficient, high data rate and highly integrated transceivers for WPAN and automotive radar applications. Although process technology is constantly improving and knowledge is continually advancing the full integration of a power amplifier on die remains a challenge for millimeter wave transceivers. This is due to several causes: the reduction in supply voltage with the scaling of CMOS technology; the limited power gain of the active devices at millimetre-wave frequencies; and the high parasitic losses of the submicron CMOS process.

The potential for single chip CMOS millimeter-wave transceivers for automotive radar applications is explored in chapter four. In this chapter a CMOS millimeter-wave integrated circuit (MMIC) power amplifier (PA) is designed and implemented for automotive radar applications with the purpose of system-on-chip integration with the rest of the electronics. To the best of the author's knowledge, this is the first reported fully integrated millimetre wave CMOS power amplifier focussing on automotive applications.

The feasibility of the use of CMOS technology for use in 71 – 76 GHz, 81 – 86 GHz and 92 – 95 GHz point-to-point link bands and the 77-GHz vehicular radar band is explored in chapter five. With a 75 – 95 GHz wideband power amplifier (PA) in 0.13-μm CMOS implemented. To the best of the author's knowledge, this is the highest reported fully integrated millimetre wave CMOS power amplifier.

A Doherty amplifier is discussed in chapter six. To the best of the author's knowledge, this is the first reported fully integrated millimetre wave CMOS power amplifier employing the Doherty technique. It is able to transmit high power with improved average efficiency. The significance of the this work is that, it proves fully integrated CMOS millimetre-wave amplifiers are feasible and will continue to be feasible as the technology scales, it shows the Doherty technique is applicable to millimetre wave amplifiers allowing for improved efficiency especially the active load pull advantages, it demonstrates the high level of linearity required for millimetre wave devices such as high data rate transceivers, that imaging can be achieved with CMOS in the millimetre wave spectrum, and it shows that the issues of limited power generation and amplification at millimeter wave frequencies can be overcome.

The awards arising from this thesis include:

Best student paper for:

B. N. Wicks, C. M. Ta, E. Skafidas, R. J. Evans, and I. Mareels, "A 60-GHz Power Amplifier and Transmit/Receive Switch for Integrated CMOS Wireless Transceivers," The 2008 International Conference on Microwave and Millimeter Wave Technology (ICMMT 2008), Nanjing, P. R. China, April 21-24, 2008.

The publications arising from this thesis:

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B. Wicks, E. Skafidas, R. Evans, "A 60-GHz Fully-Integrated Doherty Power Amplifier Based on 0.13-μm CMOS," IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, June, 2008.

B. N. Wicks, C. M. Ta, E. Skafidas, R. J. Evans, and I. Mareels, "A 60-GHz Power Amplifier and Transmit/Receive Switch for Integrated CMOS Wireless Transceivers," The 2008 International Conference on Microwave and Millimeter Wave Technology (ICMMT 2008), Nanjing, P. R. China, April 21-24, 2008.

B. Wicks, E. Skafidas, I Mareels, R Evans, "A 46.7-46.9-GHz CMOS MMIC Power Amplifier for Automotive Radar Applications," IASTED Antennas, Radar and Wave Propagation (ARP 2008), 30 May–1 June 2007, pp 80 - 84.

B. Wicks, R. J. Evans, and E. Skafidas, "Issues in the Implementation of a 60GHz Power Amplifier based on a 0.13-um CMOS Process for use in a WPAN integrated Transceiver," IEEE Power Amplifier Symposium, Orlando, USA, 21-22 Jan., 2008.

F. Zhang, E. Skafidas, W. Shieh, B. Yang, B. N. Wicks and Z. Liu, "A 60-GHz Double-Balanced Mixer for Direct Up-Conversion Transmitter on 130-nm CMOS," 2008 IEEE Compound Semiconductor IC Symposium (CSICS).

C. M. Ta, B. Wicks, F. Zhang, B. Yang, Y. Mo, K. Wang, Z. Liu, G. Felic, P. Nadagouda, T. Walsh, R. J. Evans, I. Mareels and E. Skafidas, "Issues in the Implementation of a 60GHz Transceiver on CMOS," The 2nd IEEE International Workshop on Radio-Frequency Integration Technology, Singapore, 09-11 Dec., 2007.

B. N. Wicks, C. M. Ta, E. Skafidas, I. Mareels, and R. J. Evans, "A Transmit/Receive Switch and Power Amplifier on 130-nm CMOS for 60-GHz Wireless Transceiver," Melbourne Engineering Research Institute (MERIT), Melbourne, Australia, Nov. 22, 2007.

B. Yang, Y. Mo, K. Wang, Y. Feng, B. Wicks, C. Ta-Minh, F. Zhang, Z. Liu, C. Liu, G. Felic, P. Nadagouda, T. Walsh, and E. Skafidas, "Implementation of a Gigabit Per Second Millimetre Wave Transceiver on CMOS," The 2nd International Conference on Wireless

Broadband and Ultra Wideband Communications, AusWireless 2007, 27-30 Aug., 2007, pp. 71-74.

B. Yang, Y. Mo, B. Wicks, C. Ta-Minh, F. Zhang, Z. Liu, G. Felic, K. Wang, C. Liu, P. Nadagouda, T. Walsh, R.J. Evans and E. Skafidas, "Implementation of a Gigabit per Second Millimeter Wave Transceiver on CMOS," AusWireless Book Chapter 2008.

1.5 Organisation

The thesis consists of six chapters. Chapter two is an overview of the CMOS process that is utilised to implement the transceiver and highlights the strengths and weaknesses of this selection, the models used for passives and actives and their effect on the design of the power amplifiers. Also discussed is the impact future advances CMOS technology will have on the implementation of power amplifiers.

Chapter three presents the fundamentals concepts required for the design and implementation of a power amplifier (PA) in a radio frequency (RF) system, including an overview of the concepts of classes of PA, high frequency amplifier techniques, high power amplifier techniques, matching networks, linearity and efficiency will be discussed.

Chapter four explores the potential for single chip CMOS millimeter-wave transceivers for automotive radar applications. In this chapter a CMOS millimeter-wave integrated circuit (MMIC) power amplifier (PA) is designed for automotive radar applications with the intention of integration with the rest of the electronics is designed and implemented.

In chapter five a 75 – 95 GHz wideband power amplifier (PA) in 0.13-μm CMOS is implemented to explore the feasibility of low-cost CMOS technology for use in 71 – 76 GHz, 81 – 86 GHz and 92 – 95 GHz Industrial, Scientific and Medical (ISM) bands and the 77-GHz vehicular radar band.

In chapter six a sixty-gigahertz (60-GHz) Doherty power amplifier (PA) is been designed and implemented on 0.13 μm RF-CMOS for use in an integrated 60-GHz WPAN transceiver.

Chapter seven concludes the thesis and suggests the potential areas for future work.

Chapter 2
CMOS Technology for Millimetre-Wave Power Amplifiers

2.1 Introduction

Power Amplifiers have been implemented with numerous technologies since their inception. This chapter presents the motivation for the use of Silicon Complementary Metal–Oxide–Semiconductor (CMOS) technology and highlights the strengths and weaknesses of this selection, discusses implementation of the actives and passives and the impact of future technology advances.

2.2 Motivation

When compared to the type III-V semiconductor technology that is traditionally utilised CMOS is found to be inferior in many measures. The performance metrics of the actives implemented in CMOS technology, whether maximum frequency of oscillation, frequency of transition or breakdown voltage, all tend to be significantly lower then the type III-V semiconductors. The high-resistive silicon substrate results in poorer isolation and higher parasitic losses in the passives. The two compelling reasons to consider CMOS technology, manufacturing cost and level of integration both contribute to reducing the overall cost of the device. These issues are discussed further in this section.

2.2.1 Manufacturing Capacity

The ubiquity of CMOS semiconductors today has been facilitated by the continual reduction of chip fabrication costs. This reduction in cost has been achieved by the increase in wafer area, chip yields and quality assurance. *Figure 4* shows the magnitude of the increase in MOS manufacturing capacity (excluding BiCMOS only capacity) that has occurred over the previous 25 years. In this period MOS capacity has increased from almost 500 8-inch equivalent wafers every six months in 1994 to over 2000 8-inch equivalent wafers every 3 months in 2007, an increase of over 800% [77]. Industry groups [40], [76], [77] are predicting these trends to continue for at least the next decade.

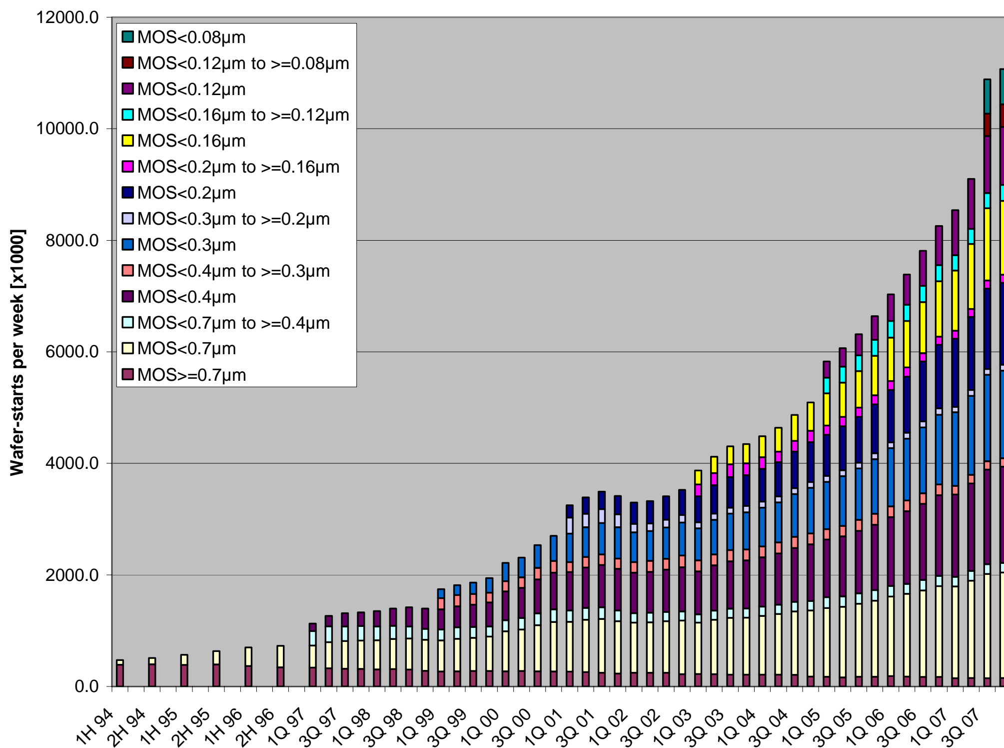

Figure 4 – MOS worldwide manufacturing capacity in 8-inch wafer equivalent areas. [76]

2.2.2 Level of Integration

In the manufacture of electronics higher integration equates to lower cost. The CMOS process is already the standard and most cost effective process for building digital circuits. The ability to implement the front-end radio frequency (RF) components of the transceiver on this process, instead of the more traditional type III-V semiconductor technology, enables a higher level of integration by allowing the combination of the digital, mixed signal and RF components of the system to be integrated onto a single substrate. Operating at millimetre wave frequencies reduces the dimensions of the antenna, to the order of millimeters, enabling new packing options including integration of the antenna on the transceiver die, a feat not possible for current centimeter wave transceivers. Ultimately this integration, and the resultant cost efficiency, would elevate CMOS to the process of choice for millimeter wave devices.

2.3 Active Devices

This section describes the important active device concepts required to implement a millimetre-wave power amplifier including device parameters, inherent characteristics, device models, and figures of merit.

This section will concentrate on NMOS transistors as these are employed as the active building block in the design of the power amplifier. This is due to NMOS devices having higher gain than PMOS devices because of the higher mobility of electrons in silicon. As a consequence lower current densities are required, less power is dissipated and higher output power can be achieved.

2.3.1 Device Parameters

NFET devices electrical performance varies with a number of parameters. It is the design engineer's role to optimise these parameters for each circuit. These parameters, shown in Figure 5, include: transistor width (W), the total effective width of the transistor; transistor finger length (L), the length; of each individual finger; number of finger (n), the total number of fingers in the transistor; transistor finger width (W_F), the individual width of each transistor finger. The effects of these parameters on the performance of the device will be investigated below.

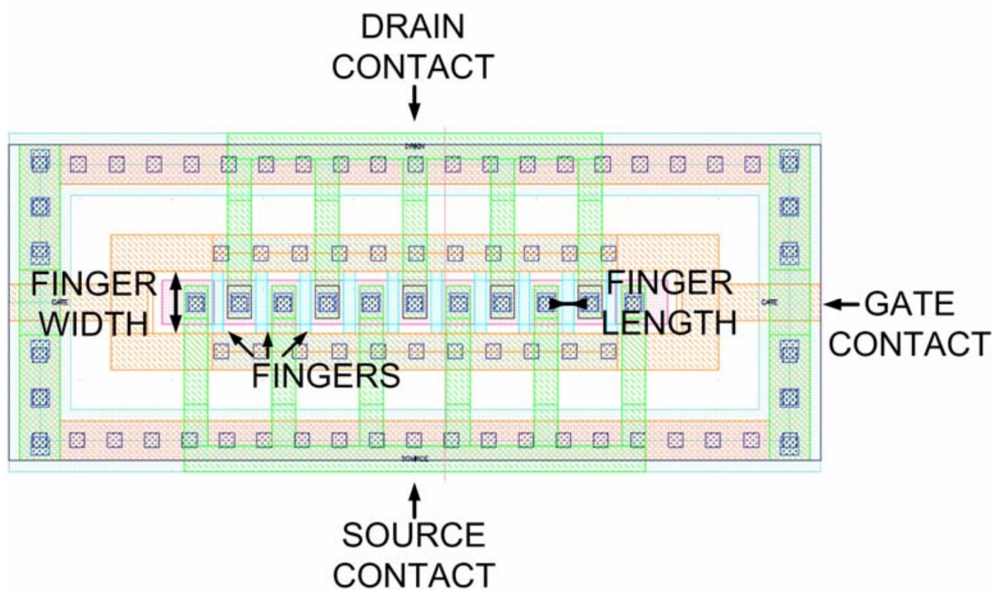

Figure 5 – CAD layout of an NFET transistor with 8 fingers.

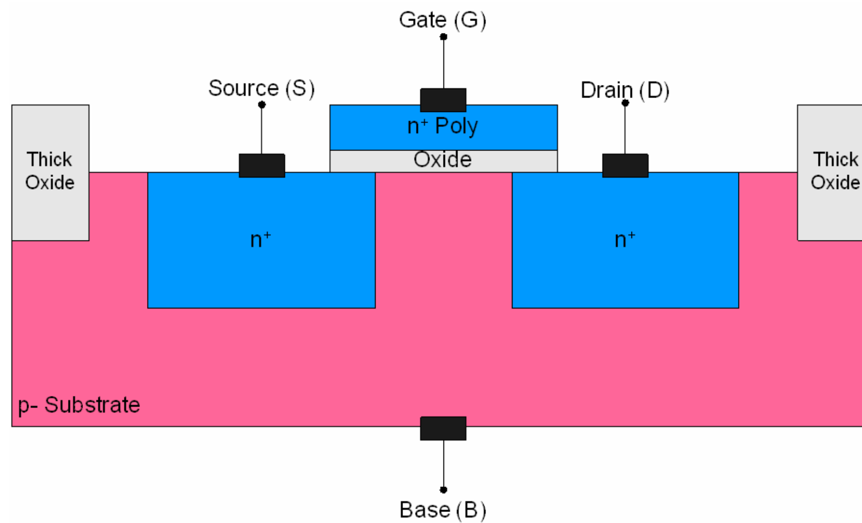

Figure 6 – Structure of an NMOS Device.

2.3.2 Device Structure

Figure *6* shows a simplified cross sectional view of an NMOS device with the four terminals labelled: source, drain, gate and base. There are two n-well regions that are heavily doped by diffusing n-type impurities deep into the p-type substrate. A thick oxide region is grown outside the active areas in order to isolate each transistor. A gate terminal is formed by a heavily doped polysilicon, which is isolated from the substrate by a thin film of silicon dioxide. This creates *pn* junctions with the source and substrate, and the drain and substrate regions. In the area between the source and drain regions a conducting channel is built up under appropriate biasing conditions allowing current to flow. For further explanation of this process consult [50],[62],[65],[72],[92].

2.3.3 Device Model

By taking into account all the parasitic capacitances, inductances and resistances it is possible to produce a physical model depicting the most significant loss mechanisms of CMOS devices as shown in Figure *7*.

Extrapolating a small signal transistor model from the physical model produces a circuit model that can be used for simulations. It should be mentioned that this model infers that the high frequency performance is limited by resistive losses, the most significant being the

gate resistance (R_G), series source/drain resistances (R_S, R_D), nonquasi-static channel resistance (R_{CH}), and resistive substrate network (R_{sb}, R_{bd} and R_{bb}) [23], [24].

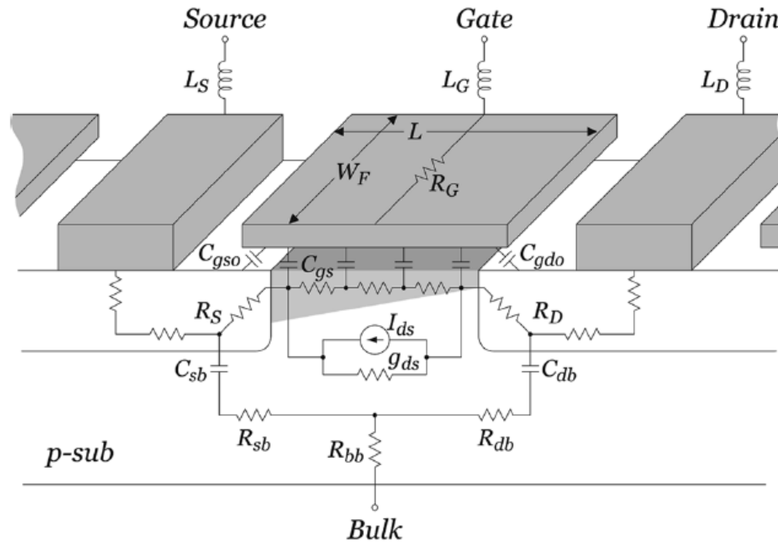

Figure 7 – Simplified Physical Model of a single finger NMOS device. [18]

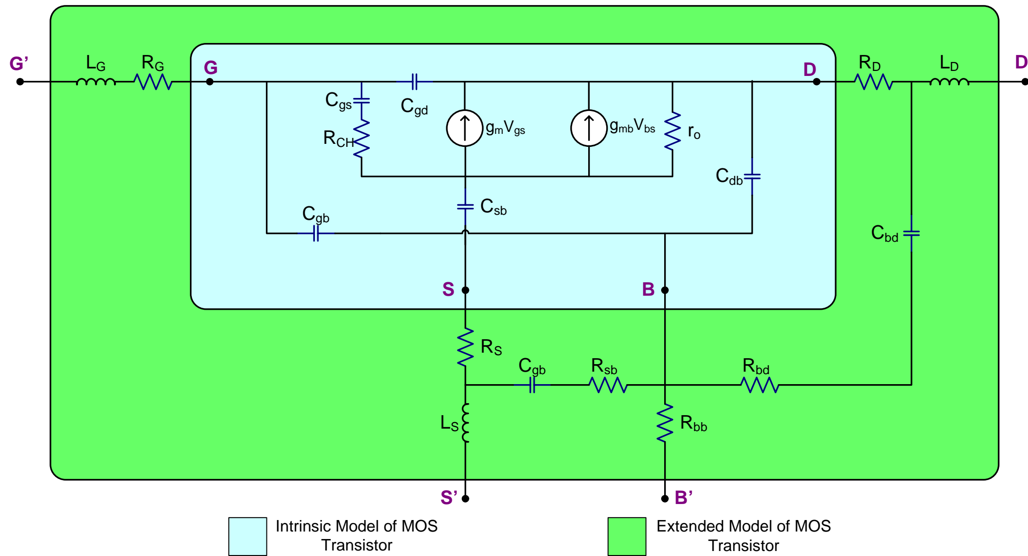

Figure 8 – Intrinsic model and extended model of a MOS device including parasitic elements.

2.3.4 Figures of Merit

The most significant figures of merit (FOM) for the frequency characteristics of active devices are the frequency of transition (f_t), the maximum frequency of oscillation (f_{max}) and

the transistor breakdown voltage. The impact of these FOMs on the millimeter wave components, including the power amplifier, is discussed in this section.

2.3.4.1 Frequency of Transition

f_t is defined as the frequency where the absolute value of the output hybrid parameter referenced from the input port becomes unity and is therefore the maximum frequency where current gain is possible. It is highly dependent on sizing and bias conditions, resistive losses, especially the series gate resistance and layout parasitics. Practically, the measured scatter parameter data is transformed into hybrid parameter data using the transform below. The definitions of the scatter parameters are taken from [31].

$$H_{21} = \frac{-2S_{21}}{(1-S_{11})(1+S_{22})+S_{21}S_{12}}. \qquad \textit{Equation 1}$$

Investigating Frequency of Transition

Circuit models were used to simulate f_t for the various NMOS transistor parameters. Firstly a voltage supply voltage, V_{DD}, needs to be chosen. This was investigated using a voltage sweep from 0V to 1.6V, the maximum drain voltage for the NMOS transistor. Feedback is used to bias the gate, with the circuit displayed in Figure 9.

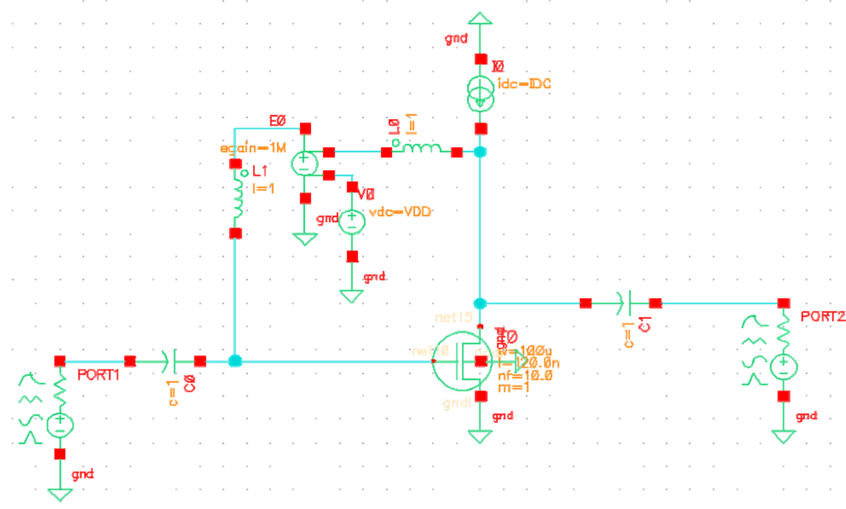

Figure 9 – NFET Characterisation Circuit

A VDD of 1.5-V was chosen as the DC supply voltage as it is 100mV below the maximum voltage allowing a margin for safety. In practice, this safety margin may have to change depending on the variation in the voltage source. The gate bias feedback voltage was 950mV. Multiple current densities, finger sizes and total device widths contained, including all combinations, were simulated and these are contained in Table I.

Variable	**Values**
Total Device Width(m)	20u, 40u, 60u, 80u, 100u,120u
Current Density(A/m)	20, 40, 60, 80, 100, 120, 140, 160,180, 200, 220, 240, 260, 280, 300, 320
Finger Width	0.5u, 1u, 1.5u, 2u, 2.5u, 3u, 3.5u, 4u, 4.5u, 5u, 5.5u, 6u, 6.5u, 7u, 7.5u, 8u

Table I – Swept device parameters for NMOS transistor

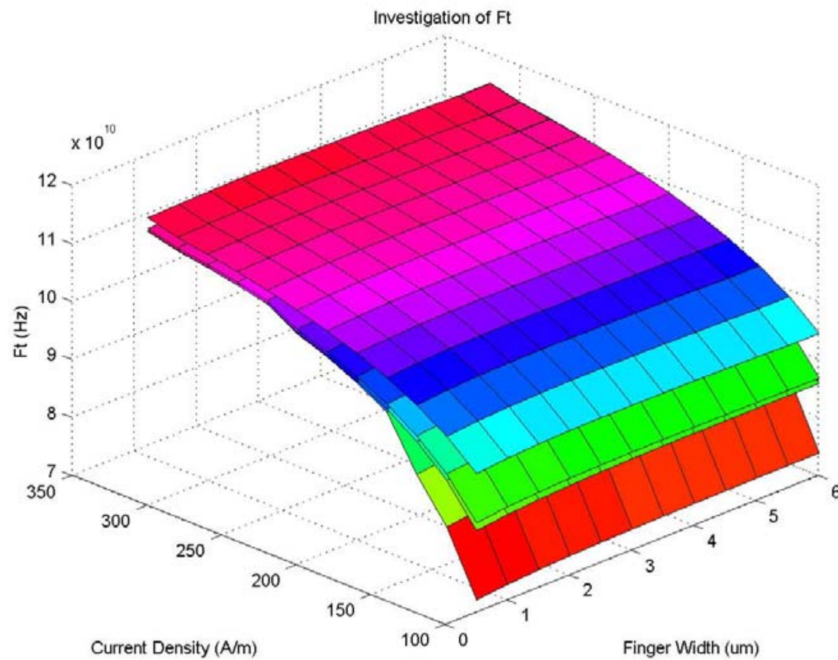

Figure 10 – Simulations of f_t of NMOS Transistor [94]

The output of the NFET characterisation circuit is shown in Figure 10 with the total device width shown as layers from the lower 20μm to the upper 120μm. These results highlight the relationship between f_t, current density, finger width and total width. Clearly visible on the graph is the invariance of f_t to finger width which is consistent with MOSFET theory stated as *Equation 2* and *Equation 3*.

$$I_{D,MAX} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \qquad \textit{Equation 2}$$

$$f_t = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \qquad \textit{Equation 3}$$

It is also evident that f_t is proportional to current density and inversely proportional to total device width and a device with f_t greater than 100 GHz is achievable.

2.3.4.2 Maximum Frequency of Oscillation

The maximum frequency of oscillation (f_{max}) is probably the most important consideration for the design of the power amplifier. Defined as the frequency at which Mason's Unilateral Gain, defined below, is unity [87] it marks the frequency point where the transistor moves from an active device to a passive one. At frequencies higher than f_{max} the transistor becomes a passive device and gain is impossible. The value of f_{max} is highly dependent on sizing and bias conditions, resistive losses and layout parasitics. For narrowband tuned amplifiers where capacitance is resonated out, f_{max} is the better metric for the active device frequency characteristics.

The unilateral gain defined by Mason is the most common design criteria for transistors because the gain is invariant to the common terminal for an active device. To achieve unilateral gain for a two port network S_{11}, S_{21} and S_{22} must be reduced to zero, Equation 4, by lossless feedback and lossless matching.

$$S_u = \begin{bmatrix} 0 & 0 \\ U^{\frac{1}{2}}\angle\theta_u & 0 \end{bmatrix} \qquad \textit{Equation 4}$$

Substitution in the S-parameter matrix allows the calculation of U by Equation 5 [87],

$$U = \frac{\left|\frac{S_{21}}{S_{12}} - 1\right|^2}{2\left[k\left|\frac{S_{21}}{S_{12}}\right| - \mathrm{Re}\left[\frac{S_{21}}{S_{12}}\right]\right]} \qquad \textit{Equation 5}$$

Solving these equations for MOSFETs the $f_{\max}$ may be expressed relative to the devices inherent properties,

$$f_{\max} = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \sqrt{\frac{1}{g_{ds}\left(R_G + R_S\right) + \frac{g_m R_G C_{GD}}{(C_{gs} + C_{gd})}}}. \qquad \textit{Equation 6}$$

Investigating Maximum Frequency of Oscillation

$f_{\max}$ can be shown theoretically to be independent of the number of fingers of a transistor. Therefore to optimize a multi-finger transistor it is sufficient to optimize the layout of a single finger transistor to reduce the resistive losses the most significant being gate, source and drain resistances.

By using multiple narrow finger widths the gate resistance becomes negligible with the disadvantage of an increased gate capacitance which can be addressed with matching networks. The advantage of a negligible gate resistance is that $f_{\max}$ will be primarily determined be the source and gate resistances.

The same NFET characterisation circuit, shown in Figure 9, with the same biasing conditions and a swept of the same parameters, shown in Table I was used to investigate $f_{\max}$.

Figure 11 shows the results of the simulations for finger width, number of fingers and total width. From these simulations the following can be concluded:

f_{MAX} increases with the total width of the transistor. This is visible as the equal total device width planes increase with the total width of the transistor, from lowest through to highest in order, 30um, 60um, 90um and then 120um. It is clear that increasing the total width of the transistor from 90um to 120u has limited affect in the f_{MAX} of the transistor.

Decreasing the finger size of the transistor does not exclusively increase f_{MAX}. Instead, at finger sizes less than 2.5um reducing the finger size may reduce f_{MAX}, this is clearly the case for a transistor with total width of 60um.

The transistor device benefits from being biased into strong inversion for optimal operation in millimeter-wave frequencies. For this reason a current density greater than 250 A/m is preferred.

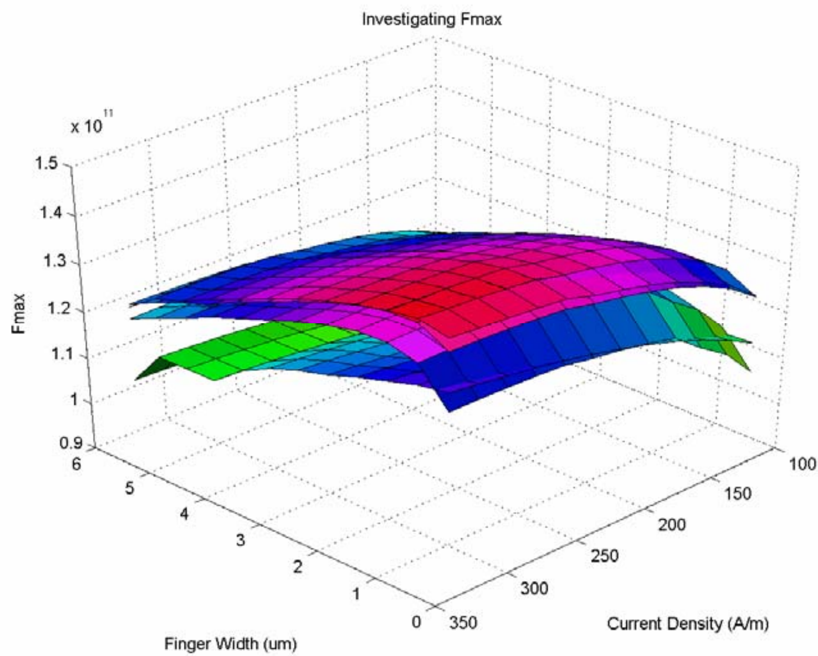

Figure 11 – Simulations of f_{max} of NMOS Transistor

2.3.4.3 Breakdown Voltage

The third critical figure of merit affecting power amplifiers performance is breakdown voltage. Breakdown voltage directly influences the magnitude of the voltage swing of the device. The time-dependent dielectric breakdown (TDDB) is the most significant limitation on the voltage range of a MOSFET. The TDDB is a function of hot carrier effects, gate oxide breakdown, snapback breakdown and junction breakdown [41]. This process damages the silicon-oxide interface and reduces the threshold voltage of the device over time.

The recommended device limitations are set by the foundry and based on DC or transient reliability test at the minimum channel lengths. It has been stipulated [62] that further investigation may relax the conservative limits on the supply voltage but this is outside the scope of this thesis. For further information the reader is directed to [62], [65], [87].

2.4 Passives

Detailed analysis of a process would not be complete without considering the implementation of passives on a process, especially as the area of passive components on a RF transceiver is far larger then the actives. This section will discuss the information of millimetre wave passives on CMOS.

2.4.1 Resistors

Resistors are used sparingly in millimetre-wave CMOS design. Two examples are biasing circuits employing resistors to provide isolation, and amplifiers commonly utilising resistors to stabilize the circuit. Resistors available for use in the CMOS process include doped and undoped polysilicon resistors, diffused substrate resistors, and BEOL precision thin film resistors. The latter is only available with the purchase of an extra mask and thus is generally undesirable for use.

2.4.2 Inductors

Millimetre wave inductors on CMOS are utilised extensively to tune out parasitic capacitances exhibited by active devices. At millimetre waves inductances are predominantly realised by short sections of transmission line. Distributed transmission line element inductors exhibit reduced process variation and improved isolation when compared to their lumped equivalents. With well characterised transmission lines simply variation of the length will produce a required inductance (within limits). In reality the length, width and separation of the signal and return paths needs to be investigated to ensure correct operation.

The two commonly implemented transmission lines are shown below. Figure 12 shows the cross section of a microstrip transmission line typically implemented using one of the top layers as the signal line and one of the bottom most layers as the return path. The bottom ground plane acts as a shield reducing the signal substrate loss. Figure 13 shows the cross section of a coplanar waveguide typically implemented using one of the top layers with small conduction loss and the ability to implement wider metal paths. The ability to finely control the spacing of the return paths facilitates ease of tuning of the desired inductance and resistance properties.

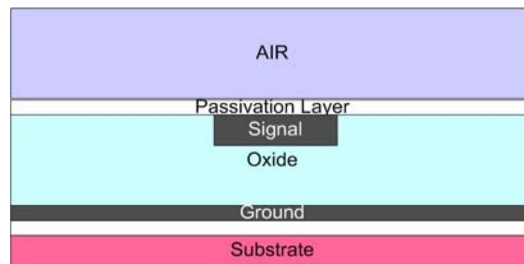

Figure 12 – Cross section of a microstrip transmission line.

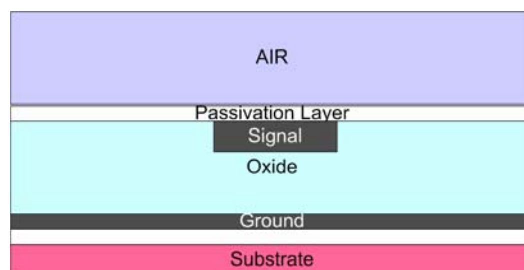

Figure 13 – Cross section of a coplanar waveguide transmission line.

2.4.3 Capacitors

In millimetre wave design capacitors are used as DC blocking, AC coupling and (rarely) for impedance matching networks. The CMOS process facilitates a number of lumped element capacitors, the MOM (metal-oxide-metal) and the MIM (metal-insulator-metal), the latter requiring an extra mask set to produce, and also the realisation of a capacitor with distributed element transmission lines similar to those discussed for inductors.

2.5 CMOS Future Trends

Two strong trends are predicted [40] that will effect the implementation of millimetre wave CMOS devices in the future. Figure 14 shows the increase in the performance of CMOS f_{max} and f_t that is predicted in the coming decade. This trend allows for more gain and faster switch of active device, facilitating reduced difficulty in achieving gain at millimetre wave frequencies. Figure 15 shows the decrease in supply voltage that is predicted in the coming decade. This trend increases the difficulty in designing circuits with sufficient power handling capabilities and will predictably lead creative solutions that utilise greater currents and less voltage.

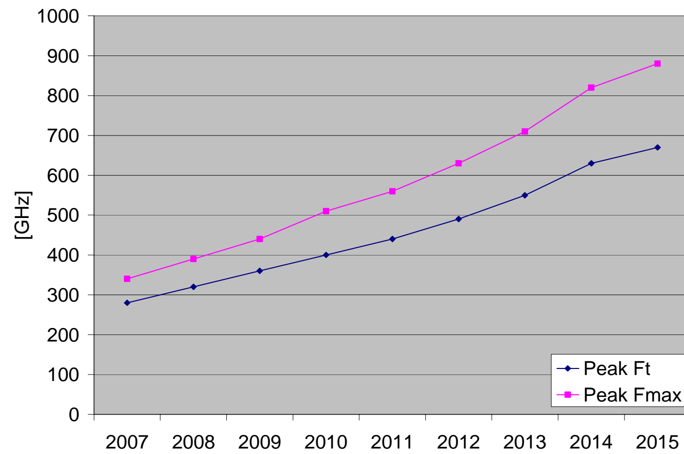

Figure 14 – Industry [40] estimates of future f_{max} and f_t transistor trends.

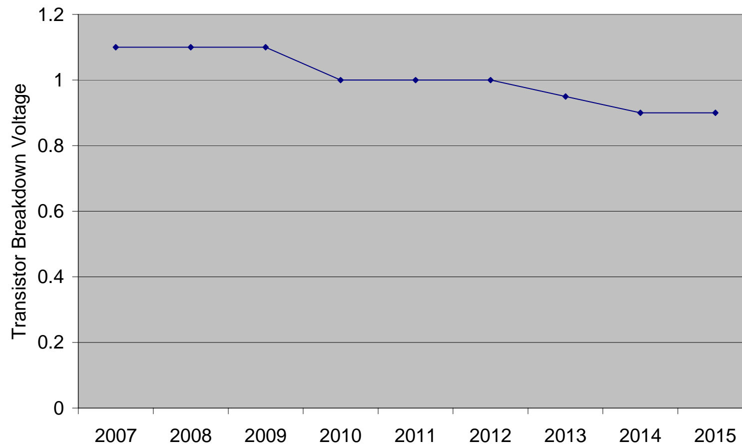

Figure 15 – Industry [40] estimates of future transistor breakdown voltage trends.

2.6 Conclusion

This chapter has presented the motivation for the use of Silicon Complementary Metal–Oxide–Semiconductor (CMOS) technology and highlighted the strengths and weaknesses of this selection, discussed implementation of the actives and passives and the impact of future technology advances.

Chapter 3
Fundamentals of Radio Frequency Power Amplifier Design

3.1 Introduction

The role of the power amplifier circuit is to generate significant output power at RF frequencies by converting DC input power. Each transmitter contains at least one power amplifier but they are also found on systems as diverse as signal generators, frequency converters, microwave heaters, and DC-to-DC converters amongst others. This chapter introduces some fundamental concepts required for the design and implementation of a power amplifier in a radio frequency (RF) system, including an overview of the concepts of classes of PA, high frequency amplifier techniques, high power amplifier techniques, matching networks, linearity and efficiency will be discussed.

3.2 Transceiver Architecture

Figure 16 shows a typical homodyne front-end architecture for a RF transmitter. The PA is located in the transmit path after the mixers and before the band-pass filter (BPF) and the RF Output, typically an antenna. Variable gain amplifiers (VGA) are used to provide sufficient input signal power to the mixers.

For completeness Figure 17 shows a typical homodyne receiver architecture. The RF input, typically from an antenna, is passed through a Low Noise Amplifier (LNA), divider, mixer and output to base-band.

Figure 18 shows a micrograph of a single die 60-GHz CMOS homodyne transceiver with architecture described in Figure 16 and Figure 17. Additionally included on-die is the phase lock loop (PLL), serial peripheral interface (SPI), and test structures. The SPI consists of an adaptive biasing circuit which includes a digital control and timing interface (DCTI), DACs and ADCs. The adaptive biasing circuit is utilised to neutralise the degradation in performance that occurs in the transceiver due to the fabrication process variations

(parasitics), temperature variations and voltage variations. The PLL circuit is utilized to produce an operating frequency to match a stable reference signal.

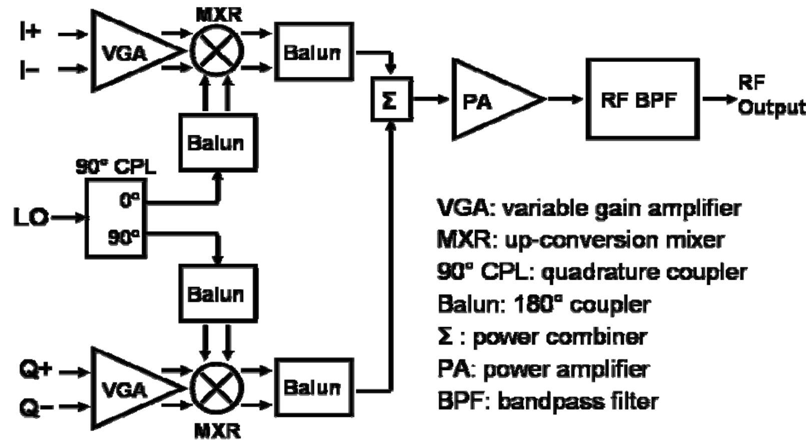

Figure 16 – Typical Homodyne Transmitter Architecture [53]

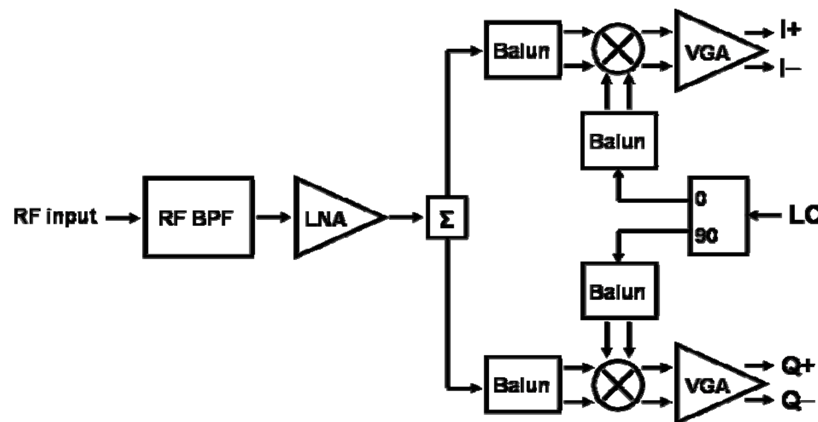

Figure 17 – Typical Homodyne Receiver Architecture [53]

3.3 Classes of Power Amplifiers

RF power amplifiers are generally divided into classes. The most common of these classes are denoted A, B, C, D, E, and F with additional classes occasionally specified in literature. The class-A power amplifier is a version of the standard small-signal linear amplifier with increased power handling capability, whilst the other classes employ various wave-shaping, non-linear and switching techniques to achieve the required performance. Originally, class specified the bias conditions but these classes grew to include variations from the "classic"

theory of the class-A, AB, B, C amplifiers. This section will discuss the topologies, biasing, power handling capability, linearity and efficiency of the power amplifier classes.

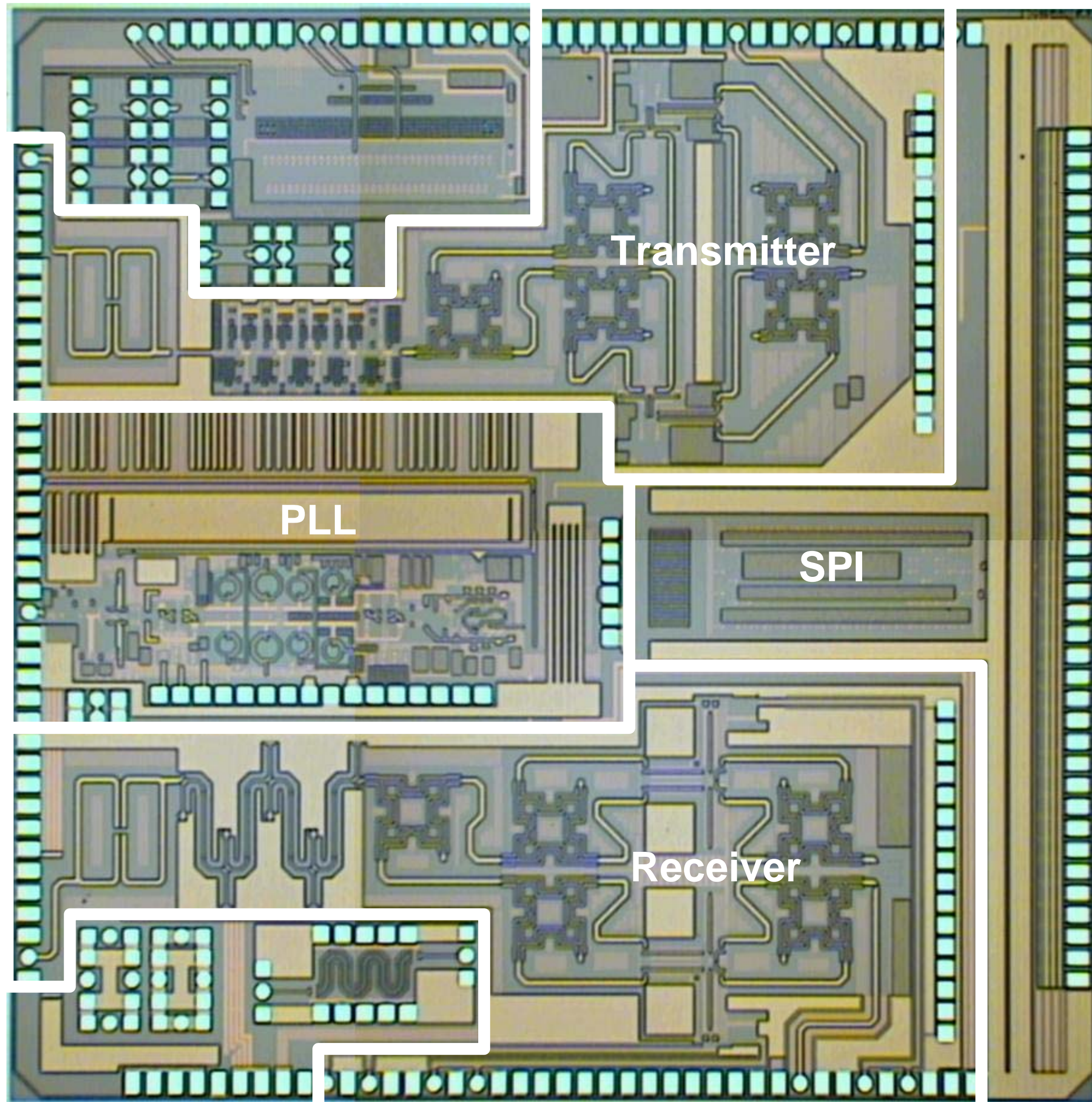

Figure 18 – Single Chip 60GHz CMOS Transceiver Micrograph

3.3.1 Class-A, AB, B, and C Power Amplifiers

These four amplifiers are architecturally similar and are distinguished most significantly by biasing conditions; all four will be discussed using the architecture shown in Figure 19. In this generic model, the output V_{OUT} is assumed to be connected to the load into which the power is to be delivered, usually a transmit / receive switch, band pass filter or an antenna. The parasitic capacitance of the transistor, C_{PAR} and the output impedance, Z_{OUT}, with

superficial input from the L_{CHOKE} and $C_{DC-BLOCK}$, form an LC tank ideally resonating at the centre frequency of the channel. L_{CHOKE} is a large inductor and serves to supply DC power to the MOSFET drain and the C_{CHOKE} is a large capacitor and serves as a DC block / AC signal pass.

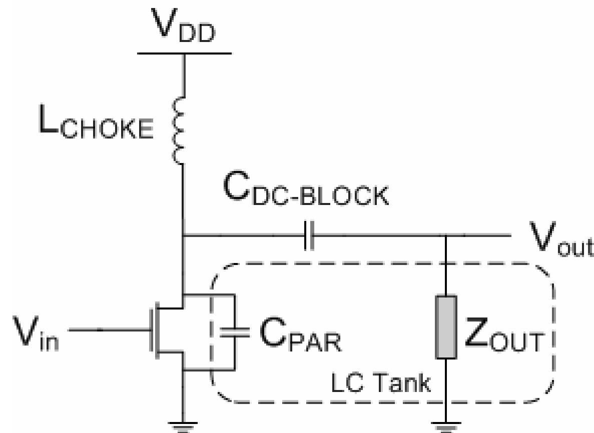

Figure 19 – Genetic Power Amplifier Architecture

In class-A the power amplifier is a scaled-up small-signal amplifier. It is the most linear of the power amplifiers as the output signal is ideally an amplified version of the input signal with minimal distortion, however this results in low efficiency. The quiescent current is large allowing operation wholly in the pentode (saturation) region with the active device operating as a current source controlled by the input current. A significant difference between the class-A power amplifier and the small signal amplifier is that the signal currents in the power amplifier are a substantial proportion of the biasing levels, with the LC tank supplying the reservoir of power that alleviates the potential for distortion under normal operating conditions. Therefore Class-A power amplifiers are typically used in applications requiring high gain, linearity, and high frequency operation, such as those described in this thesis.

In an effort to improve the efficiency of the class-A power amplifier at the expense of linearity, the gate bias of the amplifier is reduced causing the input RF signal to “turn on” and “turn off” the active device, therefore reducing the amplifier conduction duty cycle, the percentage of the waveform of the input signal that is amplified, and reducing power. Biasing the amplifier with low quiescent current allows the radio frequency alternating current signal to turn on the active device. Between 100% and 50% conduction duty cycle

the power amplifier is biased in class-AB. At 50% conduction duty cycle the power amplifier is biased at the threshold of conduction so ideally the quiescent current is zero and this is defined as class-B operation and at a conduction duty cycle less than 50% it is biased in class-C.

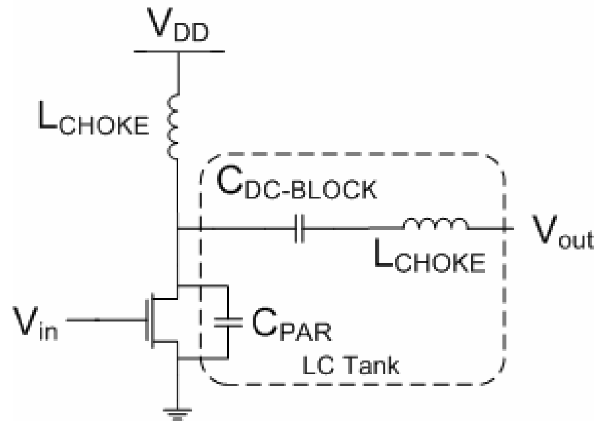

Figure 20 – Class D Architecture

3.3.2 Class-D Power Amplifiers

The class-D power amplifier shown in Figure 20, employs the active device as a switch instead of a controlled current source. As a switch ideally dissipates no power, as there is no current passing through it when it is in the off state or no voltage across it when it is in the on state, therefore if it switches between these states in zero time the efficiency ideally approaches 100%. The class-D amplifier cannot normally provide linear modulation and as a switch-mode amplifier operates well below f_t. This amplifier suffers from losses due to saturation, finite transistor switching speed causing the active device to remain operating in the active regions while conducting current, and the charging and discharging of the drain capacitance.

3.3.3 Class-E Power Amplifiers

The class-E power amplifier shown in Figure 21 is another class of amplifier employing switched-mode operation. A high-order network is used to absorb the parasitics of the active devices, eliminating the losses associated with charging of the drain capacitances (as occur in class-D), with enough degrees of freedom to allow the shaping of the voltage so that it is possible to have zero drain current and zero voltage at turn on and thus an

efficiency approaching 100%. The drawbacks are higher complexity and a reduced power handling capacity.

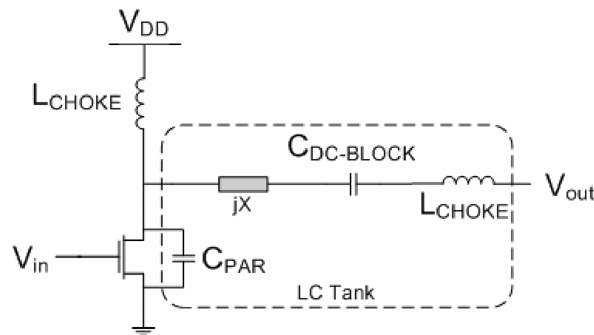

Figure 21 – Class E Architecture

3.3.4 Class-F and Inverse Class-F Power Amplifiers

The class-F and inverse class-F power amplifier is another amplifier class employing switch-mode operation. The concept of exploring harmonic resonating terminations to shape the current and voltage waveforms used in class-E amplifiers is extended by the use of extra resonating networks and as a result the amplifier has increased efficiency. In a class-F amplifier the voltage waveform consists of one or multiple odd harmonics, and the current waveform consists of one or multiple even harmonics. Conversely, the inverse class-F amplifier current waveform consists of one or multiple odd harmonics, and the voltage waveform consists of one or multiple even harmonics.

3.3.5 Class-G, Class-H Power Amplifiers

Class-G and class-H amplifiers are a more efficient version of the classic, transconductance power amplifiers. The class-G amplifier uses discrete "rail switching" to decrease power consumption and thus increase efficiency. The amplifier employs a number of power rails to increase the supply as required.

The class-H amplifier extends the class-G amplifiers discrete "rail switching" to a continuous versions supplying sufficient voltage for optimum efficiency at all input voltage levels, otherwise known as envelope tracking.

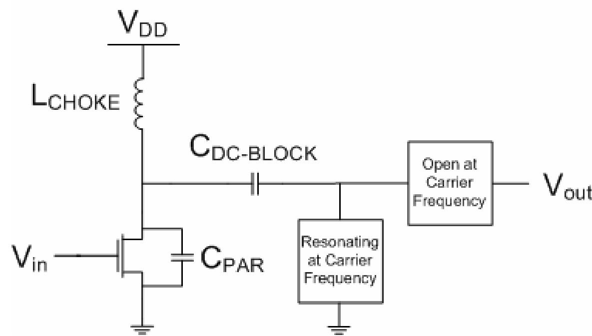

Figure 22 – Class F Architecture

3.3.6 Hybrid Class Power Amplifier

Several hybrid power amplifier classes have been proposed to deal with some of the disadvantages of the single class power amplifiers. These hybrid class amplifiers include; the class-BD power amplifier with a linear transfer characteristic, higher efficiency and with the same peak output power as a class-B [66]; the class-EF power amplifier incorporates the transistor parasitics but also shapes the output harmonics to achieve the desired current and voltage output waveforms [43].

3.4 High Frequency Amplifier Techniques

Designing amplifiers for operation at high-frequencies, operating the devise close to their inherent limitations, requires more advanced considerations a designing amplifiers at lower frequencies. Device parasitics are more pronounced at high frequencies, gain is harder to achieve, and the difficulty in designing high quality passives are a few of the challenges that impose serious constraints on circuit performance.

Several techniques used to enable high frequency amplifier design are discussed below.

3.4.1 Shunt Peaked Amplifiers

For a purely resistively loaded common-source amplifier the gain is proportional to $g_m R_L$. When a capacitance load is added the gain will reduce with frequency as the impedance reduces, Equation 7. This capacitive load may be the input capacitance of another transistor amplifier stage which is highly useful if cascading of amplifier stages is required.

$$Z(s) = R \parallel \frac{1}{sC} = \frac{R}{sRC+1} \qquad \textit{Equation 7}$$

Adding an inductive load, a zero in series, causes the impedance to increases with frequency which offsets the decreasing impedance of the capacitance. This will produce an impendence that varies less over a broader frequency range then the original network.

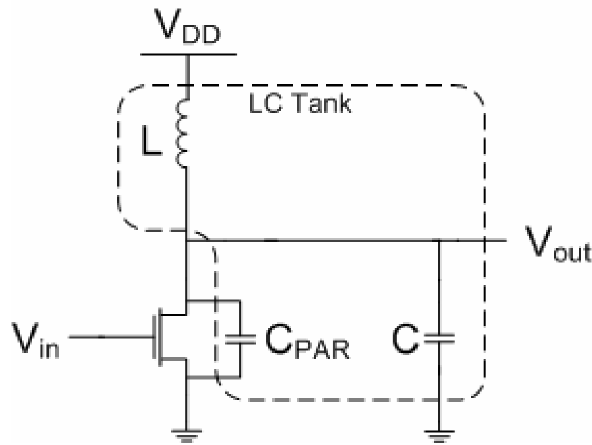

Figure 23 – Shunt Peaked Amplifier

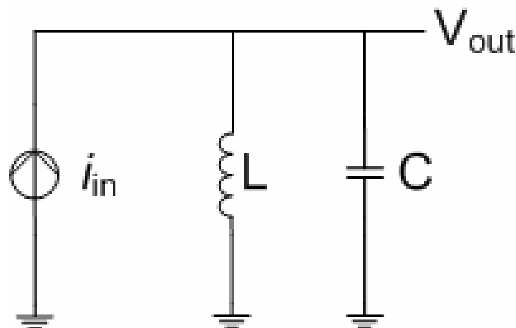

Figure 24 – Equivalent Model of the Shunt Peaked Amplifier

From Figure 24 the impedance of the RLC network may be written as

$$Z(s) = (sL + R) \,||\, \frac{1}{sC} = \frac{R[s(\frac{L}{R}) + 1]}{s^2 LC + sRC + 1} \qquad \textit{Equation 8}$$

In contrast with the RC case there now is a quadratic term in the denominator that now aids in increasing the bandwidth. This can increase the -3 dB bandwidth by a maximum of the square root of 2 [50].

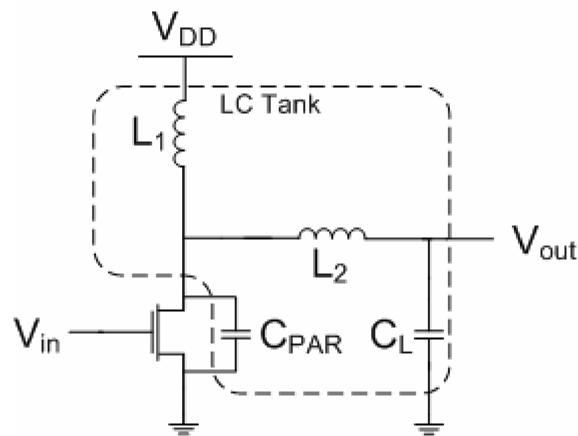

Figure 25 – Shunt and series peaked amplifier

3.4.2 Shunt and Series Peaked Amplifier

Shunt peaking may be augmented by additionally separating the load capacitance from the output capacitance of the device. Figure 25 shows the result if an inductor is used to perform the separation, this is a combination of shunt and series peaking.

This leads to only a slightly larger bandwidth then the shunt case. Shunt Peaked amplification can lead to shunt and double series peaking, then to T-Coil bandwidth enhancement and then eventually to negative feedback [31], [50].

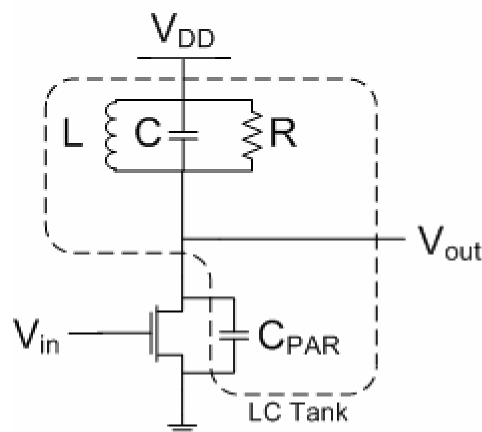

Figure 26 – Amplifier with Tuned Load

3.4.3 Tuned Amplifiers

Tuned amplifiers are used to extensively in communications circuits both to provide a high level of amplification within the channel and to filter unwanted frequencies outside the channel. Furthermore the power required to obtain the high gain can be considerably less than for broadband implementation.

Using the model for the amplifier with tuned load depicted in Figure 26, the input and output admittances can be calculated. To do this the value of V_{gs} will be fixed to make the mathematics easier, as it controls the value of the current source.

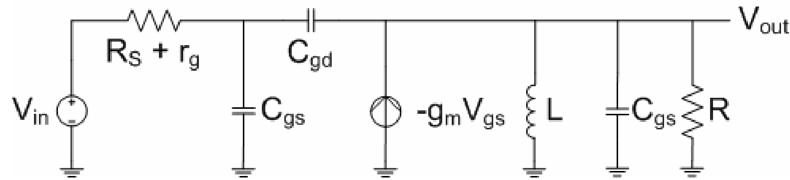

Figure 27 – Amplifier with Tuned Load Model

From the amplifier with tuned load model the capacitance of the output port of the transistor is given by, essentially Figure 27 with the RLC tank removed.

$$C_{eq} = C_{gd}[1 + g_m(R_S + r_g)] \qquad \text{Equation 9}$$

This is essentially the Miller Effect viewed from the output port, and will shift the resonant frequency downward. This shift can be compensated by increasing the inductance of the RLC tank.

Considering the input admittance next, ignoring input and gate-source impedances the following equation is produced. The approximation follows if $y_L >> y_{RLC}$.

$$\begin{aligned} y_{in} &= \frac{y_{Cgd}\, y_{RLC}}{y_{Cgd} + y_{RLC}} + \frac{g_m y_{Cgd}}{y_{Cgd} + y_{RLC}} \\ &\approx y_{Cgd} + \frac{g_m y_{Cgd}}{y_{RLC}} \end{aligned} \qquad \text{Equation 10}$$

This equation is problematic as y_{in} can now have a negative real part due to C_{gd}. This would be ideal if oscillation was the goal of the circuit but unfortunately it is not. Turning the input, as is required for the PA, will only increase the circuits tendency to oscillate and not be a power amplifier. More on oscillators can be found in [31],[50] but will not be covered here as it is outside the scope of this report, though tuning still has an important role to play in the design of the PA and will be further discussed below. But first we have to do something about C_{gd}.

3.4.4 Neutralization and Unilateralization

The magnitude of C_{gd} is a problem because the input port is coupled with the output port essentially allowing feedback between them. Removing or reducing this coupling via unilateralization reduces the potential for instability, detuning and neutralization of the Miller effect. This can be achieved in various ways; one example is the use of a common-gate stage creating the Cascode Amplifier, Figure 28. In this configuration the input signal drives the gate of the common-source device, whilst the gate of the common-gate device is grounded exhibiting a low input resistance to the common-source device and reducing the voltage gain, and thus Miller Effect of the common-source device. The high resistance of the output of the common-gate device produces voltage gain.

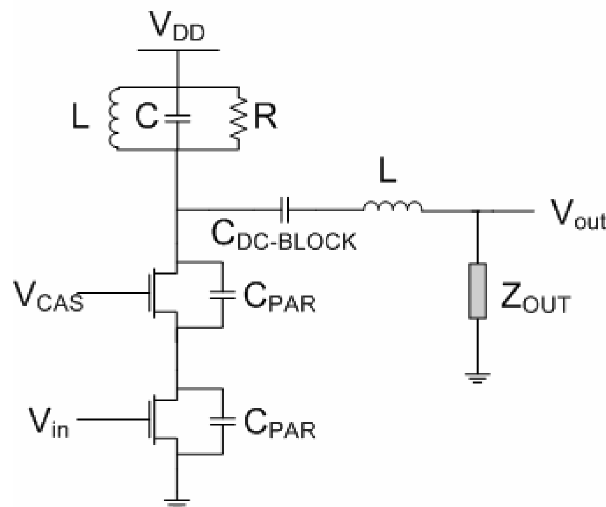

Figure 28 – Cascode Amplifier with Tuned Load

3.4.5 Cascading

When insufficient unilateral power gain is available cascading of stages is required. This is most often achieved with an input stage, driver stage and output stage with input, output and interstage matching networks.

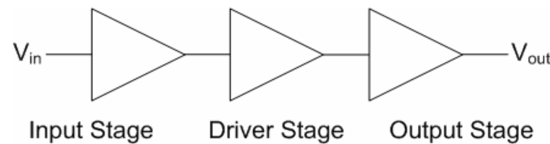

Figure 29 – Cascade Radio Architecture

Cascading stages will have a negative impact on bandwidth but allows for increased gain is impossible without cascading. This shrinkage is inversely proportional to the inverse square root of the number of stages.

3.5 High Power Amplifier Techniques

The power amplifier designer is always struggling for methods to supply more output power. This is especially evident when using the CMOS process, as it was not designed for power handling capability. Relying on the Power Law, P = *vi*, it is obvious that to increase the output power either the output voltage, output current or both need to be increased. This section will discuss the techniques used in literature to increase the output voltage and the output current.

3.5.1 Voltage Combining

Combining voltage by placing transistors in series allows several devices to contribute to the output voltage and thus increase the output power. Combining voltage requires careful consideration of device breakdown voltages. Exceeding the device breakdown voltages will result in damage to the transistor and a reduction in performance. This section will introduce the theory behind voltage combining with the design of several voltage combiner topologies discussed.

3.5.1.1 Cascode Topology

The cascode topology, Figure 28, covered previously in section 3.4.4 as a method for increasing neutralization and unilateralization of high frequency amplifiers, especially

helping to reduce the unwanted capacitive feedback of the Miller Effect. The cascode is a two-stage amplifier consists of a common-source device with a common-gate device connected to the drain. The gate of the common-source device is driven by the input signal, with the gate of the common-gate obviously AC grounded.

The cascode topology aids the power amplifier designer by allowing the circuit to sustain higher voltage before breakdown then would be possible with only one stage. Care with biasing is required to evenly share the stress caused by the higher voltage between both devices, and thus not allowing one of the devices to breakdown.

Research into several techniques to overcome the device stress of the cascode under high voltages has been presented. Research into using think-oxide devices for the common-gate device of the cascode, usually the more stressed device, to allow higher device output swing is presented in [100]. This work is not applicable for high frequency operation as thick oxide devices have a poor high frequency response and are therefore not a suitable solution for a designer looking for high frequency operation. Research into a self biased cascode topology has been presented in [80]. In this work the common-gate DC bias is dynamically biased at the same level as the output of the power amplifier. This theoretically relaxes the restriction due to the hot-carrier degradation and allows an increased voltage supply without shortening of the devices lifespan.

The disadvantages of the cascode topology include potential instability especially if an AC signal is present at the gate of the common-gate device, and possible power loss in the common-gate device. Both these issues can be overcome but require careful attention by the designer.

3.5.1.2 Totem-Pole Topology

The totem-pole amplifier, shown in Figure 30, extends the concept of the cascode amplifier by summing voltages over multiple devices in series. It also uses a self-biasing feedback ladder network to bias the common-gate devices, a similar to but extended version of the self-biasing feedback of [80]. By allowing the voltage to be distributed over multiple devices, no single device needs to exceed breakdown, and the sum of all the devices will

exceed the breakdown of a single device allowing a higher supply voltage and a higher voltage swing at the output.

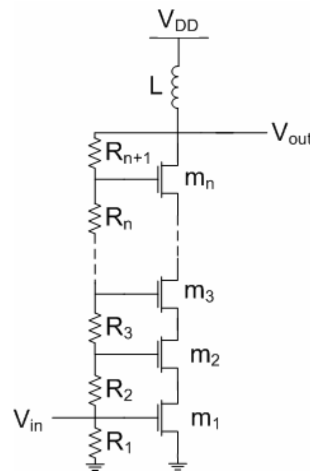

Figure 30 – Totem-Pole Architecture

For high frequency RF operation the propagation delay in the bias network severely hampers the usefulness of the totem-pole amplifier. The bias levels of the gate of the common-gate devices will not be synchronised, causing phase and amplitude distortion.

3.5.1.3 Stacked Transistor Amplifier Topology

The stacked transistor amplifier, shown in Figure 31 is a modified totem-pole amplifier that addresses the significant drawback of the frequency range of the amplifier. Recalling, that the poor frequency response of the totem-pole was caused by the resistive biasing network, [57] proposes replacing this network with transformer coupling.

3.5.2 Current Combining

Combining current by placing transistors in parallel allows several devices to contribute to the output current and thus increase the output power. Combining power requires careful consideration of reflections and distortion from poor matching. To successfully match networks and overcome this problem power combiners are required, either in a distributed or lumped component approach. This section will introduce the theory behind current combining with the design of current combiners discussed including transformer based and transmission-line based combiners.

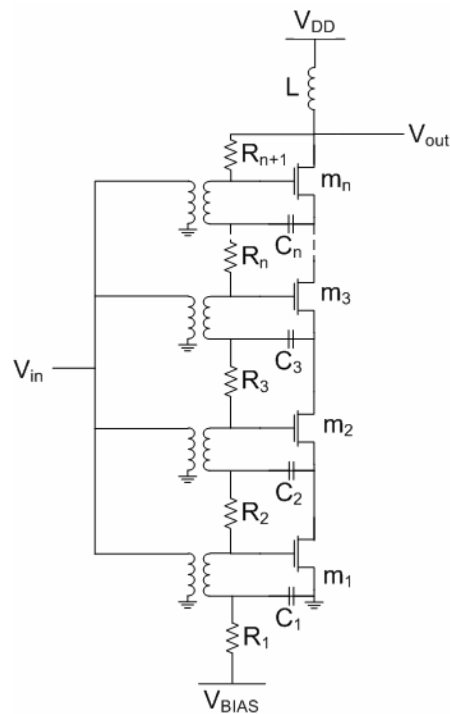

Figure 31 – Stacked Transistor Architecture

3.5.2.1 Transmission-Line Power Combining

As the operating frequency of transceivers moves into the millimetre wave spectrum the size of transmission lines scale inversely. This facilitates the use of on-chip transmission line based combining. Slow-wave structures have also been presented [75], [62] that improve the quality factor and reduce the dimensions of transmission lines. Lumped equivalent circuits have also been used in the low GHz range to synthesise transmission-line power combining circuits. In this section the most prominent power combining structures will be discussed.

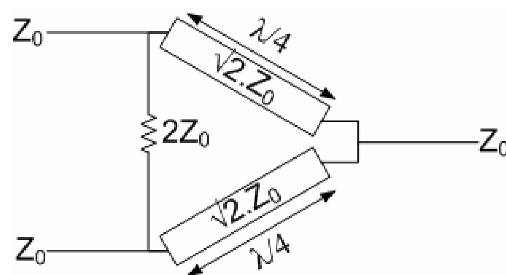

Figure 32 – Wilkinson Power combiner

Wilkinson and Corporate Power Combining

The Wilkinson power combiner [99] shown in Figure 32 ideally allows lossless power combining when the output ports are matched, with only the reflected power dissipated.

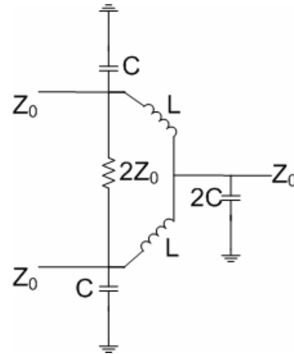

Figure 33 – Lumped Element Wilkinson Power combiner

In the centimetre-wavelength range the size of the transmission lines hinder the application of the distributed element combiner and power amplifier designers have instead focussed on lumped element equivalent implementations as shown in Figure 33. As the frequency increases into the millimetre-wavelength range transmission lines and distributed elements become more practical.

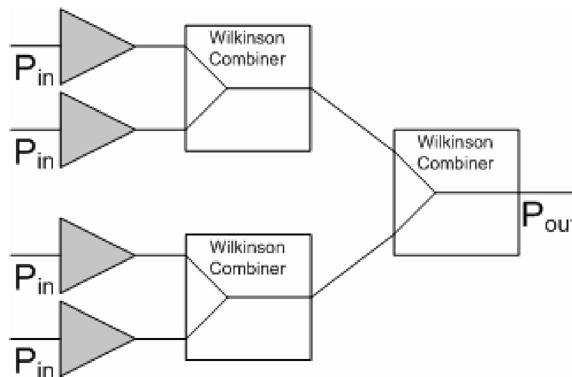

Figure 34 – Corporate Power Combiner

A corporate power combiner extends the Wilkinson power combiner by employing several stages of combiner into the one larger structure, shown in Figure 34. The corporate combiner similarly also suffers at centimetre-wavelength frequencies to the large die area required for distributed implementation, but is again more practical at higher millimetre-

wave frequency although the author cannot find an example of this technique being implemented at these frequencies. Lumped implementations are also problematic due to the complexity of the networks required.

Doherty Power Amplifier Combiner

The Doherty amplifier uses multiple amplifiers to boost average efficiency, with each amplifier contributing to the output power only over some subset of the overall power range, similar to the concept of a turbocharger. The concept first proposed by Doherty [21], used two amplifiers, a main and an auxiliary which will be disused below.

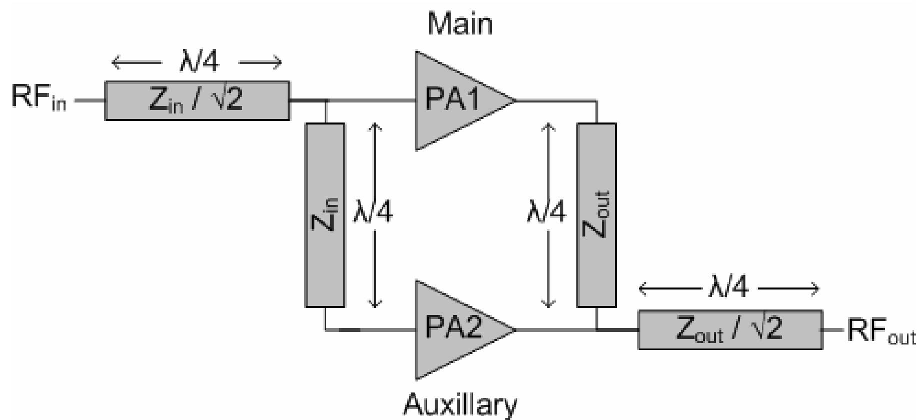

Figure 35 – Two amplifier Doherty Amplifier Architecture [95]

The Doherty amplifier consists a quarter wavelength, λ/4, input transmission line network to split the input signal between the two amplifiers and a quarter wavelength transmission-line connecting the input to the main amplifier cell with characteristic impedance of Z_0, and a quarter wavelength transmission line with characteristic impedance of $Z_0/\sqrt{2}$ connecting the inputs of the main amplifier cell with the auxiliary amplifier cell. A second quarter wavelength transmission line network is used to combine the outputs of the two amplifiers, with the output transmission line connection used to compensate for the phase shift of the splitter and combining the output currents in phase. The main amplifier is biased with a larger conduction angle compared to the auxiliary amplifier with the main amplifier biased in class AB and class C. The result of this biasing is for a high input signal both amplifiers are at their maximum output power each amplifier and will see an equal load and as the power of the input signal is reduced the auxiliary amplifier drain current turns off, leaving

only the main amplifier is active. This technique, termed the active load-pull technique, causes the reactance of the load to vary by combining current from a second in-phase source.

The operation of the Doherty amplifier, model shown in Figure 36, can be approximately analysed using three regions of operation, a high power region where both amplifiers are fully on, 0 dB backoff point, a middle region where the auxiliary amplifier contributes a proportion of its maximum output power, 0 – 6 dB backoff, and a low power region where the auxiliary amplifier is has insufficient signal power to turn on, greater then 6 dB backoff. The details relevant to this thesis are presented below; if the reader is interested a more detailed explanation is found in [10].

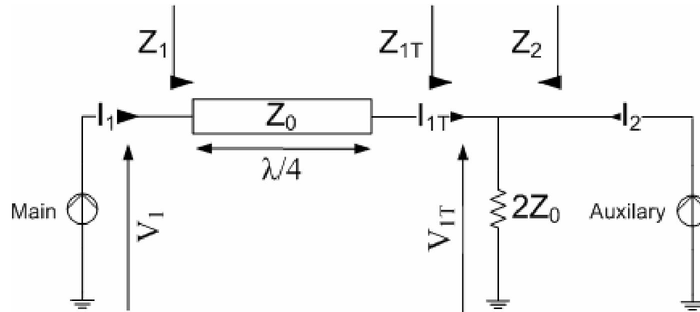

Figure 36 – Doherty Amplifier output model

Letting each of these regions correspond to a ξ value between 0 and 1 corresponding to the proportion of its maximal output the auxiliary amplifier is producing allows RF currents from the current sources to be expressed in the form,

$$I_1 = \frac{I_{MAX}}{4}[1+\xi], \qquad \text{Equation 11}$$

$$I_2 = \frac{I_{MAX}}{2}\xi . \qquad \text{Equation 12}$$

The effective resistances, Z_{1T} and Z_2, can now be expressed in the form,

$$Z_{1T} = R_L\left(1+\frac{I_2}{I_{1T}}\right), \qquad \textit{Equation 13}$$

$$Z_2 = R_L\left(1+\frac{I_{1T}}{I_2}\right). \qquad \textit{Equation 14}$$

With the relationship between the input and output voltages and currents of the quarter-wave transmission line expressed as,

$$\begin{aligned} V_{1T}I_{1T} &= V_1 I_1 \\ Z_0{}^2 &= \left(\frac{V_{1T}}{I_{1T}}\right)\left(\frac{V_1}{I_1}\right), \\ I_{1T} &= \frac{V_1}{Z_T} \end{aligned} \qquad \textit{Equation 15}$$

Substitution of I_{1T} in the expression for Z_{1T}, gives

$$Z_{1T} = R_L\left(1+\frac{I_2 Z_T}{V_1}\right). \qquad \textit{Equation 16}$$

Solving for the impedances at the output devices,

$$\begin{aligned} Z_1 &= \frac{Z_T{}^2}{Z_{1T}} \\ &= \frac{Z_T{}^2}{R_L\left(1+\frac{I_2}{I_{1T}}\right)} \\ Z_2 &= R_L\left(1+\frac{I_{1T}}{I_2}\right) \end{aligned} . \qquad \textit{Equation 17}$$

Output resistance of the load for the three regions of operation can now be calculated, these highlight the change in output impedance seen from the main amplifier;

For the high power region where both amplifiers are fully on, thus the 0 dB backoff point,

$$I_{1T} = I_2 \qquad Z_1 = \frac{{Z_T}^2}{2R_L}. \qquad Z_2 = 2R_L \tag*{Equation 18}$$

For the middle region where the auxiliary amplifier contributes a proportion of its maximum output power, thus 0 – 6 dB backoff,

$$Z_1 = \frac{{Z_T}^2}{R_L\left(1 + \frac{I_2}{I_{1T}}\right)}. \qquad Z_2 = R_L\left(1 + \frac{I_2}{I_{1T}}\right) \tag*{Equation 19}$$

For the third state, a low power region where the auxiliary amplifier is has insufficient signal power to turn on, thus greater then 6 dB backoff,

$$I_2 = 0 \qquad Z_1 = \frac{{Z_T}^2}{R_L}. \qquad Z_2 = \infty \tag*{Equation 20}$$

Finally, solving for V_1,

$$V_1 = \left(\frac{Z_T}{2R_L}\right)\left(\frac{I_{MAX}}{2}\right)\left(Z_T + \zeta\left(Z_T - \frac{R_L}{2}\right)\right). \tag*{Equation 21}$$

This produces a rather surprising result; if the characteristic impedance of the output transmission line is equal to $\frac{1}{2}R_L$ then the output voltage amplitude will remain constant at the maximum voltage swing of V_{DC}, as shown in Figure 38, whilst the current amplitude increases, shown in Figure 37, and the maximum efficiency will be maintained for the main

amplifier during the 6 dB backoff, total efficiency of the Doherty amplifier for differing levels of backoff is shown in Figure 39.

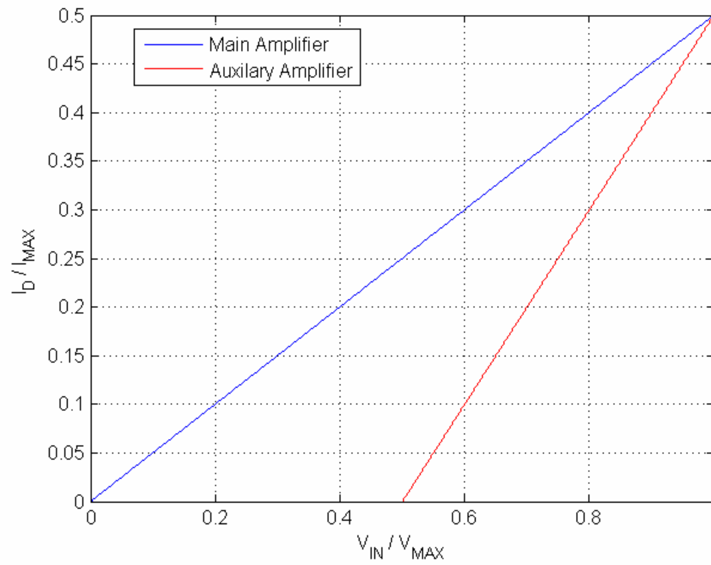

Figure 37 – Doherty amplifier main and auxiliary device currents

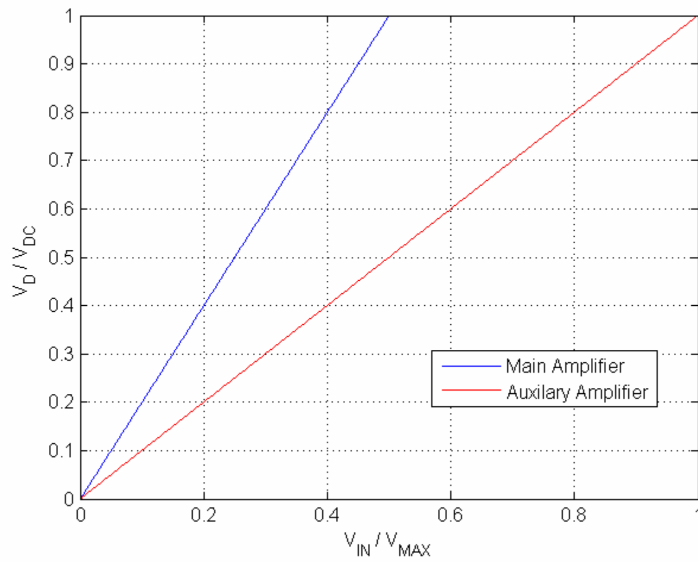

Figure 38 – Doherty Amplifier main and auxiliary device voltages

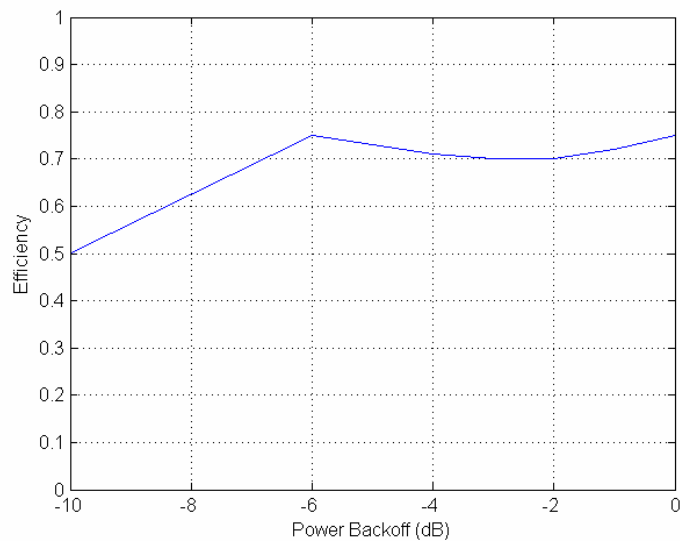

Figure 39 – Doherty Amplifier efficiency versus power backoff level.

3.5.2.2 Transformer Based Power Combining

Transformers are a widely used as a means to split or combine power. The theory is well documented and the devices uncomplicated to design. Implementations of on-chip transformers on CMOS have suffered though due to the high level of parasitics and the high insertion loss of the process causing on-chip transformers to have relatively high loss. Aoki et al. [1] have presented a design of a distributed active transformer shown in Figure 40 using lumped components to achieve high efficiencies.

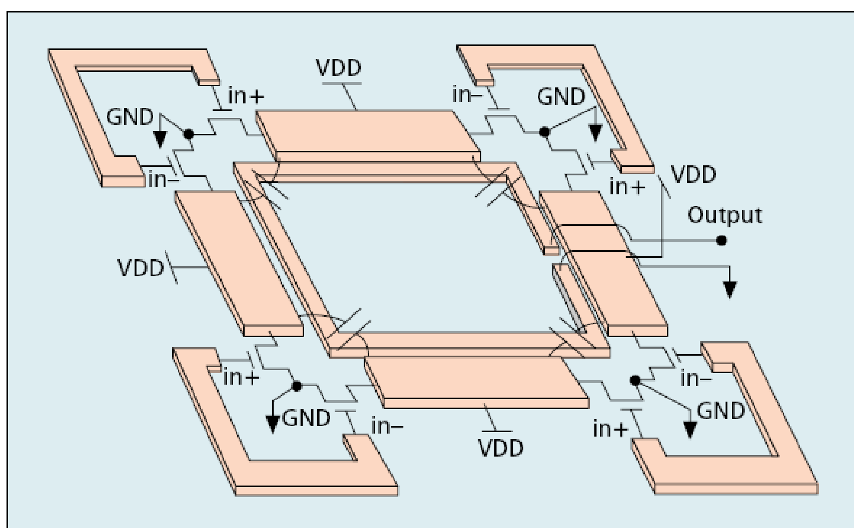

Figure 40 – Topology of distributed active transformer [1]

Doan et al. [DOAN] have presented a fully integrated class AB power amplifier in CMOS at 5.8 GHz, shown in Figure 41.

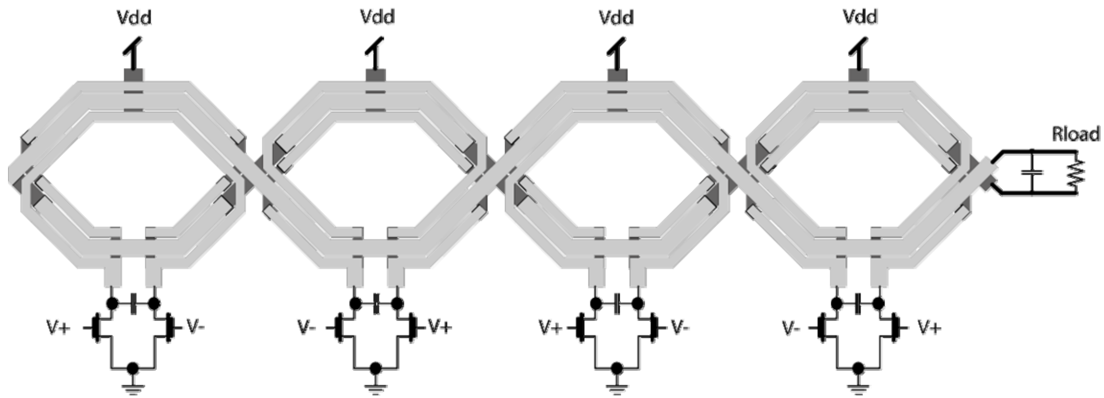

Figure 41 – Topology of on-chip transformer [52]

3.6 Passive Techniques for Power Amplifier Design

The fundamentals of designing passives for power amplifiers will be covered in this section.

3.6.1 Resonance

Taking a series resistive, inductive and capacitive (RLC) circuit, Figure 42, as a simple example to illustrate resonance the impedance seen at the input is given as Equation 22. The resistors, capacitors and inductors will all be assumed to be ideal.

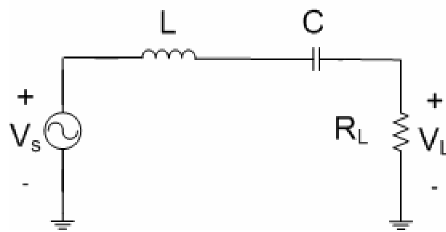

Figure 42 – Series RLC Circuit

$$
\begin{aligned}
Z &= jwL + \frac{1}{jwC} + R \\
&= R + jwL\left(1 - \frac{1}{w^2 LC}\right)
\end{aligned}
\qquad \textit{Equation 22}
$$

At the resonant frequency the impedance is purely real, $Im(Z) = 0, w = \pm\frac{1}{\sqrt{LC}}$ the impedance, by observation, will be minimal. At resonance both the capacitor and the inductor voltage magnitudes are equal but 180 degrees out of phase, and thus the voltage across the capacitor and inductor can be much larger then V_O, the circuit has voltage gain (though obviously not power gain). Using Ohm's Law the voltage across the inductor and capacitor are given below.

$$v_L = jw_o Li = jw_o L\frac{v_S}{R} = jQ \times v_s$$
$$v_C = jw_o Li = \frac{1}{jw_o C}\frac{v_S}{R} = -jQ \times v_s$$

Equation 23

Where Q has been defined as at resonance as,

$$Q = \frac{w_o L}{R} = \frac{\sqrt{\frac{L}{C}}}{R} = \frac{Z_o}{R}$$

Equation 24

3.6.1.1 The Importance of Q

Bandwidth

When the transfer function of the series RLC circuit is plotted, Figure 43, we see that the bandwidth of the circuit reduces inversely to the Q factor.

At the limits an infinite Q the circuit is perfectly selective and only allows signals of w_0 to pass to the load and a Q of zero would allow all signals to pass to the load. From this the reader can conclude that the as normalised bandwidth is inversely proportional to Q. For the proofs the reader can look to [61].

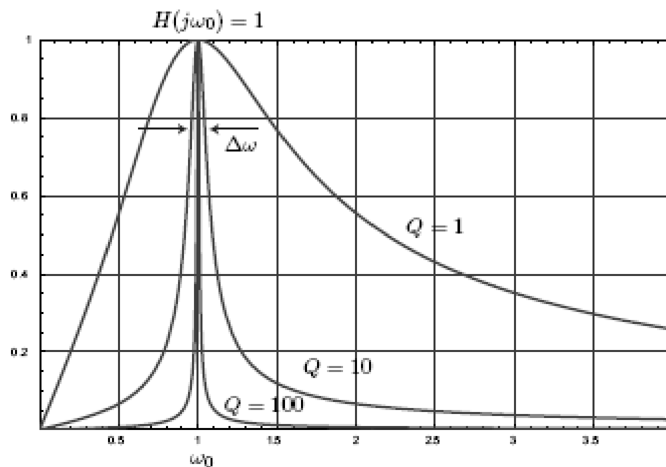

Figure 43 – Transfer Function of a Series RLC Circuit [61]

Low Insertion Loss

A lower Q value reduces the insertion loss as the power dissipation for the network increases as Q increases. The proof for this can be found in most texts, if the reader is interested including [5], [61] but the mathematics wont be repeated hear except for the ultimate result, Equation 25.

$$IL = \frac{1}{1 + \frac{Q}{Q_C}} \qquad \textit{Equation 25}$$

This simplified equation states that the Q normalised to the individual components Q is inversely proportion to the IL.

Susceptance to Process Variations

This quality follows from the previous advantages of a low Q and is rather initiative. In a high Q circuit, for example a voltage controlled amplifier, the frequency will shift with process variation and this will be especially pronounced as the process variations will shift the centre frequency whereas in a low Q circuit a shift in centre frequency will be minor as the bandwidth is large.

3.6.2 Matching Networks

Matching Networks are the glue that binds the active devices together. They are used to change a given load reactance, Z_L, to match a given source reactance, Z_S. This is achieved by inductive and capacitive elements combined in series and parallel. Figure 44 displays a generic matching network visualized as a black box.

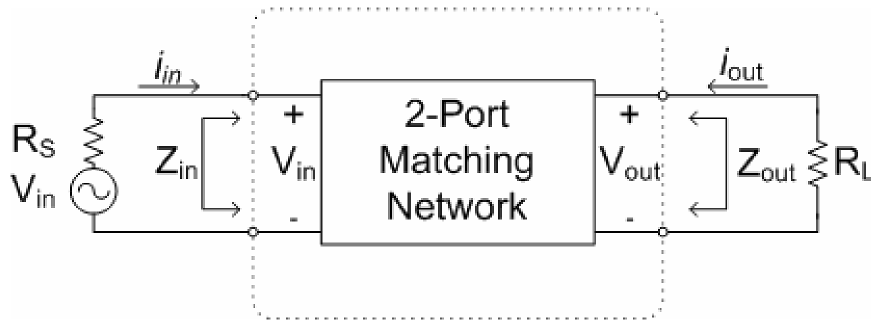

Figure 44 – Generic 2-Port Matching Network

Using Ohm's Law the load and source resistances can be stated as $R_L = v_o / i_o$ and $R_S = v_i / i_i$. Therefore a transformation from a source impendence to a load impedance may be achieved by a voltage gain or loss, $v_i = k\ v_o$. Assuming the black box matching network is realized with only memory less passive elements therefore power will be conserved, Equation 27.

$$i_i v_i = i_o v_o \qquad \textit{Equation 26}$$

This transformation will also require the current to change by the reciprocal of k, $i_i = k^{-1}\ i_o$. Equation 27 shows the result of this transformation.

$$Z_{in} = \frac{v_i}{i_i} = \frac{kv_o}{k^{-1}i_o} = k^2 \frac{v_o}{i_o} = k^2 R_L \qquad \textit{Equation 27}$$

3.6.2.1 Benefits of Matching Networks

Matching Networks are the bain of a RF circuit designer (especially at high frequencies with limited gain). So why spend all this time matching networks?

Optimal Power Transfer

Optimal Power Transfer is the imperative need of the Power Amplifier. Matching circuits allow maximum power to transfer from source to load by transforming the source and load impedance to the values that allows maximum power transfer.

Analysis of Figure 44 without the matching network the optimum load resistance for power transfer is performed below.

$$V_o = \frac{V_{SRC} R_L}{R_S + R_L}$$

$$P_O = \frac{V_L^2}{R_L} \qquad \textit{Equation 28}$$

$$= \frac{V_o^2 R_L}{R_S + R_L}$$

Differentiating P_o with respect to R_L to find the stationary point of the curve when the derivative is zero.

$$P'_O = \frac{V_L^2}{R_S}$$

$$= \frac{V_o^2 (R_S - R_L)}{R_S + R_L} \qquad \textit{Equation 29}$$

From Equation 29 the stationary point of the curve is found at $R_S = R_L$. Using a matching network the optimal impedance match occurs for $R_L = Z_{OUT}$ and $R_S = Z_{IN}$. Therefore, a matching network allows the matching of differing source and load resistances and to produce an optimal power transfer.

Power Transfer Example

The need to transform reactance in order to facilitate power transfer will be illustrated with an example. Using a generic class-A power amplifier topology with a 1.5-V supply, shown in *Figure 19*, the maximum output power able to be delivered to the 50-Ω load is calculated.

$$P_{OUT} = \frac{V_{dd}}{2 \cdot R_L} = \frac{1.5^2}{2 \cdot 50} = 22.5mW \qquad \textit{Equation 30}$$

Whilst this output power maybe sufficient for select applications, in order to transmit larger output powers, for example 250mW, are possible by transforming the output load into a lower resistance.

$$R_L = \frac{V_{dd}}{2 \cdot P_{OUT}} = \frac{1.5^2}{2 \cdot 250mW} = 4.5\Omega \qquad \textit{Equation 31}$$

In reality many more issues, such as layout parasitics and bandwidth are involved in the selection of the load resistance transformation.

Stability

An unstable circuit will oscillate which is undesirable for a power amplifier. There are various reasons that an amplifier will become unstable but the most likely is poor input and / or output termination.

At lower frequencies transfer function are commonly available and the Nyquist criteria provides a safe indication of stability. A summary of this technique can be found in most control literature including [31]. At RF and higher frequencies as the broadband nonlinear models are not always available and instead a frequency domain based analysis is required.

For this purpose RF circuit stability is calculated at individual frequencies using the small signal two port s-parameters. Due to the limitations of s-parameters, only modeling linear responses, it is only possible to model small signal circuit and linear applications. This can cause problems as the power amplifier may operate in the nonlinear region during normal operation. For the analysis linear operation will be assumed and this is sufficient for our purposes.

For K > 1, Equation 32 and Bf > 0, Equation 33, derived from the small signal parameters, shown in [87], a power amplifier will be unconditionally stable. A typical response is shown in Figure 19.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}.S_{22} - S_{21}.S_{12}|^2}{2|S_{12}.S_{21}|} \qquad \text{Equation 32}$$

$$B_1 = \frac{1 + |S_{11}|^2 - |S_{22}|^2 - |S_{11}.S_{22} - S_{21}.S_{12}|^2}{2|S_{12}.S_{21}|} \qquad \text{Equation 33}$$

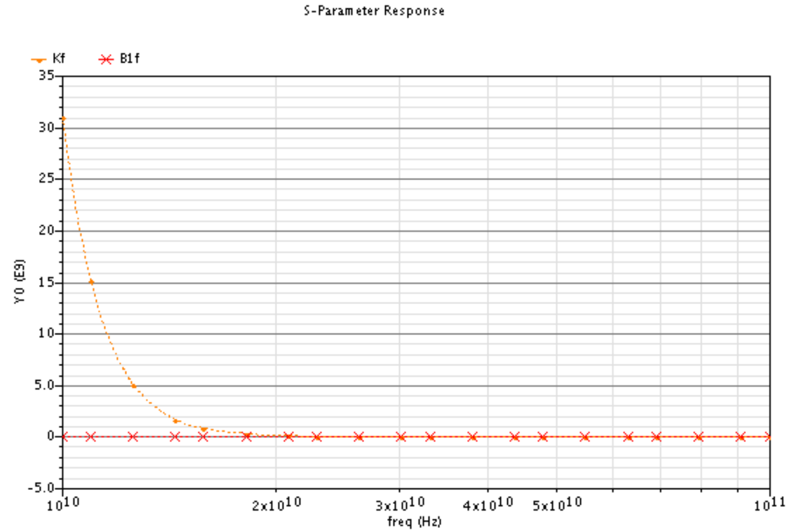

Figure 45 – Example of a typical Stability Response

Optimal Noise Figure

The noise figure, F, is a measure of the noise performance of the system. It is defined as the total noise output power divided by the output noise due to input source. The main protagonists of noise are the Thermal Noise, noise to randomly varying nature of current in a conductor, Shot Noise, due to the nonlinearity of a device and Flicker Noise, due to the physical markup of the devices.

For a N-stage device the overall noise figure, F_N, is given as [5],

$$F_N = F_1 + \frac{F_2 - 1}{G_1} + \ldots + \frac{F_{N-1} - 1}{G_1 G_2 \ldots G_{N-1}} \qquad \text{Equation 34}$$

The implication of this equation is that the PA located almost at the end of the transceiver has negligible effect on the noise figure and thus the matching networks will only be minimally optimized for the matching networks.

Minimum Reflections in Transmission Line

Without proper terminations reflections can lead to interference due to the reflections that occurs at both the source and load terminations. This interference becomes severe when individual transceiver components are connected together. It is imperative that these are minimized, and are covered in the specifications as input and output voltage standing wave ratios [5], [30], [31], [61].

Optimal Efficiency

Another use of matching networks is to increase the efficiency of circuits. Whilst a complex impedance match will result in maximum power transfer, the maximum efficiency almost exclusively occurs for a different resistance.

$$\eta = \frac{P_L}{P_{dc}} = \frac{1}{2}\frac{v_o i_o}{I_Q V_{SUP}} \qquad \textit{Equation 35}$$

The optimal efficiency can be achieved in multiple ways but probably the most prominent is in the ability of a matching network to transform load impedances. A 50 or 75 ohm load can be transformed into a low resistance load that a power amplifier usually requires for high efficiency. Further investigation is performed in [5], [31], [61].

3.6.2.2 Types of Matching Networks

The following subsection will describe the matching networks used in the design of the 60GHz Power Amplifier. It is by no means a complete list of matching networks and a more thorough investigate can be found in [31], [50].

L-Match Network

An L-Matching Network, *Figure 46*, is named due to the topology. It is used to boost the load impedance.

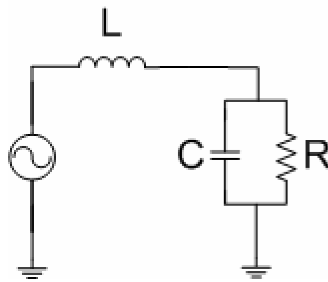

Figure 46 – L-Matching Network[15]

Figure 46 is a simple RLC circuit connected to a power source and recalling from the previously theory on matching networks the resistance seen by the source is Q^2 larger than R_L. For example, if the gate resistance of the NFET device was 5 ohms and needed to be matched to an input impendence of 50 ohms a Q of approximately 3.3 would be required. This is a common situation that occurs at the input port of a power amplifier. Considering impedances as lumped greatly simplifies the task of building a matching network, though in RF design all impedances are distributed and simulations are required to adequately characterise these networks. This will be discussed further in later sections.

Pi-Matching Network

Also named due to the topology of the circuit the pi-matching network is a cascade of L-matching networks. This allows for a lager degree of freedom when designing the network.

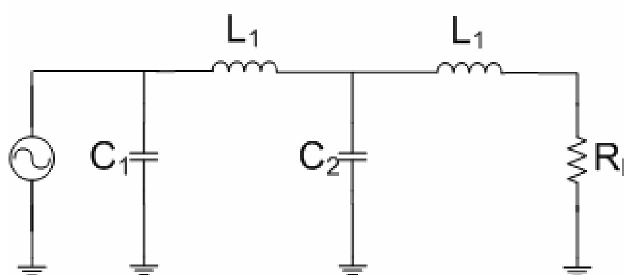

Figure 47 – PI-Matching Network

Figure 47 shows a pi-matching network connected to a load. Using multiple stages allows for a smaller Q then over a single stage design. A pi-matching network is used in the design of a typical power amplifier to connect the output of the amplifier stages to the input of the following stages with the reduction in Q increasing the bandwidth of the amplifier.

3.7 Figures of Merit

The performance of power amplifiers are described by their figures of merit (FOM). These FOM guide the hand of the designer, and are usually influenced by system level requirements, set by regulation or standards bodies. Linearity and Efficiency are inherently the two difficulties that a RF power amplifier designer faces (i.e. a power amplifier can never be too efficient or linear), and as such will be covered here in detail. Both theses as both cover a wide number of sub-metrics used to differentiate power amplifiers including saturated power levels, compression point levels, drain efficiency and power added efficiency, amongst others.

3.7.1 Linearity

Linearity is a highly desired feature of power amplifiers. Many radio frequency systems are based on orthogonal frequency division multiplexing (OFDM) or other complex modulation schemes. These complex modulation schemes are characterized by a high peak to average power ratio (PAPR) and require low distortion to preserve the integrity of the signal and in order to minimize intercarrier interference. High linearity preserves the integrity of the signal and allows recovery at the receiver. Signals distorted by due to nonlinearities cause unwanted distortion products to leak outside the channel and present unwanted interference to other spectrum users.

A distortion analysis of a power amplifier is highly mathematical, power and Taylor series have been employed to analyse the distortions [5], [34]. Linearity will be discussed in this section with the aid of Taylor series such as the transfer characteristic of a single-ended power amplifier, expressed below:

$$s_o(t) = \sum_{n=1}^{\infty} a_n s_i(t) = a_1 s_i(t) + a_2 s_i(t)^2 + a_3 s_i(t)^3 + \ldots \qquad \textit{Equation 36}$$

3.7.1.1 Amplitude Modulation (AM)-to-Amplitude Modulation (AM) Distortion

AM-to-AM modulation distortion covers the class of distortion arising from the relationship of the amplitude of the input and output signals of the power amplifier. The most common metrics used when discussing AM-to-AM distortion are the points of compression and saturation. These compression points describes the point at which the

gain is compressed by a certain proportion, thus the point at which the small-signal power gain is compressed by one decimal is the one decibel compression point (P_{1dB}), this can be specified as both input or output referred. The point at which the output power reaches a maximum is the power saturation point (which if you think about it is actually the infinite decibel compression point). Lastly, the intermodulation products, where the input signal frequencies intermodulate producing distortion will be discussed.

Compression Points

Input a sinusoidal frequency signal into the system described by Equation 36, such as;

$$s_i(t) = s\cos(\omega t) \qquad \textit{Equation 37}$$

The output produced, in a single ended power amplifier is thus;

$$s_o(t) = a_1 s\cos(\omega t) + a_2 s^2 \cos(\omega t)^2 + a_3 s^3 \cos(\omega t)^3 + \ldots \qquad \textit{Equation 38}$$

Now only the fundamental and the even harmonics will add at the fundamental frequency, so ignoring the higher order terms;

$$G = a_1\left(1 + \frac{3}{4}\frac{a_1}{a_3}s^2 + \ldots\right) \qquad \textit{Equation 39}$$

The coefficients will have opposite signs, therefore causing the gain to compress as the amplitude of the input signal increase. Equation 39 can be solved for the P_{1dB} compression point;

$$P_{1dB,input} \approx \sqrt{0.15\left|\frac{a_1}{a_3}\right|} \qquad \textit{Equation 40}$$

Figure 51 displays the two-tone output spectrum of a CMOS millimeter-wave power amplifier for automotive radar applications. An example of fundamental compression of the amplifier is evident, with the P_{1dB} highlighted at 1 dBm.

Saturation Point

The saturation point (or the infinite compression point) is the point at which the fundamental output becomes, independent of the input and, constant. It denotes the maximum output level. Figure 51 is an example of fundamental compression and shows saturation point to be approximately 2 dBm.

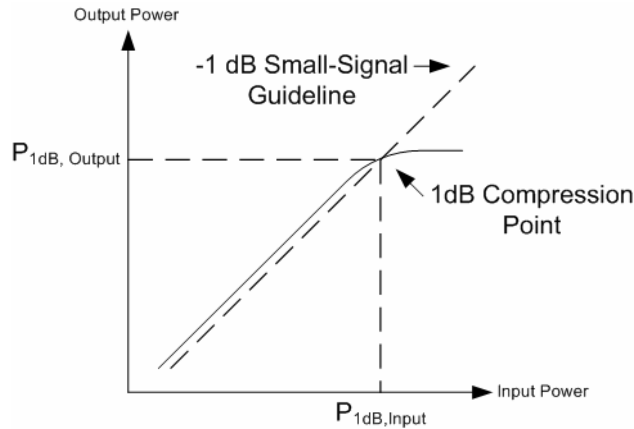

Figure 48 – Definition of 1-dB compression point.

Intermodulation Distortion

Intermodulation creates an insidious form of distortion that arises from the odd higher order terms that we have so far ignored, though the cubic term is often considered the dominate and as such we will ignore the higher terms. Consider a simple input signal consisting of two in-band signals of the same amplitude. Two signals of differing amplitudes can be considered which leads to cross-modulation, where the amplitude of the smaller input signal is modulated by the amplitude of the larger input signal, but this is rarely used as a metric, the reader is encouraged to visit [5], [10] for more analysis.

$$s_i(t) = s\left(\cos(\omega_1 t) + \cos(\omega_2 t)\right) \qquad \textit{Equation 41}$$

The output from such an input in the system as described in Equation 36 becomes

$$s_i(t) = a_1 s\big(\cos(\omega_1 t) + \cos(\omega_2 t)\big) + \\ a_2{}^2 s\big(\cos(\omega_1 t) + \cos(\omega_2 t)\big)^2 + \\ a_3{}^3 s\big(\cos(\omega_1 t) + \cos(\omega_2 t)\big)^3 \\ + \ldots \qquad \textit{Equation 42}$$

Expanding the cubic term

$$a_3 s^3\big(\cos(\omega_1 t) + \cos(\omega_2 t)\big)^3 = \\ \frac{a_3 s^3}{4}\big(\cos(3\omega_1 t) + 3\cos(\omega_1 t)\big) \\ + \frac{a_3 s^3}{4}\big(\cos(3\omega_2 t) + 3\cos(\omega_2 t)\big) \\ + \frac{3a_3 s^3}{4}\big(2\cos(\omega_1 t) + \cos(2\omega_2 - \omega_1)t + \cos(2\omega_2 + \omega_1)t\big) \\ + \frac{3a_3 s^3}{4}\big(2\cos(\omega_2 t) + \cos(2\omega_1 - \omega_2)t + \cos(2\omega_1 + \omega_2)t\big) \qquad \textit{Equation 43}$$

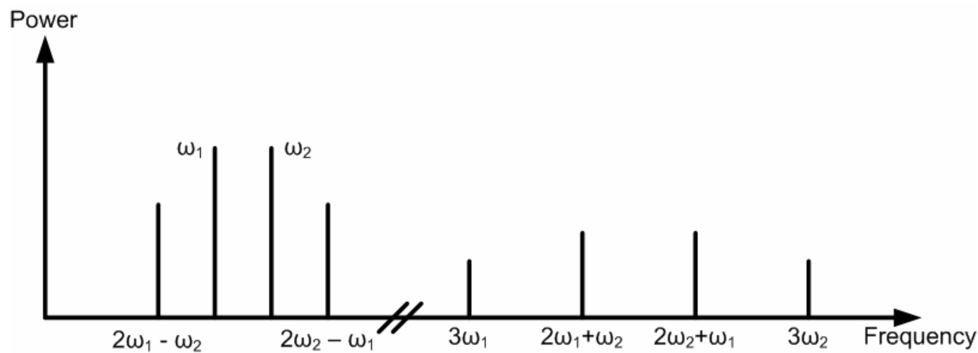

Figure 49 – The spectrum of the two-tone cubic intermodulation (IM3) products.

As the cubic higher order terms dominate, this distortion is known as the third-order intermodulation (IM3) products, with the spectrum shown in Figure 49. As these products are dependent on s^3, they increase at 3 times the rate of the fundamental or 3-dB for every 1-dB increase in input or output fundamental power. The definition of these third order parameters is shown in Figure 50. A typical output power graph resulting from two equal tones applied to a non-linear device is shown in Figure 51 with this steeper increase evident in the IM3.

Finally the point at which the tangent to the fundamental and the tangent to the third-order harmonics meet is defined as the IM3 intercept point, a purely descriptive term that conveys some idea about the linearity of the power amplifier, without paying too close attention to the mathematical rigours. For more information please consult [11].

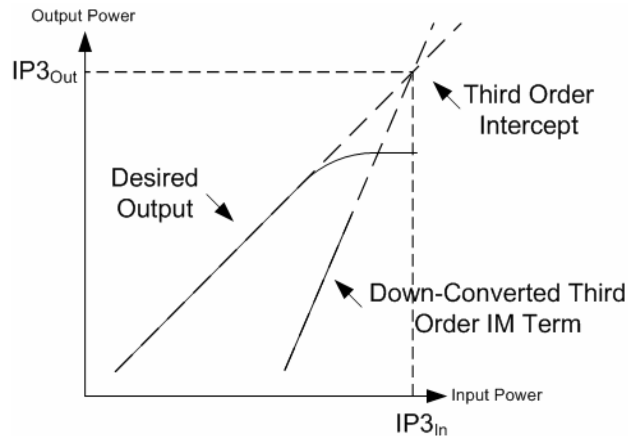

Figure 50 – Definition of third order linearity parameters.

3.7.1.2 Amplitude Modulation (AM)-to-Phase Modulation (PM) Distortion

Another category of distortion that plagues amplifier design is AM-to-PM distortion, a type of distortion that arises when the output phase of the amplifier is dependent on the input magnitude of the input [50]. AM-to-PM distortion is somewhat poorly covered in literature compared to AM-to-AM distortion, possibly due to the difficulty in measurements and lack of widely used metrics available. One significant contributing factor to this type of distortion in the design of power amplifiers is the input amplitude dependent biasing point, especially with respect to how this affects the amplitude dependent parasitic capacitances, especially in the active devices [90].

The mitigation of this type of distortion is especially vital in systems that employ complex coding schemes, such as OFDM. These schemes utilize both phase and amplitude to increase the throughput of the channel assuming orthogonally between AM and PM. Distortion invalidates this assumption, reduces throughput, increases bit-error rate, and if severe can cause a communication system to be ineffectual.

3.7.2 Efficiency

This section introduces and explains the various concepts of efficiency related to power amplifiers. Efficiency is one of the most important power amplifier metrics and is a measure of the amplifiers ability to convert direct current (DC) power to RF power. Power amplifiers with poor efficiency require large power wastage, which almost exclusively gets converted to heat, and thus requires the die to have a cooling solution. Efficiency can be calculated instantaneously or by an average, both these calculation will be discussed.

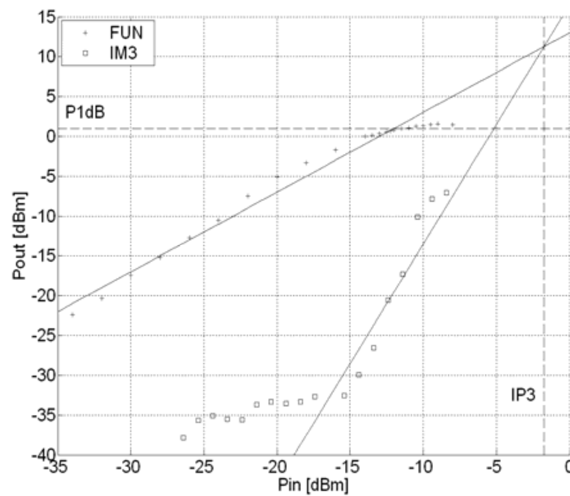

Figure 51 – Amplitude Compression for Fundamental and 3rd Order Intermodulation with 3rd Order Intercept Point Marked [94]

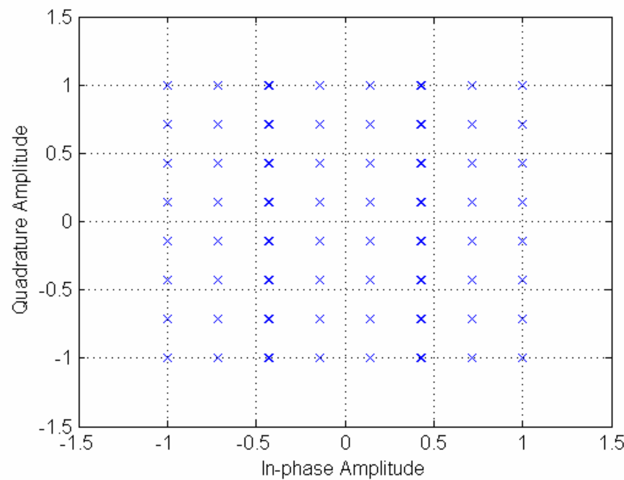

Figure 52 – An ideal 64-QAM Constellation.

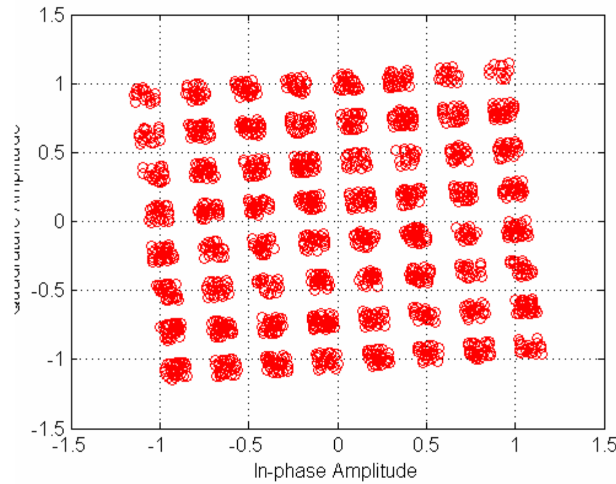

Figure 53 – A 64-QAM Constellation with AM-AM and AM-PM distortion.

3.7.2.1 Instantaneous Efficiency

Instantaneous efficiency is the efficiency of the power amplifier measured at one power output level. Calculation of a power amplifier's instantaneous efficiency is calculated in the literature using three differing methods, each will discussed below.

Drain Efficiency

Drain efficiency, denoted η_D, is defined as the ratio of output RF power P_{OUT} to DC power consumed from the power supply, P_{SUPPLY} (also equal to power consumer from the drain).

$$\eta_D = \frac{P_{OUT}}{P_{SUPPLY}} \qquad \text{Equation 44}$$

The drawback with using drain efficiency as a metric is that is independent of amplifier gain and essentially assumes that the gain is large and input power is negligible, unfortunately in RF power amplifiers the gain is may not be large and the input power may be significant.

Power Added Efficiency

Power added efficiency (PAE), denoted η_{PAE}, is defined as the ratio of the difference of output RF power to P_{OUT} input RF power P_{IN} to DC power consumed from the power supply, P_{SUPPLY}.

$$\eta_{PAE} = \frac{P_{OUT} - P_{IN}}{P_{SUPPLY}} \qquad \text{Equation 45}$$

It is also possible to express the PAE in terms of the gain of the amplifier, G, and the drain efficiency, η_D.

$$\eta_{PAE} = \frac{P_{OUT} - P_{IN}}{P_{SUPPLY}} = \frac{P_{OUT}(1-\frac{1}{G})}{P_{SUPPLY}} = \eta_D.(1-\frac{1}{G}) \qquad \text{Equation 46}$$

As the gain becomes large the PAE approximates the drain efficiency, as per the assumptions made for drain efficiency. By simple algebra it can also be shown that cascading individual amplifiers with the same PAE will produce a combined amplifier with the same total PAE.

Total Efficiency

Total Efficiency, denoted η_{PAE}, is the ratio of all output power, P_{OUT}, to all input power, both RF input power, P_{IN}, and DC input power, P_{SUPPLY}.

$$\eta_{PAE} = \frac{P_{OUT}}{P_{SUPPLY} + P_{IN}} \qquad \text{Equation 47}$$

This final efficiency metric, seemingly based on the principals of thermodynamics, will always be less then 100% as the total power out always less then the total power in. This metric is not frequently used in literature; instead most designers and authors use PAE as the metric for efficiency.

3.7.2.2 Average Efficiency

Instantaneous efficiency is fundamentally deficient as it is only a measure of efficiency at one particular output power level, usually at or close to the most efficient power level. For a time varying amplitude signal, such as an orthogonal frequency division multiplexing (OFDM) signal, or due to environmental factors, transmission distance, interference, and antenna orientation, will cause the output power to vary, the instantaneous efficiency to

vary, and thus the average efficiency will be less then the instantaneous efficiency. The average efficiency [68] measure overcomes this deficiency by calculating the average efficiency, which is a more practical measure of a transceivers performance, in a communication system. Average drain efficiency, denoted $\bar{\eta}$, is calculated as the ratio of the average output power, denoted $\overline{P_{OUT}}$, to the average power in, denoted $\overline{P_{IN}}$ and can be used with any of the instantaneous definitions of efficiency. For simplicity, the average drain efficiency will be calculated below;

$$\bar{\eta}_D = \frac{\overline{P_{OUT}}}{\overline{P_{SUPPLY}}} \qquad \textit{Equation 48}$$

Using the probability-density function (PDF) of the output power, $p(P_{OUT})$ the average output power, DC power and the drain efficiency can be calculated;

$$\overline{P_{OUT}} = \int_0^{P_{OUT,MAX}} P_{OUT}(P_{OUT}) \cdot p(P_{OUT}).dP_{OUT} \qquad \textit{Equation 49}$$

$$\overline{P_{SUPPLY}} = \int_0^{P_{OUT,MAX}} P_{SUPPLY}(P_{OUT}) \cdot p(P_{OUT}).dP_{OUT} \qquad \textit{Equation 50}$$

$$\overline{\eta_D} = \int_0^{P_{OUT,MAX}} \eta(P_{OUT}) \cdot p(P_{OUT}).dP_{OUT} \qquad \textit{Equation 51}$$

A linear class-A power amplifier will be used to illustrate the concept of average efficiency (rather poor average efficiency). A class-A amplifier operates wholly in the saturation region of the active device and thus there will always be dissipation due to the bias current and this can be reasonably approximated for a single tone by,

$$i_D = I_{DC} + i_{RF}\sin\omega_0 t\,, \qquad \textit{Equation 52}$$

where I_{DC} is the DC bias current, i_{RF} is the amplitude of the signal component of the drain current and ω_0 is the signal frequency. Equation 52 assumes ideal linearity and ignores the effects of distortion, but the equation is sufficient to illustrate the concept of average efficiency.

Continuing with the previous assumptions, the large inductor in the power amplifier will force a DC current from the supply and the AC pass capacitor will allow the RF current to pass through to the output of amplifier will be the RF signal from Equation 52 to pass to the load.

$$i_{RF,RMS} = \frac{i_{RF}}{\sqrt{2}}, \qquad \textit{Equation 53}$$

Therefore the voltage out will simply be the RF current from the drain thorough the load resistance, R,

$$\begin{aligned} v_{OUT} &= -i_{RF} R \sin \omega_0 t \\ v_{OUT,RMS} &= \frac{i_{RF} R}{\sqrt{2}} \end{aligned} . \qquad \textit{Equation 54}$$

Therefore calculating the efficiency power signal delivered to the load,

$$P_{OUT,RMS} = \frac{i_{RF}{}^2 R}{2}. \qquad \textit{Equation 55}$$

To keep our assumption of linear class A amplifier operation valid the DC current must be large enough to ensure the transistor will not enter cut off. Therefore,

$$I_{DC} \geq i_{RF}. \qquad \textit{Equation 56}$$

And finally, the DC input power (substituting in the pervious equation),

$$\begin{aligned} P_{SUPPLY} &= I_{DC} V_{DD} \\ &\geq i_{RF} V_{DD} \end{aligned} \quad . \qquad \textit{Equation 57}$$

Finally calculating the instantaneous drain efficiency,

$$\begin{aligned} \eta_D &= \frac{P_{OUT}}{P_{SUPPLY}} \\ &\leq \frac{i_{RF}{}^2 R}{2 i_{RF} V_{DD}} \\ &\leq \frac{i_{RF} R}{2 V_{DD}} \leq \frac{V_{DD}}{2 V_{DD}} \\ &\leq \frac{1}{2} \end{aligned} \qquad \textit{Equation 58}$$

Therefore, the maximum instantaneous efficiency for a class A power amplifier is 50%, and only occurs when the RF current is equal to the DC current, $i_{RF} = i_{DC}$. As the output power of the amplifier is backed off the instantaneous efficiency decreases linearly, as shown in Figure 54.

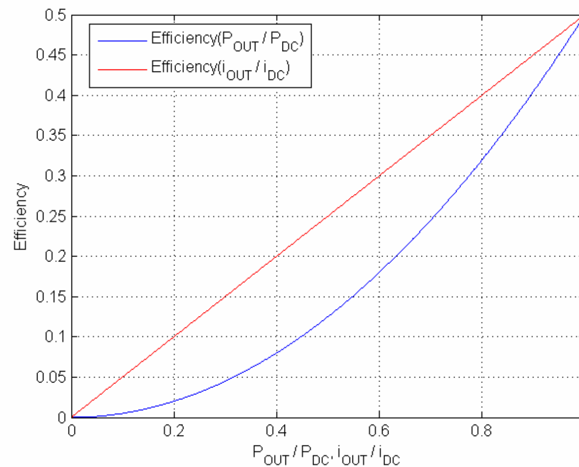

Figure 54 – Power efficiency of class A power amplifier referred to ratio of power out to power in and drain current to output current.

In the operation of a transmitter the output power, and subsequently the power amplifier output power is affected by many variables such as the transmit distance, path,

environment. This greatly affects the power output PDF, especially the operation of the class A amplifier in a backed-off mode. From Figure 54 it is evident has quickly the efficiency reduces with the reduction in output power. More efficient architectures, biasing and non-linear operation are required to reduce the power wasted.

3.8 Conclusion

In this chapter the fundamental concepts of power amplifier design were discussed including the classes of power amplifiers, matching networks, and the metrics used to design power amplifiers.

Chapter 4
A Fully-Integrated CMOS Millimeter-Wave Power Amplifier for Automotive Applications

4.1 Introduction

Worldwide more than 1.2 million people die and 50 million are injured worldwide in automobile accidents every year [82]. The European Union and other countries have set ambitious targets of reducing road deaths by 50% by 2010. According to General Motors [36] 49.2% of vehicle collisions could be avoided if cars were equipped with radar that assisted with braking, helped in inclement weather and provided the driver with a lane departure warning. In order to facilitate the deployment of these technologies, regulatory bodies such as the FCC have allocated spectrum 24-29 GHz, 46.7-46.9 GHz and 76-77 GHz bands for automotive radar [25].

An important consideration before these systems can be deployed in cars is their cost. Until recently, monolithic integrated circuits used to build radar components have been the domain of semiconductor technologies such as Gallium Arsenide (GaAs), Indium Phosphide (InP) and other more exotic III-V semiconductors. Although these materials exhibit superior performance compared to CMOS technology due to inherent characteristics including their higher electron mobility, ability to generate less noise, and higher transistor breakdown voltage they are prohibitively expensive for automotive applications.

Recent advancements in the CMOS process have allowed mm-wave components to be implemented using this technology [15]. Realizing MMIC devices in CMOS technology is the goal of many research groups and semiconductor companies [16], [105]. It is cheaper and allows for the integration of digital components necessary for radar signal processing and tracking: CMOS promises a higher level of integration for transceivers as it is inherently better for implementing low power logic circuits using complimentary devices, P-channel field effect transistors (FET), and has more metal layers that allows the

fabrication of complicated digital integrated circuits. CMOS enables integrated digital and analogue radio frequency (RF) components, either on a single chip, system-on-chip (SOC), or in a single package, System in Package (SinP) which further reduce the cost [6], [51], [53], [91].

In this chapter, the potential for MMIC automotive radar transceiver operating at 46.7 to 46.9 GHz compliant with [25] and implemented in 0.13-μm bulk CMOS is explored. In particular attention is focused to the power amplifier design. The power amplifier presented achieves a peak gain of 15.5 dB in channel with a 3-dB bandwidth of 44.5 GHz to 48 GHz. The 1-dB compression point greater than 1 dBm, saturated output power is greater than 1.5 dBm. To the best of our knowledge this is the only reported CMOS PA designed for operation in the 46.7-46.9 GHz automotive radar band. It achieves the highest S21 gain of any amplifier implemented in the 0.13-μm process greater then 40 GHz and is the only amplifier demonstrated in this process with a centre frequency between 40 GHz and 60 GHz.

4.2 Transceiver Architecture

In this section we outline the system architecture of the radar on a chip. In the current implementation the radio frequency front end is implemented as a homodyne receiver and is shown in Figure 55.

The air interface consists of an array of antennae embedded in the package. The size of each antenna is approximately half a wavelength in width and length or approximately 2.1mm on the epoxy based package. Each antenna has approximately 6dBi of gain and is circularly polarized by appropriately truncating the edges of the patch. The system has the ability to vary the direction of the transmit and receive beam. The phase of the signal at each patch antenna is controlled by a phase shifting circuit. In this design the phase of each antenna can be varied continuously by varying the voltage at the input of the varactor connected to each patch antenna. Immediately following the phase shifting circuit is a passive bandpass filter. This filter minimizes out of band transmit emissions and also reduces out of band receive energy from other sources such as other radars and jammers. The bandpass filter stops these other signals from reaching and saturating the transmit/receive switch or the first stage of the low noise amplifier. Following the

bandpass filter is a transmit/receive switch. This switch is required to enable the radio frequency front end to share the same antenna array for both transmit and receive. The low noise amplifier (LNA) amplifies the weak signal and provides signal gain at a minimal noise figure.

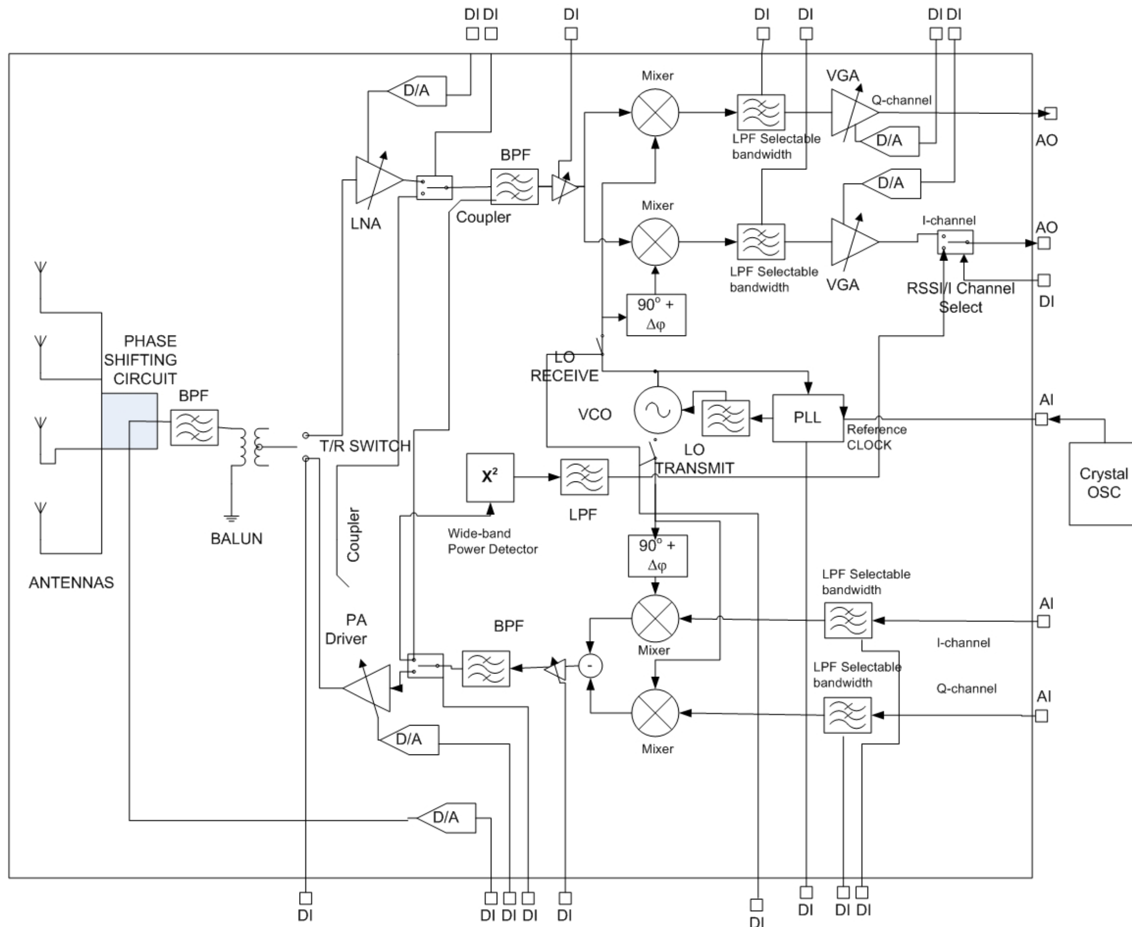

Figure 55 – Radio architecture illustrating the major components and functionality of the radar on a chip transceiver. [94]

After the LNA is a switch that either transports the signal from the LNA to the mixer or the output from the power amplifier after it has been attenuated by a -20dB coupler. Power amplifier distortion is device temperature and output envelope/waveform dependent. This feedback loop permits calibration of the power amplifier and permits digital correction for any in phase or quadrature (I/Q) amplitude and phase imbalance, amplitude to amplitude (AM/AM) or amplitude to phase (AM/PM) modulation that the power amplifier may introduce. The mixers are implemented as double balanced Gilbert cell mixers. This mixer

architecture offers better conversion gain, lower power consumption, better port to port isolation and cancellation of the second harmonic alleviating the need for an external of chip filter.

In this architecture a low phase noise high frequency stability and accuracy (20ppm) 100MHz external reference crystal is utilized to stabilize the VCO. The VCO is implemented utilizing a push pull architecture. The first stages of the fractional divider are implemented using two regenerative divide by 4 stages and subsequent division is performed digitally. In the subsequent sections we describe the design and implementation of the integrated power amplifier on CMOS for radar applications.

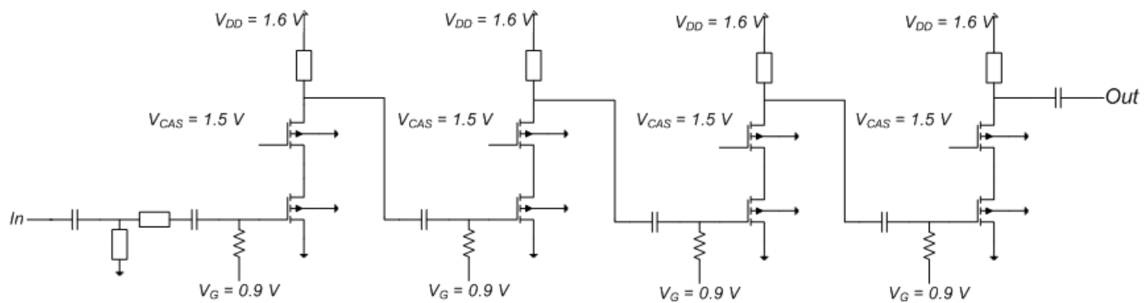

Figure 56 – Simplified Schematic of 46.7-46.9 GHz 4-stage power amplifier employing transmission lines. [94]

4.3 Design and Implementation

A power amplifier operating at 46.7-46.9 GHz was designed for a 0.13-μm CMOS technology as shown in Figure 56. The topology of the amplifier consists of four cascode stages, biased in "Class A" with input, output and interstage matching networks. Dimensions for the NFET transistors was investigated using simulations. These showed that the peak f_t current density remains constant at 200 μA/μm for varying finger widths for both the common source and cascode configurations and that the f_{max} current density increases until it plateaus above 200 μA/μm, Figure 57. Therefore a NFET transistor with a finger size of 2.5 μm and with 32 fingers per device for a total device size of 80 μm was chosen.

The power amplifier employs cascode transistors in order to increase gain by reducing the Miller Capacitance, and also to improve stability. Each cascode pair was biased at 200

μA/μm and possessed a maximum available gain (MAG) of 7 dB at 47 GHz. The transistors are biased from a 1.6-V rail to allow for a larger voltage swing and greater output power. This allows the individual transistors to remain below the rated breakdown voltage of 1.6 V.

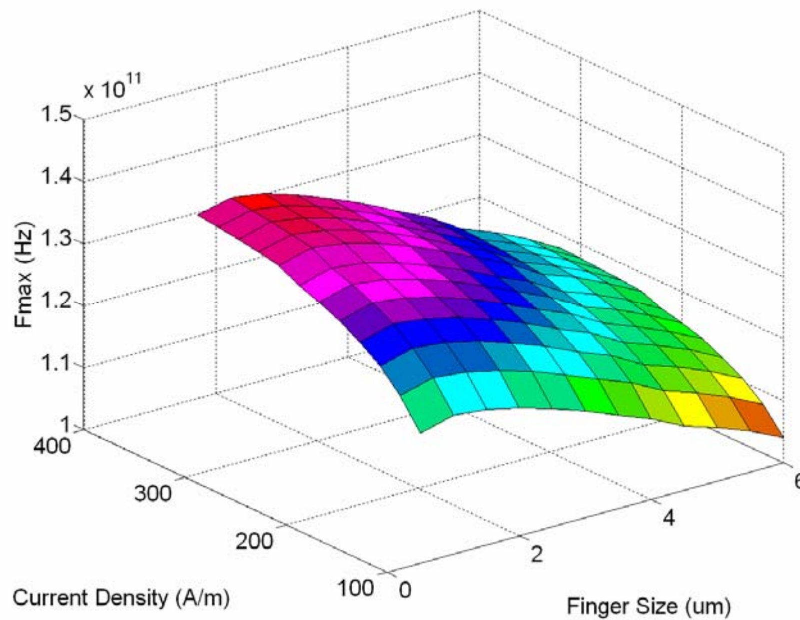

Figure 57 – Simulated f_{max} for varying device finger size and current density. Total device size was kept constant at 80 μm. [94]

Throughout the design, microstrip waveguides were used for impedance matching, interconnects and for biasing the common gate device. These lines were kept as short as possible in order to minimize losses and to reduce transmission line effects. Bias was provided to the common source device of the cascode via a large resistor. AC coupling has been used between each amplifier stage as well as at the input and output connection between the pads and amplifier stages. Input and output were both designed to be matched to 50 Ω. The insertion losses for the inter stage matching network was designed to be 1.9 dB, input matching network to 1.5 dB and output matching networks to 1.7 dB. These were all kept as low as possible to increase S21 gain.

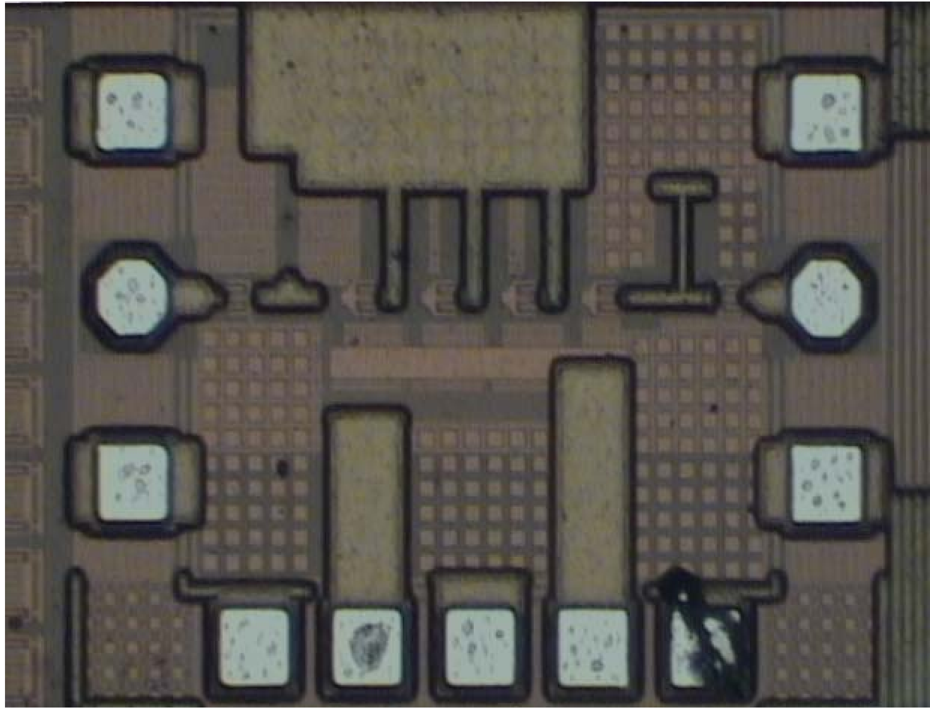

Figure 58 – Image of Fabricated Power Amplifier [94]

4.4 Fabrication and Results

The design was fabricated on a 0.13-μm lithography bulk CMOS process that supports high volume communications and data processing for digital applications. It is shown in Figure 58. It is specifically designed for low cost wireless applications especially for those in the low gigahertz spectrum (Bluetooth™ and Wi-Fi). This process consists of 8 metal layers, 3 thin copper layers on the bottom, then 2 thick copper layers, finally 3 radio frequency (RF) layers, 1 copper and 2 aluminium, are placed on top and covered by a final passivating layer consisting of silicon oxide, silicon nitride and polyimide. The fabricated device has a die size of 720 μm by 570 μm including all pads.

S-parameter measurements of the power amplifier was performed on wafer with a Suss-Microtech probe station with 65 GHz Ground-Signal-Ground (G-S-G) coplanar probes and a 65 GHz Anritsu Vector Network Analyser. Calibration was performed using a custom setup. This involved on-wafer calibration and calibration of the probe tips. The measured S-Parameters for the power amplifier are shown in Figure 59. The power amplifier achieves a peak power gain of 15.5 dB in channel with a 3-dB bandwidth of 44.5

GHz to 48 GHz, input power return loss greater than 10 dB, output power return loss greater than 10 dB and reverse isolation is greater than 30 dB.

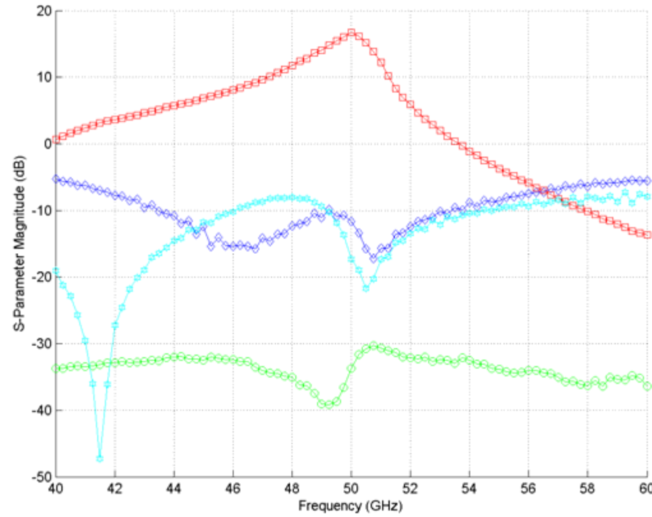

Figure 59 – Measured S-parameters of PA in decibel scale [94]

Figure 60 shows that measured output 1-dB compression point is greater than 1 dBm, maximum power output, P_{SAT}, is greater than 1.5 dBm and the IIP3 is -2 dBm. A summary of the measured results along with a comparison with state of the art amplifiers is provided in Table II.

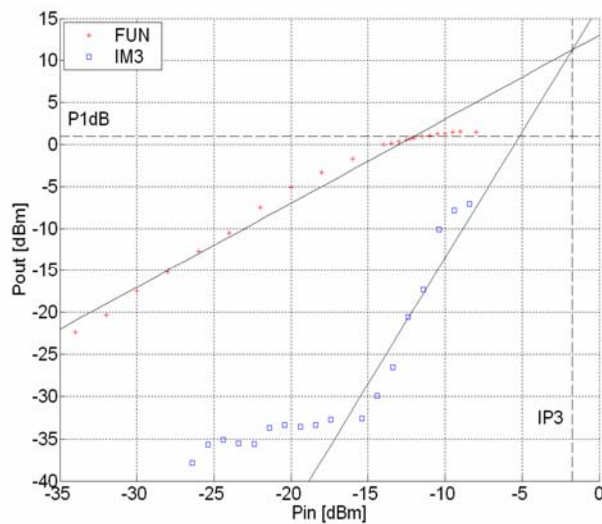

Figure 60 – Two-tone distortion for the power amplifier showing P_{SAT}, P_{1dB}, IP3. [94]

Technology CMOS	0.18-μm	0.18-μm	0.13-μm	90-nm	0.13-μm
Frequency [GHz]	24	25.7	60	60	46.8
Gain [dB]	10	8.9	12	5.2	15.5
3-dB BW [GHz]	-	23-27.5	51-65	52-65	44.5-46.9
Output P_{1dB} [dBm]	-	-1.3	+2.0	+6.4	+1
IIP3 [dBm]	-3.0	+2.8	-	+2.7	-2
NF [dB]	6.0	6.9	8.8	-	-
S_{11} [dB]	-14	< -14	< -15	< -3	< -10
S_{22} [dB]	-	< -12	<-15	< -10	< -10
S_{12} [dB]	-	< -32.5	< -45	< -30	< -30
Reference	[29]	[108]	[3]	[105]	This Work

Table II – Comparison of the automotive amplifier with published mm-wave CMOS amplifiers [94]

4.5 Conclusion

In this chapter a millimeter-wave power amplifier was designed for automotive radar applications and fabricated using a mainstream standard CMOS technology. A 4-stage cascode amplifier operating at 46.7 to 46.9 GHz with all input, output and inter stage matching networks has been implemented on chip.

Chapter 5
A 75 – 95 GHz Wideband CMOS Power Amplifier

5.1 Introduction

Currently, the monolithic millimeter-wave integrated circuits (MMIC) used in the 71 – 76 GHz, 81 – 86 GHz and 92 – 95 GHz fixed point-to-point bands and the 77-GHz vehicular radar band, shown in Figure 61, are the domain of type III-V semiconductor technologies such as the Gallium Arsenide (GaAs), Indium Phosphide (InP) PHEMT or Silicon Germanium (SiGe) processes [8], [37]. These technologies possess superior performance, compared to CMOS technology, due to characteristics such as higher carrier mobility, higher transistor breakdown voltage and lower process parasitics.

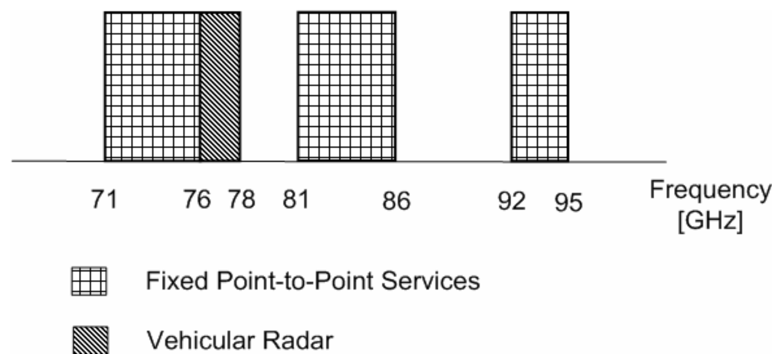

Figure 61 – The United States fixed point-to-point and radar band allocation in the 65 – 100 GHz spectrum 105[97]

Realizing these 75 – 95 GHz band MMIC devices on the CMOS process promises the integration of baseband signal processing, mixed signal and radio frequency (RF) components on a single die, with this integration resulting in significant cost benefits and the facilitation of a range of new lost-cost applications.

Recent advancements in CMOS technology have allowed the implementation of MMIC components on the CMOS process for frequencies up to 77 GHz [16], [83], [85], [94] [105] and CMOS oscillators at higher frequencies [28].

The power amplifier is an important but difficult to integrate component in building an integrated transceiver. Some of the difficulties encountered are due to the low breakdown voltage, low power density and operation at a significant portion of the transistors maximum oscillating frequency.

In this chapter, we present a two stage design and optimisation technique for high frequency PA design on CMOS. The methods outlined in this chapter were used to build the power amplifier using a 0.13-μm RF-CMOS process, provided by MOSIS and IBM.

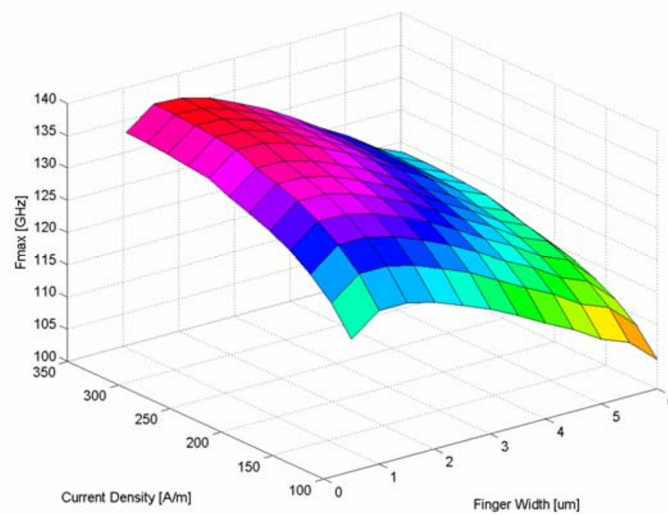

Figure 62 – Simulated f_{max} for varying device finger size and current density. Total device size was kept constant at 60 μm [97]

5.2 Transistor Design

An important parameter when designing high frequency amplification components is the transistors maximum oscillating frequency (f_{max}), defined as the frequency where the Mason's unilateral gain of the transistor becomes unity (U = 1). A transistors f_{max} is most significantly dependent on the channel length, width, number of fingers (which influences the gate resistance), biasing conditions and transistor parasitic resistances and capacitances. The dominant parasitic losses are due to the gate resistance, source resistance, drain resistance, channel resistance and the substrate resistance networks. It is common practice for CMOS circuits to be designed for operation at frequencies of less then one-fifth of the transistors peak f_{max}. At higher frequencies, especially those approaching the performance

limits of a process, these loss mechanisms must be carefully considered and optimised to increase f_{max}, thus increasing the frequency range operation of the designed components.

A critical step of the power amplifier design process is the design and optimisation of transistors for optimal performance. In this chapter, NMOS transistors are used as the active component building block. NMOS transistors have higher gain then a PMOS counterpart because of the higher mobility of electrons in silicon. As a consequence lower current densities are required, less power is dissipated and higher output power can be achieved.

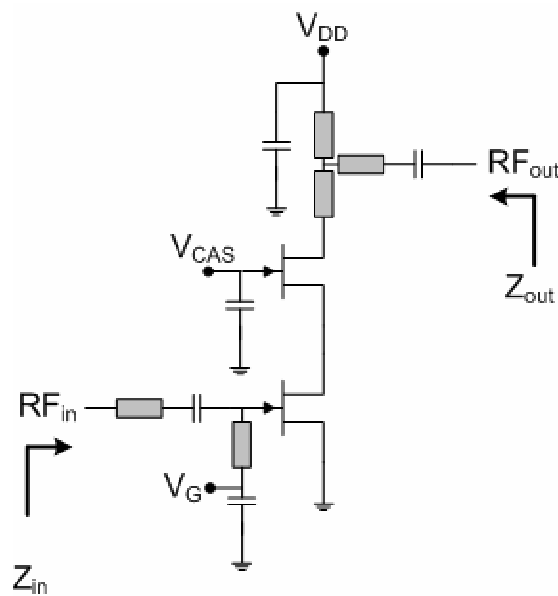

Figure 63 – Schematic of a single stage of the power amplifier [97]

The dimensions of the implemented NMOS devices in this chapter were chosen with the aid of CAD simulations and verified against multiple fabricated devices with varying lengths, widths and fingers. The f_{max} of the NMOS transistors increases as the finger width reduces from 8 μm to 2 μm due to a significantly reduced gate resistance. Below 1 μm the substrate resistance network becomes a significant factor and f_{max} begins to decrease, *Figure 62*. From our device simulations, a transistor with gate length of 0.12 μm, finger width of 2.5 μm (to increase source-drain current and allow ease of matching), and 32 fingers per device for a total device size of 80 μm was chosen. With these parameters the device possessed an f_{max} of greater than 135GHz at a biasing of 350 μA/μm of gate width.

At millimetre wave frequencies, the layout of a transistor can have a significant impact on the characteristics of the device due to the major effect the layout has on the parasitic elements especially gate resistances, metal layer inductances, losses in the substrate and capacitive coupling between transistor components. This requires each transistor to be implemented (laid out) carefully to minimise the parasitics in the gate (including connection of both gate contacts), source, drain, and substrate resistances (including minimising the resistance to ground of the substrate contact ring).

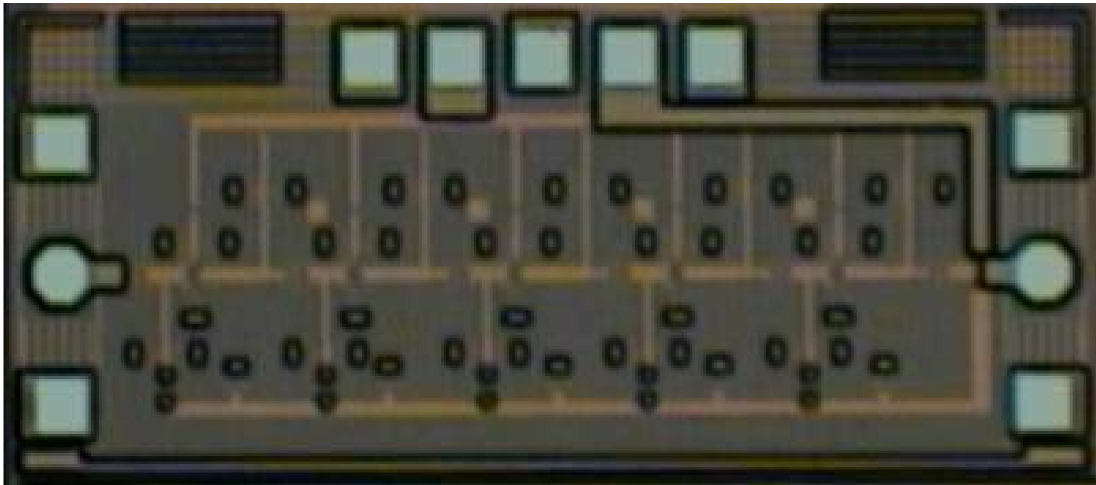

Figure 64 – Die micrograph of the 0.13μm CMOS 77-GHz PA with, dimensions 1230 μm by 520 μm [97]

5.3 Circuit Design

5.3.1 Architecture

The PA presented in this chapter, is a five-stage amplifier with each stage operating as a Class-A amplifier as shown in *Figure 63*, with the input, output and interstage matching networks all integrated onto one chip. A cascode topology was employed at each stage to increase the gain, reduce the Miller Capacitance, and to increase the stability of each stage. To allow the device to operate at 77 – 95 GHz strong biasing into the inversion region is required.

When biased with a current density of 350 μA/μm of gate width, each cascode pair possessed a simultaneously conjugate matched maximum gain (G_{MAX}) of 4 dB at 75 GHz and 3 dB at 95 GHz.

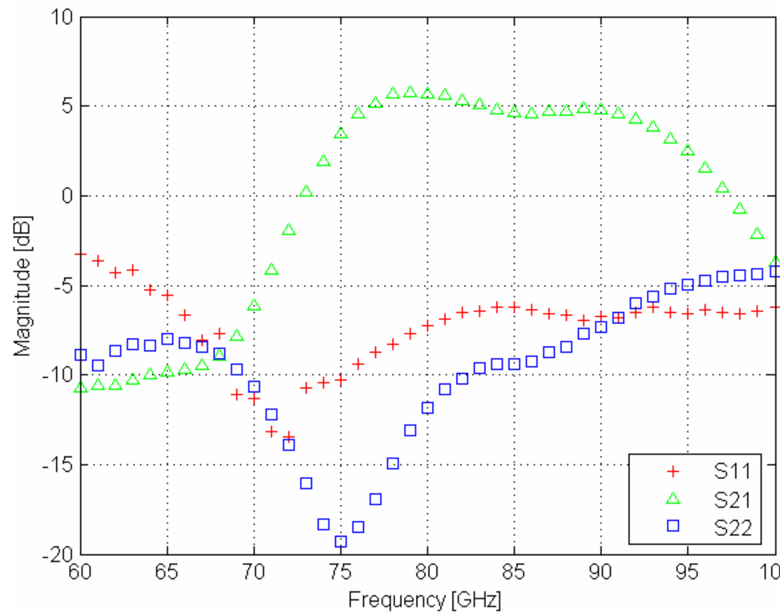

Figure 65 – Measured S-parameters of the PA [97]

5.3.2 Matching Networks

Such a limited G_{MAX} and the utilization of large devices with limited output impedances requires precise matching networks with losses in the passive components needed to be kept to a minimum to maintain adequate gain. Careful selection of metal layers and ground planes was required to build microstrip transmission lines which were used for the design of the impedance matching networks, interconnects and for biasing the common gate and common source devices. These transmission lines were optimized to increase bandwidth and minimize losses (both resistive and radiation losses due to discontinuities), and are significantly shorter than $\lambda/4$ (< 80 μm) to reduce the occurrence of transmission line effects. AC coupling has been used between each amplifier stage, as well as the input and output connections between the pads and the PA. This was accomplished by using a metal-insulator-metal (MIM) capacitor. The input and output of the PA were both designed to be matched to 50Ω.

5.4 Experimental Results

The S-parameter results of the power amplifier measured using a Suss-Microtech probe station with 110 GHz Ground-Signal-Ground (G-S-G) coplanar probes and a 110 GHz Anritsu Vector Network Analyser. Power measurements were performed using an Anritsu

power meter and a signal generator. The micrograph of the fabricated power amplifier is shown in *Figure 64*, and has dimensions 520 μm by 1230 μm.

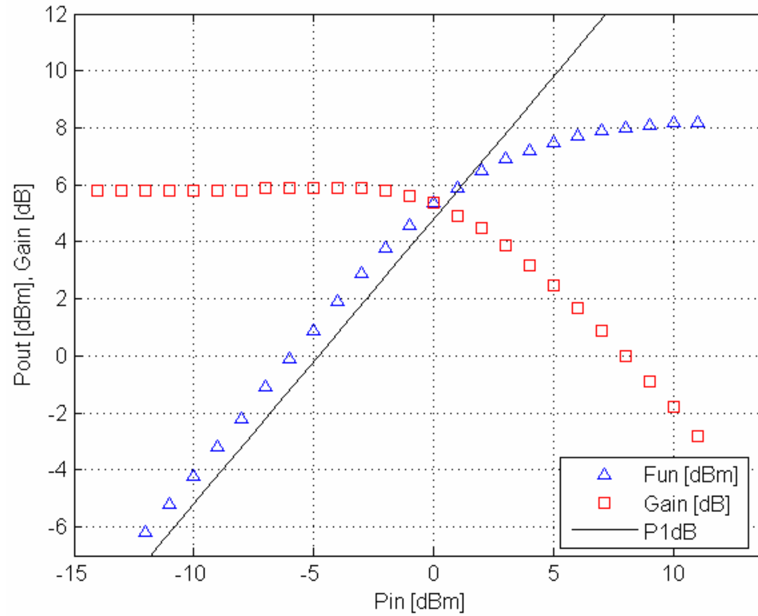

Figure 66 – Measured large-signal characteristics at 77 GHz [97]

At 77 GHz the power amplifier achieves a measured small signal gain of 6.0 dB, input and output return losses better then 9 and 15 dB respectively and a 3-dB bandwidth of 75 – 95 GHz as shown in Figure 65, whilst drawing 135 mA from a 2.5 V power supply. It demonstrated a saturated output power of 8.1 dBm, an output referred power at the 1-dB compression point of 6.3 dBm, shown in Figure 66, and maximum power added efficiency (PAE) of 0.5% at P_{1dB}.

The ITRS has defined a PA figure of merit (FoM_{PA}), which links the output power (P_{OUT}) with the Gain (G), PAE and frequency (*f*) as a standard to compare power amplifiers:

$$FoM_{PA} = P_{OUT} * G * PAE * f^2 \ [40] \qquad \textit{Equation 59}$$

Table III provides a comparison of this PA with other published millimeter-wave PAs in terms of the ITRS FoM_{PA}. To the best of the authors' knowledge, this power amplifier is the highest frequency CMOS PA reported and also the only CMOS PA reported for the 81 – 86 GHz and 91 – 95 GHz ISM bands.

PA Technology	f [GHz]	G [dB]	P_{sat} [dBm]	P_{1dB} [dBm]	PAE [%]	*FoM [6]*
84 GHz f_{max} 0.18-um CMOS [78]	40	7	10.4	-	2.9	2.6
130 GHz f_{max} 0.130-um [16]	60	12	-	2.0	-	-
200 GHz f_{max} 90nm CMOS [85]	60	5.2	9.3	6.4	7.4	7.5
200 GHz f_{max} 90-nm CMOS [94]	60	8	10.6	8.2	-	-
200 GHz f_{max} 90-nm CMOS [83]	77	9	6.3	4.7	-	-
130 GHz f_{max} 0.130-um [95]	60	13.5	7.8	7.0	3.0	15.2
130 GHz f_{max} 0.130-um (this work)	77	6	8.1	6.3	0.5	2.1

Table III – Comparison of the 75 – 95 GHz wideband CMOS power amplifier with published CMOS millimeter-wave PA results [97]

5.5 Conclusion

In this chapter, a wideband 75 – 95 GHz power amplifier was designed and implemented on 0.13 μm RF-CMOS to explore the feasibility of low-cost CMOS technology for use for 75 – 95 GHz point-to-point, and automotive radar band. The fully-integrated design implements the main and auxiliary amplifiers, matching networks, and input and output transmission line networks on-chip. The designed amplifier achieves small signal gain of 6.0 dB at 77 GHz, a 3-dB bandwidth of 75 – 95 GHz and delivers a saturated output power of 8.1 dBm at 77-GHz.

Chapter 6
A 60-GHz Fully-Integrated Doherty Power Amplifier

6.1 Introduction

The appeal of the 60-GHz channel for high-speed short distance wireless personal area networks (WPANs) and radar applications has motivated research into low cost, efficient and small form factor integrated millimeter-wave devices in order to facilitate their use in consumer electronic (CE) applications. This channel has a large allocated bandwidth around the 60 GHz region of the spectrum.

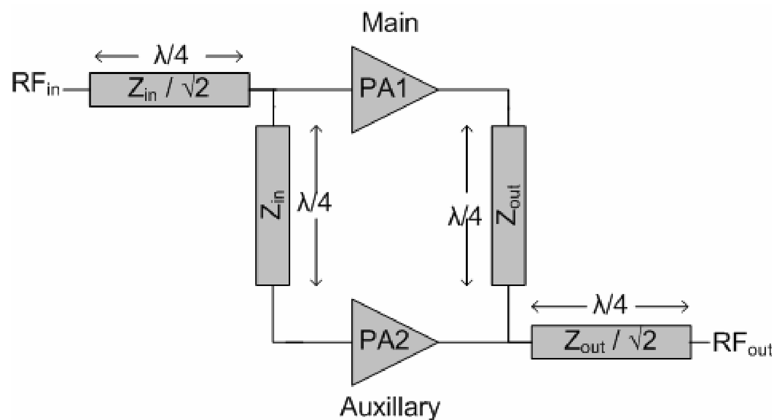

Figure 67 – Block diagram of the Doherty power amplifier configuration [95]

Traditionally, millimeter-wave radio transceivers have been implemented in type III-V semiconductor technologies, such as GaAs, InP, and SiGe but with the recent developments in CMOS technology an increasing number of CMOS based 60-GHz transceiver components have been reported [17], [78], [85], [104]. The use of CMOS technology for a 60-GHz transceiver is particularly attractive as it permits efficient and integrated digital, mixed signal and radio frequency (RF) components, on a single chip, system-on-chip (SOC). To realize this vision, the challenges involved with the power amplifier, an important but difficult to integrate component, must be overcome. These

difficulties include operating at a frequency that is a significant proportion of the transistor maximum frequency of oscillation and the low breakdown voltage of CMOS.

6.2 Architecture and Circuit Description

6.2.1 Power Amplifier Architecture

Many implementations of high data rate systems are based on orthogonal frequency-division multiplexing (OFDM), and the IEEE 802.15.3c task group is considering OFDM as the modulation scheme for personal area systems operating in the 57–64 GHz channel. OFDM signals are characterized by a high peak to average power ratio (PAPR) and require low distortion in order to minimize intercarrier interference. In order to contend with high PAPR a Doherty PA [21] is implemented in our design. The Doherty PA employs two amplifiers operating in different class, typically in class-A, class-B or class-AB, each contributing to the power output thus increasing the power range of the amplifier. This is a good choice for OFDM systems as it increases both the power added efficiency (PAE) at low power and also the fundamental 1-dB output compression (P_{1dB}) and saturation points (P_{SAT}).

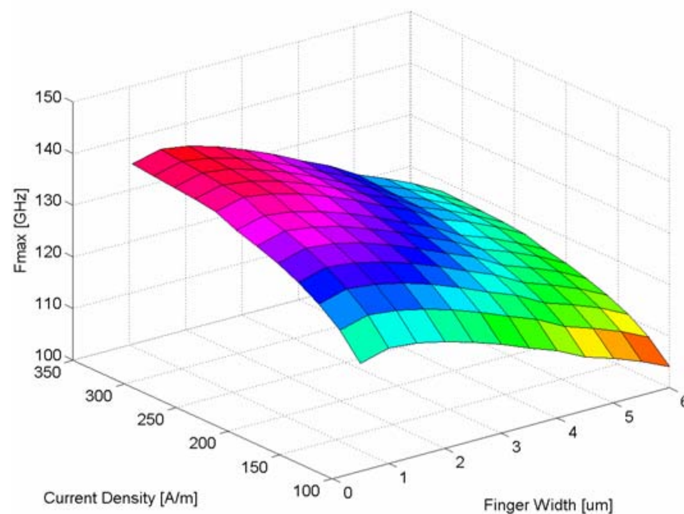

Figure 68 – Simulated f_{max} for varying device finger size and current density. Total device size was kept constant at 80 μm. [95]

Figure 67 shows the basic design of the implemented Doherty amplifier. It employs two amplifier cells, the main amplifier cell and the auxiliary amplifier cell. Both input and output networks were matched to 50 Ω. A quarter wavelength, λ/4, transmission line network is used to split the input signal between the two amplifiers and consists of a quarter wavelength transmission-line connecting the input to the main amplifier cell with characteristic impedance of Z_0 = 50 Ω, and a quarter wavelength transmission line with characteristic impedance of $Z_0 = (50 / \sqrt{2})$ Ω connecting the inputs of the main amplifier cell with the auxiliary amplifier cell. A second quarter wavelength transmission line network is used to combine the outputs of the two amplifiers, with the output transmission line connection used to compensate for the phase shift of the splitter. Therefore, adding the output currents in phase.

When both amplifiers are at their maximum output power each amplifier will see an equal load. These input and output transmission line networks significantly aid in achieving a low input and output return loss, respectively.

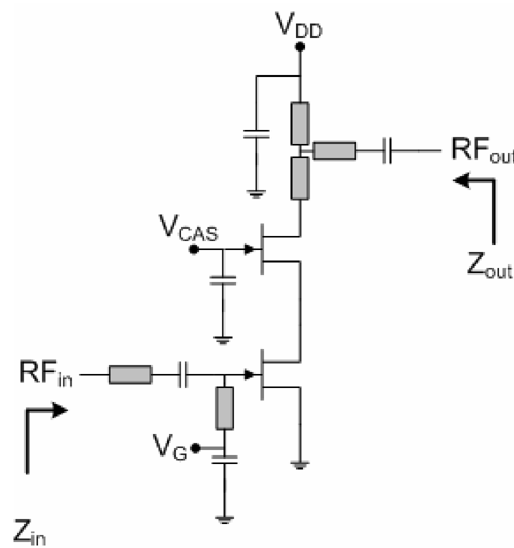

Figure 69 – Schematic of a single stage of both the main and auxilliary amplifiers [95]

6.2.2 Transistor Design

Transistor optimization is critical in the design of a millimeter power amplifier design on CMOS. NMOS transistors were employed throughout the design as they are able to achieve a higher gain at lower current densities then their PMOS counterparts. The

dimensions of the NFET transistors were optimized using CAD simulations using the maximum oscillating frequency (f_{max}) of a transistor, defined as the frequency where Mason's unilateral gain becomes unity, as our figure of merit (FoM). The transistors implemented in the process were most significantly influenced by the channel length, finger width, number of fingers and biasing conditions. *Figure 68* shows the simulated f_{max} of an active device for varying transistor finger sizes and current densities whilst keeping the gate length and total device size constant at 0.12 μm and 80 μm respectively. It can be seen that the f_{max} of the NFET transistor is a convex curve and achieves a peak of 135 GHz for a finger width of 1 μm at a bias of 350 μA/μm of gate width.

From these simulations a device with gate length 0.12μm, finger width of 2.5 μm (to increase source drain current and aid matching) and with 32 fingers per device for a total device size of 80 μm was chosen.

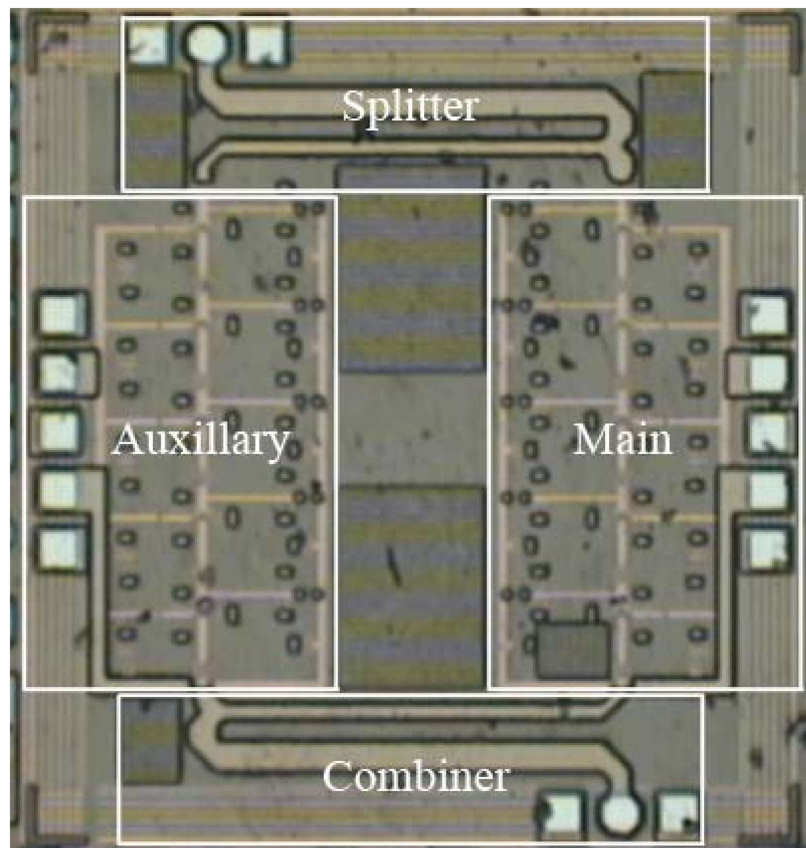

Figure 70 – Die micrograph of the 0.13μm CMOS Doherty PA with main, auxiliary amplifiers and splitters labelled [95]

Each NFET transistor device was carefully implemented to minimize the parasitics particularly in the gate, source, drain, and substrate resistances as the layout of a transistor can have a significant impact on the characteristics of the device at millimeter-wave frequencies (especially gate resistances, metal layer inductances, losses in the substrate and capacitive coupling between transistor components).

The topology of each of the amplifier cells consists of five cascode stages. The cascade cell building block, shown in *Figure 69*, was used to increase gain of the PA by reducing the Miller capacitance and also to improve amplifier stability. Care was taken during design and layout to ensure the supply rail, V_{DD}, and gate biasing rails, V_{CAS} and V_G, were sufficiently decoupled to prevent instability and as a result the cascode pairs were unconditionally stable above 25 GHz. The cascode inter-stage input and output matching networks were both matched to 50 Ω. When biased at 200 μA/μm of gate width each cascode pair possessed a simultaneously conjugate matched maximum gain (G_{MAX}) of 7 dB at 60 GHz and an f_{max} of greater then 115 GHz.

6.2.3 Matching Networks

Microstrip transmission lines were used for impedance matching, interconnects and for biasing the active devices. These lines required careful selection of both the signal layer and the ground plane in order to minimize power loss (both resistive and radiation losses) and are kept significantly shorter than a quarter-wavelength in order to reduce transmission line effects. A metal-insulator-metal (MIM) capacitor was used to AC couple between each amplifier stage as well as at the input and output connection between the pads and the PA. The insertion losses achieved for the inter-stage matching networks were 1.9 dB, the input matching network was 1.4 dB and output matching networks was 1.8 dB. These were all kept as low as possible to increase the power gain and the output power. The design was fabricated on a 0.13-μm bulk CMOS process. A micrograph of the fabricated power amplifier is shown in *Figure 70*, and has dimensions of 1310 μm by 1410 μm.

6.3 Experimental Results

The fully-integrated Doherty CMOS PA was measured with using a Suss-Microtech probe station with 110 GHz Ground-Signal-Ground (G-S-G) coplanar probes and a 110 GHz Anritsu Vector Network Analyzer. This PA operates from a 1.6-V supply with the main

amplifier cell biased in the "Class A" region and the output power of the auxiliary cell was optimized by adjusting the gate bias of the common sources devices. Employing this technique the gain compression of the main amplifier cell is compensated by the gain expansion of the auxiliary amplifier cell both maximizing the P1dB, P_{SAT} (*Figure 71*) and the efficiency (*Figure 72*) of the PA. *Figure 72* also describes the uneven input DC power feeding of the main cell and auxiliary cells. The measured S-Parameters for the power amplifier are shown in *Figure 73*.

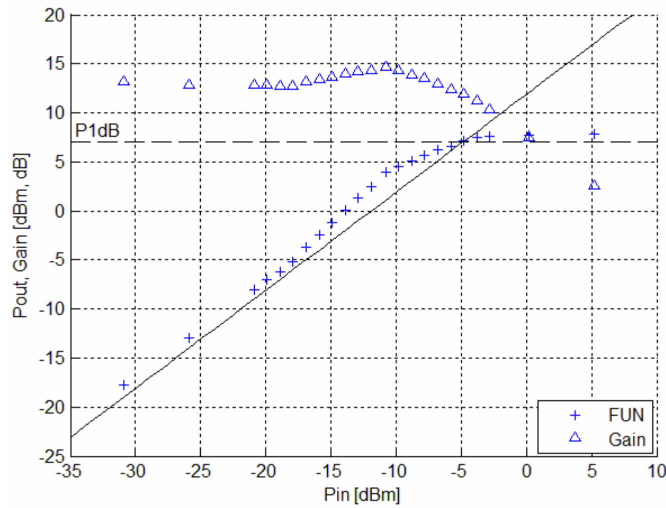

Figure 71 – Measured RF performance of the Doherty PA at 60 GHz [95]

At the output referred 1-dB compression point the amplifier delivers +7.0 dBm with a peak small signal power gain of 13.5 dB, with a 3-dB bandwidth of 6.7 GHz from 55.5 GHz to 62.2 GHz, input power return loss greater than 10 dB, output power return loss greater than 10 dB and reverse isolation of greater than 35 dB and a power added efficiency (PAE) of 3.0%.

The ITRS has defined a PA figure of merit (FoM_{PA}), which links the output power (P_{OUT}) with the Gain (G), PAE and frequency (f) as a standard to compare power amplifiers. Table IV provides a comparison of this PA with other published millimeter-wave PAs in terms of this figure of merit.

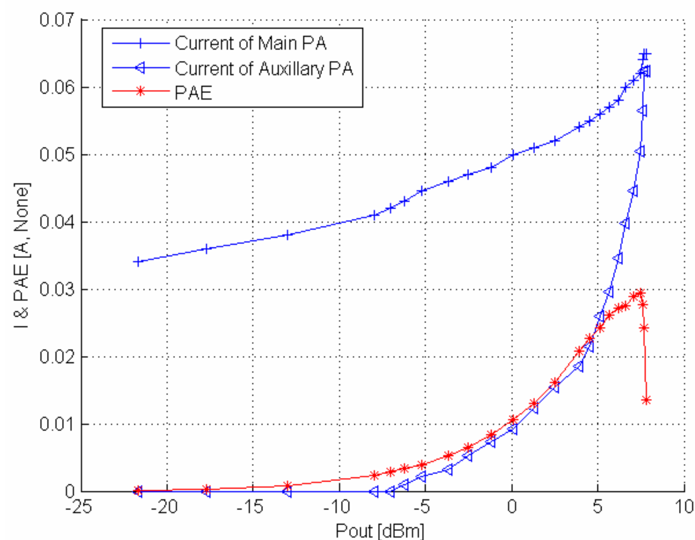

Figure 72 – Measured currents for both the main and auxiliary amplifiers and efficiency of the Doherty PA [95]

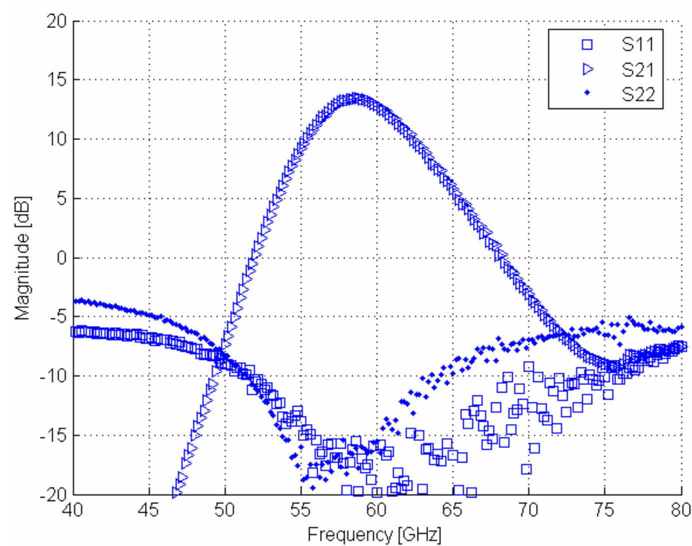

Figure 73 – Measured S-parameters of the Doherty PA [95]

6.4 Conclusion

In this chapter, a 60-GHz Doherty power amplifier was designed and implemented on 0.13 μm RF-CMOS for use in an integrated 60-GHz transceiver. The fully-integrated design implements the main and auxiliary amplifiers, matching networks, and input and output transmission line networks on-chip. The prototype operating from a 1.6-V supply exhibits

an output referred P1dB of 7.0 dB, a P_{SAT} of +7.8 dBm, with peak power gain of 13.5 dB, a 3-dB bandwidth of 6.7 GHz, and 3.0 % PAE. The die area is 1.8mm^2.

PA Technology	f [GHz]	G [dB]	P_{sat} [dBm]	P_{1dB} [dBm]	PAE [%]	*FoM [6]*
84 GHz f_{max} 0.18-um CMOS [78]	40	7	10.4	-	2.9	2.6
130 GHz f_{max} 0.130-um [16]	60	12	-	2.0	-	-
200 GHz f_{max} 90nm CMOS [85]	60	5.2	9.3	6.4	7.4	7.5
200 GHz f_{max} 90-nm CMOS [94]	60	8	10.6	8.2	-	-
200 GHz f_{max} 90-nm CMOS [83]	77	9	6.3	4.7	-	-
130 GHz f_{max} 0.130-um [97]	77	6	8.1	6.3	0.5	2.1
130 GHz f_{max} 0.130-um (this work)	60	13.5	7.8	7.0	3.0	15.2

Table IV – Comparison of the Doherty PA with published CMOS millimeter-wave PA results [95]

Chapter 7
Conclusion

7.1 Thesis Conclusion

Developing CMOS for use in the millimeter-wave spectrum has the promise to facilitate low cost, power efficient, high data rate and highly integrated transceivers. This promise would allow for wireless personal area network applications such as wireless communication of your favourite TV shows, latest movies, and the footy wirelessly within seconds, and automotive radar applications allowing your automobile to navigate without your control, to safely, efficiently drive you home, eliminating the possibility of an accident. This thesis has focussed on the theory and design techniques to implement CMOS millimetre-wave power amplifiers, an enabler of this vision.

Full integration of an entire system on chip remains a challenge for millimetre wave transceivers due to the difficulties integrating the power amplifier. This is due to several causes: the reduction in supply voltage with the scaling of CMOS technology; the limited power gain of the active devices at millimetre-wave frequencies; and the high parasitic losses of the submicron CMOS process. This thesis develops the theory and design techniques and employs these to implement CMOS millimeter-wave power amplifiers facilitating the development of these low cost, power efficient, high data rate and highly integrated transceivers.

The thesis has explored the potential for single chip CMOS millimeter-wave transceivers for automotive radar applications. A CMOS millimeter-wave integrated circuit (MMIC) power amplifier (PA) designed and implemented for automotive radar applications with the purpose of system-on-chip integration with the rest of the electronics.

The feasibility of the use of CMOS technology for use in 71 – 76 GHz, 81 – 86 GHz and 92 – 95 GHz Industrial, Scientific and Medical (ISM) bands and the 77-GHz vehicular

radar band is explored in chapter five. With a 75 – 95 GHz wideband power amplifier (PA) in 0.13-μm CMOS implemented.

A fully integrated millimetre wave CMOS power amplifier employing the Doherty technique is implemented allowing transmission of high power with improved average efficiency. This device demonstrates; fully integrated CMOS millimetre-wave amplifiers are feasible and will continue to be feasible as the technology scales; the Doherty technique is applicable to millimetre wave amplifiers allowing for improved efficiency especially the active load pull advantages; the high level of linearity required for millimetre wave devices such as high data rate transceivers and imaging can be achieved with CMOS in the millimetre wave spectrum; that the issues of limited power generation and amplification at millimeter wave frequencies can be overcome.

7.2 Future Work

Potential topics of study arising from this work are numerous. Power amplifier engineers are always searching for techniques to create more linear and more efficient designs. Future work possible for the millimeter wave amplifiers designed and implemented is addressed below.

Foremost, the process used for implementation of the amplifier can also be re-evaluated especially due to the dynamics of fabrication process' cost and availability that have occurred in the years since the this work began. New processes have been developed and come online, availability of processes have shifted and costs have reduced which may have altered the fundamental assumptions of what process technology for implementation may have altered.

Efficiency is one of the most critical power amplifier metrics. Power amplifiers with poor efficiency require large power wastage, which almost exclusively gets converted to heat, and thus requires the die to have a cooling solution. Efficiency can be calculated instantaneously or by an average and both these issues need to be addressed. Efficiency techniques such as Kahn envelope tracking, nonlinear amplification, distributed amplification and power combining may be implemented to increase the amplifiers efficiency.

Linearity is a highly desired feature of power amplifiers. Many radio frequency systems are based complex modulation schemes characterized by a high peak to average power ratio (PAPR) and require low distortion to preserve the integrity of the signal and to minimize intercarrier interference. High AM-AM and AM-PM linearity preserves both the integrity of the signal and allows recovery at the receiver. Linearity boosting techniques such as Wilkinson, totem-pole and stacked transistor topologies as well as transformer based power combining techniques may be implemented to increase the amplifiers linearity.

Bibliography

[1] I. Aoki, S. Kee, D. B. Rutledge and A. Hajimiri, “Fully integrated CMOS power amplifier design using the Distributive Active-Transformer architecture,” IEEE J. Solid-State Circuits, vol. 37, no. 3, pp. 371-383, March, 2002.

[2] I. Aoki, S.D. Kee, D. Rutledge, A. Hajimiri, "A 2.4-GHz, 2.2-W, 2-V fully-integrated CMOS circular-geometry active-transformer power amplifier," Proceedings of CICC, pp. 57-60, May 2001.

[3] D. Alldred, B. Cousins, and S. P. Voinigescu, “A 1.2 V, 60 GHz radio receiver with on-chip transformers and inductors in 90 nm CMOS,” in Proc. IEEE Compound Semiconductor Integrated Circuits Symp., Nov. 2006, pp. 51–54.

[4] C.R. Battjes, “A wide-band high-voltage monolithic amplifier,” IEEE J. Solid-State Circuits, vol. sc-8, no. 6, pp. 408-413, December, 1973.

[5] L. Besser, R. Gilmore, “Practical RF Circuit Design for Modern Wireless Systems,” Artech House.

[6] Y. Bo, E. Skafidas, R.J. Evans, “Empirical Study of The Q- Factor of Integrated Square Spiral Inductors on Silicon on Sapphire,” WSEAS Transactions on Circuits and Systems, Issue 5, Vol 5, pp 697-704, May 2006.

[7] T. Chalvatzis, K. H. K. Yau, P. Schvan, M. T. Yang, and S. P. Voinigescu, “A 40-Gb/s decision circuit in 90-nm CMOS,” in Proc. ESSCIRC, Sep. 2006, pp. 512–515.

[8] H.-Y. Chang, H. Wang, M. Yu, and Y. Shu, “A 77-GHz MMIC Power Amplifier for Automotive Radar applications,” IEEE Microwave Wireless Compon. Lett., vol. 13, no. 4, pp. 143-145, Apr. 2003.

[9] R. E. Collin, “Foundations for Microwave Engineering,” Second Edition, IEEE Press, N.Y. 2001.

[10] S. C. Cripps, “RF Power Amplifiers for Wireless Communications,” 2nd ed. Boston, MA: Artech House, 2006.

[11] S. C. Cripps, “Intercept Point Deception,” IEEE Microwave Mag., Feb., 2007.

[12] T. O. Dickson, R. Beerkens, and S. P. Voinigescu, “A 2.5-V 45-Gb/s decision circuit using SiGe BiCMOS logic,” IEEE J. Solid-State Circuits, vol. 40, no. 4, pp. 994–1003, Apr. 2005.

[13] T. O. Dickson, M. LaCroix, S. Boret, D. Gloria, R. Beerkens, and S. P. Voinigescu, “30–100 GHz inductors and transformers for millimeter- wave (Bi)CMOS integrated circuits,” IEEE Trans. Microw. Theory Tech., vol. 53, no. 1, pp. 123–133, Jan. 2005.

[14] T. O. Dickson, K. H. K. Yau, T. Chalvatzis, A. M. Mangan, E. Laskin,R. Beerkens, P. Westergaard, M. Tazlauanu, M.-T. Yang, and S. P.Voinigescu, “The invariance of characteristic current densities in nanoscale MOSFETs and its impact on algorithmic design methodologies and design porting of Si(Ge) (Bi)CMOS high-speed building blocks,” IEEE J. Solid-State Circuits, vol. 41, no. 8, pp. 1830–1845, Aug. 2006.

[15] C. H. Doan, S. Emami, A.M. Niknejad, R.W. Brodersen, "A 60GHz CMOS Front-End Receiver," ISSCC Digest of Tech. Papers, 2007, pp. 190-191.

[16] C. H. Doan, S. Emami, A. M. Niknejad, and R. W. Brodersen, "A 60-GHz down-converting CMOS single-gate mixer," RFIC Digest of Tech. Papers, 2005, pp.163-166.

[17] C. H. Doan, S. Emami, A. M. Niknejad, and R. W. Brodersen, "Design of CMOS for 60GHz applications," ISSCC Digest of Technical Papers, 2004, pp. 440-538.

[18] C. H. Doan, S. Emami, A. M. Niknejad, and R. W. Brodersen “Millimeter-Wave CMOS Design,” IEEE J. Solid-State Circuits, vol. 40, No 1, pp.144 – 155 Jan 2005.

[19] C. H. Doan, S. Emami, D. Sobel, A. M. Niknejad, and R. W. Brodersen, "60 GHz CMOS radio for Gb/s wireless LAN," in IEEE RFIC Symp. Dig., June 2004, pp. 225-228.

[20] C. H. Doan, S. Emami, D. A. Sobel, A. M. Niknejad, and R. W. Brodersen, "Design considerations for 60 GHz CMOS radios," IEEE Commun. Mag., vol. 42, pp. 132-140, Dec. 2004.

[21] W. Doherty, "A new high efficiency power amplifier for modulated waves," Proc. IRE, vol. 24, pp. 1163-1182, Sep. 1936.

[22] M. Elmala, R. Bishop, "A 90nm CMOS Doherty Power Amplifier with Integrated Hybrid Coupler and Impedance Transformer" RFIC Symposium, 2007 IEEE, pp. 423 – 4263, 5 June 2007.

[23] S. Emami, C. H. Doan, A. M. Niknejad, and R. W. Brodersen, "Large-signal millimeter-wave CMOS modeling with BSIM3," in IEEE RFIC Symp. Dig., Jun. 2004, pp. 163–166.

[24] C. Enz, "An MOS transistor model for RF IC design valid in all regions of operation," IEEE Trans. Microw. Theory Tech., vol. 50, no. 1, pp. 342–359, Jan. 2002.

[25] Federal Communication Commission, "Code of Federal Regulations," [Online]. Available: www.fcc.gov/.

[26] B. Floyd, S. Reynolds, U. Pfeiffer, T. Beukema, J. Grzyb, and C. Haymes, "A silicon 60 GHz receiver and transmitter chipset for broadband communications," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2006, pp. 649–658.

[27] B. A. Floyd, S. K. Reynolds, U. R. Pfeiffer, T. Zwick, T. Beukema, and B. Gaucher, "SiGe bipolar transceiver circuits operating at 60 GHz," IEEE J. Solid-State Circuits, vol. 40, no. 1, pp. 156–157, Jan. 2005.

[28] L. M. Franca-Neto, R. E. Bishop, and B. A. Bloechel, "64 GHz and 100 GHz VCO's in 90 nm CMOS using optimum pumping method," in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, Feb. 2004, pp. 444–445.

[29] L. M. Franca-Neto, B. A. Bloechel, and K. Soumyanath, "17 GHz and 24 GHz LNA designs based on extended-S-parameter with microstrip-on-die in 0.18-μm logic CMOS technology," in Proc. Eur. Solid-State Circuits Conf., Sep. 2003, pp. 149–152.

[30] H. T. Friis, "Noise Figures in Radio Recievers," Proc. Of IRE, July 1944.

[31] G. Gonzalez, "Microwave Transistor Analysis," Second Edition, Prentice Hall, 1996.

[32] M. Gordon and S. P. Voinigescu, "An inductor-based 52-GHz, 0.18 _m SiGe BiCMOS cascode LNA with 22 dB gain," in Proc. ESSCIRC, Sep. 2004, pp. 287–291.

[33] M. Q. Gordon, T. Yao, and S. P. Voinigescu, "65-GHz receiver in SiGe BiCMOS using monolithic inductors and transformers," in Si Monolithic Integrated Circuits in RF Systems, Tech. Dig., Jan. 2006, pp. 265–268.

[34] P. R. Gray, P. J. Hurst, S. H. Lewis, R. G. Meyer, "Analysis and Design of Analog Integrated Circuits," 4th Edition, John Wiley & Sons, Inc., 2001.

[35] B. Heydari, M. Bohsali, E. Adabi, A. M. Niknejad, "Low-Power mm-Wave Components up to 104GHz in 90nm CMOS," ISSCC Digest of Technical Tech. Papers, 2007, pp. 200-201, 597.

[36] M. A. Hogan, "Short Range Radar Enabled Automotive Safety Systems," Proceedings of IWPC – International Wireless Industry Consortium, Washington D.C, Sept 19-21, 2006.

[37] P. P. Huang, T.-W. Huang, H. Wang, E. W. Lin, Y. Shu, S. D. Gee, R. Lai, H. M. Biedenbender, and J. H. Elliott, "A 94-GHz 0.35-W power amplifier module," IEEE Trans. Microwave Theory Tech., vol. 45, pp. 2418–2423, Dec. 1997.

[38] IBM CMRF8SF Reference Guide.

[39] IBM CMOS8RF Design Manual.

[40] International Technology Roadmap for Semiconductors (ITRS). [Online]. Available: http://public.itrs.net.

[41] E. O. Johnson, "Physical limitations on frequency and power parameters of transistors," IEEE Intl. Conv. Record, p. 27, 1965.

[42] J. Kang, D. Yu, K. Min, B. Kim, "A Ultra-High PAE Doherty Amplifier Based on 0.13-um CMOS Process," Microwave and Wireless Components Letters, IEEE, Volume: 16 , Issue: 9, pp. 505 – 507, Sept. 2006.

[43] S. D. Kee, I. Aoki, A. Hajimiri, D. B. Rutledge, "The class-E/F family of ZVS switching amplifiers," IEEE Trans. Microwave Theory Tech., vol. 51, no. 6, pp. 1677-1690, June 2003.

[44] P. B. Kenington, "High linearity RF amplifier design," Artech House Inc, 2000.

[45] W. S. Kim, X. Li, and M. Ismail, "A 2.4 GHz CMOS low noise amplifier using an inter-stage matching inductor," in Proc. 42nd Midwest Symp. Circuits and Systems, Aug. 1999, vol. 2, pp. 1040–1043.

[46] A. Komijani and A. Hajimiri, "A 24 GHz, +14.5 dBm fully-integrated power amplifier in 0.18 _m CMOS," in Proc. Custom Integrated Circuits Conf. (CICC), Oct. 2004, pp. 561–564.

[47] A. Komijani and A. Hajimiri, "A wideband 77 GHz, 17.5 dBm power amplifier in silicon," in Proc. Custom Integrated Circuits Conf. (CICC), Sep. 2005, pp. 571–574.

[48] M. C. A. M. Koolen, J. A. M Geelen, M. P. J. G. Versleijen, "An Improved De-Embedding Technique for On-Wafer Characterization," IEEE Bipolar Circuits and Technology Meeting, 1991.

[49] E. Laskin, S. T. Nicolson, P. Chevalier, A. Chantre, B. Sautreuil, and S. P. Voinigescu, "Low-power, low-phase noise SiGe HBT static frequency divider topologies up to 100 GHz," in Proc. IEEE Bipolar/BiCMOS Circuits Technology Meeting, Oct. 2006, pp. 235–238.

[50] T. H. Lee, "The design of CMOS radio-frequency integrated circuits," 1st Edition, Cambridge University Press, 1998.

[51] K. Lim, S. Pinel, M. Davis, A. Suntono, C-H Lee, D. Heo, A. Obatoynbo, J. Laskar, M. Tantzeris, and R. Tummala, "RF-SOP for wireless communications," IEEE Microwave Magazine, vol. 3, no. 1, pp.88-99, Mar. 2002.

[52] G. Liu, T-J. King, A. M. Niknejad, "A 1.2V, 2.4GHz Fully Integrated Linear CMOS Power Amplifier with Efficiency Enhancement," Proceeding of CICC, 2006, pp.141-144.

[53] Z. Liu, "Millimeter Wave CMOS VCO and PLL Design and Phase Noise Mitigation Techniques," May, 2008, submitted.

[54] Z. Liu, E. Skafidas, R.J Evans, " A Small Signal Model and Extraction Procedure for RF SoS MOSFETs operating at millimeter Wavelengths," WSEAS Transactions on Circuits and Systems, Issue 2, Vol 5, pp 196-202, Feb 2006.

[55] C.-M. Lo, C.-S. Lin, H. Wang, "A Miniature V-band 3-Stage Cascode LNA in 0.13nm CMOS," ISSCC Dig. Tech. Papers, pp. 322-323, Feb. 2006.

[56] A. Mangan, S. P. Voinigescu, M.-T. Yang, and M. Tazlauanu, "Deembedding TLMs for accurate modeling of IC designs," IEEE Trans. Electron Devices, vol. 53, no. 2, pp. 235–241, Feb. 2006.

[57] J. G. McRory, G. G. Rabjohn, R. H. Johnston, "Transformer coupled stacked FET power amplifiers," IEEE J. Solid-State Circuits, vol. 34, no. 2, pp. 157-161, February, 1999.

[58] S. T. Nicolson, K. K. W. Tang, K. H. K. Yau, P. Chevalier, B. Sautreuil, and S. P. Voinigescu, "A 2.5 V 77 GHz automotive radar chipset," in Proc. IEEE MTT-S Int. Microwave Symp., Honolulu, HI, Jun. 2007.

[59] S. T. Nicolson and S. P. Voinigescu, "Methodology for simultaneous noise and impedance matching in W-band LNAs," in Proc. IEEE Compound Semiconductor Integrated Circuits Symp., Nov. 2006, pp. 279–282.

[60] A. Niknejad, ASITIC. Univ. California at Berkeley, 2002 [Online]. Available: http://rfic.eecs.berkeley.edu/~niknejad/asitic.html.

[61] A. M. Niknejad, "Electromagnetics for High-Speed Communication Circuits," available online.

[62] A. M. Niknejad, Hossein Hashimi, "mm-Wave Silicon Technology," Springer, 2008.

[63] U. Pfeiffer, "A 20 dBm fully-integrated 60 GHz SiGe power amplifier with automatic level control," in Proc. ESSCIRC, Sep. 2006, pp. 356–359.

[64] U. R. Pfeiffer, S. K. Reynolds, and B. A. Floyd, "A 77 GHz SiGe power amplifier for potential applications in automotive radar systems," in Radio Frequency Integrated Circuits (RFIC) Symp. Dig., Jun. 2004, pp. 91–94.

[65] D. M. Pozar, "Microwave Engineering," Third Edition, John Wiley & Sons, Inc 2005.

[66] F.H. Raab, "The class BD high-efficiency RF power amplifier," IEEE J. Solid-State Circuits, vol. sc-12, no. 3, pp. 291-298, June 1977.

[67] F. H. Raab, P. Asbeck, S. Cripps, P.B. Kenington, Z.B. Popovic, N. Pothecary, J.F. Sevic, and N.O. Sokal, "Power Amplifiers and Transmitters for RF and Microwave," IEEE Transactions on MTT, vol. 50, no.3, pp. 814-826, March 2002.

[68] F. H. Raab, P. Asbeck, S. Cripps, P.B. Kenington, Z.B. Popovic, N. Pothecary, J.F. Sevic, and N.O. Sokal, "RF and Microwave Power Amplifiers and Transmitter Technology," Part 1-5, High Frequency Electronics, 2003-2004.

[69] B. Razavi, "A 60-GHz CMOS receiver front-end," IEEE J. Solid-State Circuits, vol. 41, no. 1, pp.17-22, January, 2006.

[70] B. Razavi, "A 60-GHz direct-conversion CMOS receiver," in IEEE Int.Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2005, pp.400–401.

[71] B. Razavi, "A mm-Wave CMOS Heterodyne Receiver with On-Chip LO and Divider," ISSCC Dig. Tech. Papers, 2007, pp. 188-189.

[72] B. Razavi, "Design of Analogue CMOS Integrated Circuits," McGraw-Hill, 2001.

[73] E. F. Sartori, "Hybrid Transformers," IEEE Trans. on Parts, Materials, and Packaging, PMP-4, pp.59-66, September, 1968.

[74] A. S. Sedra and K.C. Smith, "Microelectronic Circuits," Fifth Edition, Oxford University Press, 2004.

[75] S. Seki, H. Hasegawa, "Cross-tie slow-wave coplanar waveguide on semi-insulating GaAs substrates," IEEE Elec. Lett., vol. 17, no. 25, pp. 940-941, December, 1981.

[76] Semiconductor International Capacity Statistics (SICAS). [Online]. Available: http://www.sicas.info.

[77] Semiconductor Industry Association (SIA). [Online]. Available: www.sia-online.org/.

[78] H. Shigematsu, T. Hirose, F. Brewer, and M. Rodwell, "Millimeterwave CMOS circuit design," IEEE Trans. Microw. Theory Tech., vol. 53, no. 2, pp. 472–477, Feb. 2005.

[79] E. Skafidas, "Millimeter Wavelength Communication Systems," 2004.

[80] T. Sowlati, D.M.W. Leenaerts, “A 2.4-GHz 0.18-μm CMOS self-biased cascode power amplifier,” IEEE J. Solid-State Circuits, vol. 38, no. 8, pp. 1318-1324, August, 2003.

[81] M. B. Steer, “Comparison of the Gain and Frequency Performance of State-of-the-Art MESFET, MODFET and PBT mm-Wave Transistors,” IEEE Electron Device Letters, Vol. EDL-7, November 1986, pp 640 – 642.

[82] K. M. Strohm, R. Schneider, J. Wenger, “KOKON: A Joint Project for the Development of 79GHz Automotive Radar Sensors,” pp 97-101, Proceedings of the International Radar Symposium, Berlin 2005.

[83] T. Suzuki, Y. Kawano, M. Sato, T Hirose, K Joshin, “60 and 77GHz Power Amplifiers in Standard CMOS,” IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, Feb. 2008, pp. 562-563.

[84] T. Suzuki, Y. Nakasha, T. Takahashi, K. Makiyama, K. Imanishi, T. Hirose, and Y. Watanabe, “A 90 Gb/s 2:1 multiplexer IC in InP-based HEMT technology,” in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2002, pp. 192–193.

[85] C. M. Ta, B. Wicks, F. Zhang, B. Yang, Y. Mo, K. Wang, Z. Liu, G. Felic, P. Nadagouda, T. Walsh, R. J. Evans, I. Mareels and E. Skafidas, "Issues in the Implementation of a 60GHz Transceiver on CMOS," The 2nd IEEE International Workshop on Radio-Frequency Integration Technology, Singapore, 09-11 Dec., 2007.

[86] K.-C. Tsai, P. R. Gray, "A 1.9-GHz, 1-W CMOS class-E power amplifier for wireless communications," IEEE Journal of Solid-State Circuits, vol. 34, July 1999, pp. 962-970.

[87] G. D. Vendelin, Anthony M. Pavio, Ulrich L. Rohde, “Microwave Circuit Design Using Linear and Nonlinear Techniques,” Second Edition, Wiley-Interscience, June, 2005.

[88] S. P. Voinigescu, T. O. Dickson, M. Gordon, C. Lee, T. Yao, A. Mangan, K. Tang, and K. H. K. Yau, “RF and millimeter-wave IC design in the nano-(Bi)CMOS era,” in Si-Based Semiconductor Components for Radio-Frequency Integrated Circuits (RFIC), 2006, W. Z. Cai, Ed. New Delhi, India: Transworld Research Network.

[89] C. H. Wang, Y. H. Cho, C. S. Lin, H. Wang, C. H. Chen, D. C. Niu, J. Yeh, C. Y. Lee, and J. Chern, “A 60 GHz transmitter with integrated antenna in 0.18 _m SiGe BiCMOS technology,” IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2006, pp. 186–187.

[90] C. Wang, M. Vaidyanathan, L.E. Larson, “A capacitance-compensation technique for improved linearity in CMOS class-AB power amplifiers,” IEEE J. Solid-State Circuits, vol. 39, no. 11, pp. 1927-1937, November 2004.

[91] A. Werthof, H. J. Siweris; H. Tischer, W. Liebl, G. Jaeger, T. Grave, “A 38/76 GHz automotive radar chip set fabricated by a low cost PHEMT technology, Volume 3, pp1855–1858, June 2002.

[92] N. Weste and D. Harris, “CMOS VLSI Design,” Boston, MA: Addison-Wesley, 2005.

[93] B. Wicks, R. J. Evans, and E. Skafidas, "Issues in the Implementation of a 60GHz Power Amplifier based on a 0.13-um CMOS Process for use in a WPAN integrated Transceiver," IEEE Power Amplifier Symposium, Orlando, USA, 21-22 Jan., 2008.

[94] B. Wicks, E. Skafidas, I Mareels, R Evans, “A 46.7-46.9-GHz CMOS MMIC Power Amplifier for Automotive Radar Applications,” IASTED Antennas, Radar and Wave Propagation (ARP 2008), 30 May–1 June 2007, pp 80 - 84.

[95] B. Wicks, E. Skafidas, R. Evans, “A 60-GHz Fully-Integrated Doherty Power Amplifier Based on 0.13-μm CMOS,” IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, June, 2008.

[96] B. N. Wicks, C. M. Ta, E. Skafidas, R. J. Evans, and I. Mareels, "A 60-GHz Power Amplifier and Transmit/Receive Switch for Integrated CMOS Wireless Transceivers," The 2008 International Conference on Microwave and Millimeter Wave Technology (ICMMT 2008), Nanjing, P. R. China, April 21-24, 2008.

[97] B. N. Wicks, E. Skafidas, R. J. Evans, and I. Mareels, “A 75 – 95 GHz Wideband CMOS Power Amplifier,” The European Microwave Integrated Circuits Conference 2008, Amsterdam, 27-28 October 2008.

[98] B. N. Wicks, C. M. Ta, E. Skafidas, I. Mareels, and R. J. Evans, "A Transmit/Receive Switch and Power Amplifier on 130-nm CMOS for 60-GHz Wireless Transceiver," Melbourne Engineering Research Institute (MERIT), Melbourne, Australia, Nov. 22, 2007.

[99] E. Wilkinson, “An N-way hybrid power divider,” IRE Trans. on Microwave Theory and Techniques, vol. MTT-8, pp. 116-118, January, 1960.

[100] N. Wongkomet, L. Tee and P. Gray, “A 1.7GHz 1.5W CMOS RF Doherty Power Amplifier for Wireless Communications,” IEEE ISSCC Digest of Technical Papers, pp. 486-487, February 2006.

[101] B. Yang, Y. Mo, K. Wang, Y. Feng, B. Wicks, C. Ta-Minh, F. Zhang, Z. Liu, C. Liu, G. Felic, P. Nadagouda, T. Walsh, and E. Skafidas, "Implementation of a Gigabit Per Second Millimetre Wave Transceiver on CMOS," The 2nd International Conference on Wireless Broadband and Ultra Wideband Communications, AusWireless 2007, 27-30 Aug., 2007, pp. 71-74.

[102] B. Yang, Y. Mo, B. Wicks, C. Ta-Minh, F. Zhang, Z. Liu, G. Felic, K. Wang, C. Liu, P. Nadagouda, T. Walsh, R.J. Evans and E. Skafidas, “Implementation of a Gigabit per Second Millimeter Wave Transceiver on CMOS,” AusWireless Book Chapter 2008.

[103] T. Yao, L. Tchoketch-Kebir, O. Yuryevich, M. Q. Gordon, and S. P.Voinigescu, “65 GHz Doppler sensor with on-chip antenna in 0.18 _mSiGe BiCMOS,” in IEEE MTT-S Int. Microwave Symp. Dig., Jun. 2006,pp. 1493–1496.

[104] T. Yao, M. Q. Gordon, K. K. W. Tang, K. H. K. Yau, M.-T. Yang, P. Schvan, S. P. Voinigescu, “Algorithmic Design of CMOS LNAs and PAs for 60-GHz Radio,” IEEE J. OF Solid-State Circuits, Vol. 42, No. 5, May 2007.

[105] T. Yao, M. Gordon, K. Yau, M.T. Yang, S. P. Voinigescu, “60 GHz PA and LNA in 90-nm RF-CMOS,” IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, June 2006.

[106] K. H. K.Yau, A. Mangan, P. Chevalier, P. Schvan, and S. P.Voinigescu,“A scalable transmission-line based technique for de-embedding noise parameters,” in Proc. IEEE ICMTS Conf., Tokyo, Japan, Mar. 2007.

[107] K. H. K. Yau, K. K. W. Tang, P. Schvan, P. Chevalier, B. Sautreuil, and S. P. Voinigescu, “The invariance of the noise impedance in nMOSFETs across technology nodes and its application to the algorithmic design of tuned low noise amplifiers,” in Proc. 7th Topical Meeting on Si Monolithic Integrated Circuits in RF Systems, Long Beach, CA, Jan. 2007.

[108] K.-W. Yu, Y.-L. Lu, D.-C. Chang, V. Liang, and M.F. Chang, “K-band low-noise amplifiers using 0.18 μm CMOS technology,” IEEE Microwave Wireless Component Lett., vol. 14, no. 3, pp. 106-108, Mar. 2004..

[109] F. Zhang, E. Skafidas, W. Shieh, B. Yang, B. N. Wicks and Z. Liu, "A 60-GHz Double-Balanced Mixer for Direct Up-Conversion Transmitter on 130-nm CMOS,” 2008 IEEE Compound Semiconductor IC Symposium (CSICS).

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