HIGHLY EFFICIENT SILICON PHOTONICS DEVICES FOR NEXT GENERATION ON-CHIP INTERCONNECTION NETWORKS

Thesis by

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Abstract

Silicon photonics provides a unique solution to increase the intra- and inter-chip bandwidth and break the transmission layer bottleneck of the conventional cooper wire connections. In order to realize fully integrated on-chip optical interconnection networks, high efficient silicon integrated devices with low loss, broadband and compact size attract more and more attentions. The objective of this dissertation is to investigate novel silicon photonic devices for photonic integrated circuits.

The dissertation starts with a literature survey of key silicon photonics components, which provides basic concepts for the following research work. Then the detailed fabrication processes are introduced, including fabrication processes for single layer passive devices and spot size converter facet smoothing. Electron-beam lithography (EBL) and Reactive Ion Etching (RIE) techniques are discussed. We also highlight several important details during the fabrication to avoid failures. The third part describes three novel devices proposed based on original publications. The circular high contrast grating (HCG) shows ultra-high reflectivity over a broad working bandwidth (> 300 nm). The high polarization extinction ratio (PER) of the circular HCG further demonstrates its suitability as a reflector in hybrid silicon laser designs to avoid mode degeneration. The second device is a 2×2 polarization beam splitter (PBS) on the silicon nitride platform. The PBS has low insertion loss and can support broadband operation with a compact size, which is very challenging with the low material index of silicon nitride. The device was experimentally demonstrated and the results match well with simulation results. Further optimization is also discussed. The third device is an interlayer coupler for high density optical interconnect systems. Interlayer coupler is a critical component for three-dimensional photonic integrated circuits to further increase the chip density. The coupler is designed for both the silicon and the silicon nitride platforms. For the silicon nitride based design, a nonlinear inverse taper with low loss and compact length is further introduced. Compared to the grating based and inverse taper based solutions, the proposed couplers show higher efficiency and lower interlayer
crosstalk. The final part of this thesis summarizes all previous work and discusses some future work based on previous outcome.
Thesis Declaration

This is to certify that:

i. the thesis comprises only my original work towards the PhD except where indicated in the Preface,

ii. due acknowledgement has been made in the text to all other materials used,

iii. the thesis is fewer than 100,000 words in length, exclusive of tables, maps, bibliographies and appendices.

Signed:  

__________________________

Shitao Gao

Date: 17/02/2017
Preface

This thesis presents my work that I have completed throughout my PhD candidatures at the Centre for Neural Engineering and Department of Electrical and Electronics Engineering, University of Melbourne, Australia.

The work presents in Chapter 3 was accomplished in collaboration with Mr. Yang Wang, Dr. Ke Wang, Mr. Dan Smith and Professor Efstratios Skafidas. Mr. Yang and I developed most of the general fabrication processes and the experiment setup. Mr. Dan Smith provides a lot of useful suggestions to assist our development at the Melbourne Centre for Nanofabrication. Dr. Ke Wang, and Professor Efstratios Skafidas provided funding support for the fabrication and useful discussions during the development. My original contribution includes development of the RIE process, realization of the first fiber-to-chip alignment measurement using experiment setup designed by ourselves.

The work presents in Chapter 4 was accomplished in collaboration with Mr. Yang Wang, Dr. Ke Wang, Dr. Chang Joon Chae and Professor Efstratios Skafidas. The results have been published at High contrast circular grating reflector on silicon-on-insulator platform. Optics Letters 41: 520-523, (2016). Mr. Yang Wang contributed part of the fabrication development and provided some useful discussions during the device design process. Dr. Chang Joon Chae initialized the project and provided a very good start point for the design. Dr. Ke Wang, and Professor Efstratios Skafidas provided funding support for the fabrication and useful discussions during the development. My original contribution includes optimization of the original design structure to significantly improve the device performance, conducting all the simulations and data analysis to design the device, fabrication of the device at the Melbourne Centre for Nanofabrication, measurement of the device performance and publishing the results at Optics Letters.

The work present in Chapter 5, was accomplished in collaboration with Mr. Yang Wang, Dr. Ke Wang, and Professor Efstratios Skafidas. The results have been published at Low Loss and Broadband 2×2 Polarization Beam Splitter Based on Silicon Nitride
Platform. *IEEE Photonics Technology Letters*. 28: 1936-1939, (2016). Mr. Yang Wang contributed part of the fabrication development and provided some useful discussions during the device design process. Dr. Ke Wang, and Professor Efstratios Skafidas provided funding support for the fabrication and useful discussions during the development. My original contribution includes proposing the idea and designing the device structure, conducting all the simulations and data analysis to design the device, fabrication of the device at the Melbourne Centre for Nanofabrication, measurement of the device and publishing the results at *IEEE Photonics Technology Letters*.

The work presents in Chapter 6 was accomplished in collaboration with Mr. Yang Wang, Dr. Ke Wang, and Professor Efstratios Skafidas. Mr. Yang Wang, Dr. Ke Wang, and Professor Efstratios Skafidas provided some useful discussions during the development. My original contribution includes proposing the idea and optimizing the device structure for silicon and silicon nitride platforms by simulation.

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I would like to thank the staff members at the Melbourne Centre of Nanofabrication. They provide professional trainings on the fabrication facilities and can always give me useful suggestions for my fabrication processes. The excellent performance of the facilities ensured the device quality in this dissertation.

I would like to thank National ICT Australia (NICTA) for the top-up scholarship through the first 3.5-year study and the funding support for the conference travel.

And finally, I would like to thank my parents and my wife for their strong support in my life.
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List of Symbols

CMOS Complementary Metal-Oxide-Semiconductor
UV Ultra-Violet
BOX Buried Oxide
SOI Silicon on Insulator
EBL Electron-Beam Lithography
FWM Four-Wave-Mixing
MZI Mach-Zehnder Interferometer
ICP Inductively Coupled Plasma
RIE Reactive Ion Etching
PECVD Plasma Enhanced Chemical Vapour Deposition
HCG High Contrast Grating
PBS Polarization Beam Splitter
3D Three Dimensional
FDTD Finite-Difference Time-Domain
c-Si Crystalline Silicon
SEM Scanning Electron Microscope
E-field Electric Field
TE Transverse Electric
TM Transverse Magnetic
FSR Free Space Range
Q-factor Quality Factor
LPCVD Low Pressure Chemical Vapour Deposition
SSC Spot Size Converter
PMMA Polymethyl Methacrylate
BSS Beam Spot Size
HSQ Hydrogen Silsesquioxane
PER Polarization Extinction Ratio
WDM Wavelength-Division Multiplexing
TDM Time-Division Multiplexing
AWG Arrayed Waveguide Grating
SiN Silicon Nitride
MMI Multimode Interferometer
OSA Optical Spectrum Analyser
PC Polarization Controller
ASE Amplified Spontaneous Emission
a-Si Amorphous Silicon
1 Introduction

1.1 OVERVIEW OF SILICON PHOTONICS

Silicon photonics integration has been widely recognized as a key technology for next generation communication systems and on-chip optical interconnect systems to break the bandwidth bottleneck of current electric interconnect systems [1-3]. Because silicon photonics offers higher bandwidth, denser integration, longer transmission distance, lower cost and lower power consumption. As shown in Figure 1.1 [4], the market demand of silicon photonic systems is expected to bloom in the next decade because of the continuous growing data transmission demand inside data centres.

Figure 1.1: Silicon photonics market forecast. Source: Silicon Photonics for Data Centers and Other Application 2016, Yole Développement. [4]
1.1.1 Silicon Photonics On-Chip Optical Interconnect

Silicon photonics provides a unique solution to increase both the intra- and inter-chip bandwidth, and break the transmission layer bottleneck of the conventional cooper wire connections. Recently, optical transceivers based on silicon photonics have been commercialized by companies such as Luxtera, Mellanox, and Intel. The transceiver can be used for large scale cloud and enterprise data centres. The schematic of silicon photonics based transceiver can be shown as Figure 1.2.

![Figure 1.2: Schematic of silicon photonics based transceiver for data centre connection.](image)

The on-chip light source is generated by several hybrid silicon lasers. Then digital signals from data centre are transmitted to the on-chip optical modulators to modulate the optical carrier. The modulated lightwave is combined using wavelength-division multiplexing method through an on-chip optical multiplexer and then transmitted to the receiver through a fiber by using appropriate fiber-to-chip coupling methods. Once the optical signal reaches the receiver, an on-chip de-multiplexer splits the signal based on their wavelengths and on-chip photo-detectors are used to convert the optical signals to digital signals.

The next step for silicon photonics based on-chip optical interconnect is to integrate the optical transmission line on the motherboard to support core-to-core optical transmission. In Figure 1.3, a possible design for the on-chip core-to-core optical interconnect system is shown.
The embedded on-chip optical interconnect system has a similar network structure compared to the system shown in Figure 1.2. However, optical transceivers are connected to the digital components such as processors, memories, and I/O interfaces directly. The embedded system has the ability to break the data transmission bottleneck on the motherboard and improve the performance of local processors.

1.1.2 Fabrication Platform for Silicon Photonics

One of the key advantages of silicon photonics is its compatibility with conventional CMOS fabrication platforms [5,6]. Devices can be fabricated on a silicon-on-insulator (SOI) wafer using deep ultraviolet (UV) lithography, which provides a minimum resolution of 14 nm. The popular SOI wafer used for integrated photonic devices normally comes with 2 ~ 3 μm thick buried oxide layer (BOX) and 220 ~ 250 nm crystalline silicon device layer. The resolution of deep UV is considered sufficient for most integrated photonic device designs. Higher resolution can be realized by using electron-beam lithography (EBL), which can support a higher resolution of 2 nm.
Details of EBL will be introduced in Chapter 2. The fabrication friendly property also helps silicon photonics toward the fabless semiconductor industry [7, 8].

In addition, due to several limitations of the crystalline silicon material, other materials such as silicon nitride, germanium and III-V materials have been developed on top of the silicon layer to support different functions.

### 1.1.3 Challenges for Silicon Photonics

The rapid development of silicon photonics technology is undeniable. However, several limits still exist due to the material property, and still need further research to be addressed.

Firstly, due to its indirect bandgap, silicon is difficult to be used as a gain material and hybrid structures are normally adopted to realize on-chip light sources [9]. Researchers have been working on silicon based lasers for years. Silicon Raman lasers [10, 11], hybrid III-V silicon lasers [12, 13], and semiconductor optical amplifier (SOA) based external cavity silicon lasers [14, 15] have been proposed and demonstrated. The up-to-date hybrid tunable laser has the ability to achieve linewidth lower than 100 kHz and its tuning range covers both the C and the L bands. However, these methods require either external pump source or complicated bonding process. Recently, a continuous-wave InAs/GaAs quantum dot laser has been demonstrated [16], which first time directly grows uniform III-V materials on a silicon substrate. The design opens new possibility for silicon based lasers.

Secondly, due to the time-reversal symmetry property of silicon, the realization of silicon integrated isolators and circulators is also a challenge. In previous studies, a number of mechanisms have been proposed and studied, including the opto-magneto effect [17]-[21], opto-mechanical effects [22, 23], indirect inter-band photonic transitions [24, 25], plasmonics [26, 27], and nonlinear optical effects [28, 29]. However, the fabrication of opto-magneto effect based devices is complicated, and exhibit high insertion loss due to the absorption and scattering at the materials interfaces. In opto-mechanical effects based solutions, both the movable micro-cavity [22] and the optomechanical ring resonator [23] have been utilized. However, it is difficult to integrate the movable micro-cavity with other photonic devices due to the non-planar structure, and the bandwidth of opto-mechanical ring resonator based isolators is
typically highly limited to only a few MHz. The indirect photonic transitions are promising in realizing silicon integrated isolators. Nevertheless, complicated spatial and temporal domains electrical modulation is compulsory and such devices suffer from high insertion loss. We recently proposed a silicon integrated isolator based on four-wave-mixing (FWM) effect [30], which also provides a possible solution to the challenge.

Other than the silicon material physical limitations, several other challenges still remain. Fiber-to-chip coupling method still has a large space to be improved. The grating coupler based methods [31-40] offer acceptable flexibility for measurements and packaging. However, the coupling loss is still at a high level and the working bandwidth is limited. On the other hand, butt coupling [41-47] significantly reduces the coupling loss, whilst its low alignment tolerance causes complexity for measurements and packaging. In addition, a high efficiency layer-to-layer optical coupling method is an indispensable part to realize high density three-dimensional chip design. Other challenges include variability, placement and routing, and verification [48].

1.2 Thesis Outline

The main objective of this thesis is to investigate silicon photonic device fabrication process and new silicon photonic devices for the next generation on-chip optical interconnect networks. Fabrication process using local nano-fabrication facilities is introduced. Several passive devices such as circular grating reflector, polarization beam splitter, and layer-to-layer coupler are designed, fabricated, and experimentally demonstrated. Several potential device optimization solutions and applications are discussed as well.

The thesis begins in Chapter 2 with a literature survey of silicon photonic technologies. Two major fiber-to-chip coupling methods, grating coupler and butt coupler, are introduced. The advantage and limitation of different coupling mechanism are discussed. In particular, we compare the difference between insertion loss, working bandwidth and polarization sensitivity. Several key components, such as silicon waveguide, directional coupler, ring resonator, and Mach-Zehnder Interferometer (MZI), are compared and discussed.
In Chapter 3, the fabrication process for silicon photonic devices using local fabrication facilities is introduced. In our work, E-beam lithography is used for most devices fabrication. Reactive ion etching (RIE) is used to etch multiple materials, such as silicon, silicon oxide and silicon nitride. For thin film deposition, we introduced electron beam evaporation, plasma enhanced chemical vapour deposition (PECVD) and furnace.

Chapter 4 presents a novel high index contrast circular grating reflector (circular HCG) design. The proposed grating is designed based on the SOI platform. The circular HCG has a high reflection over an ultra-wide working bandwidth. The device is designed to have a very compact footprint compare to conventional silicon based reflector designs. In addition, a hybrid silicon integrated laser using the modified circular grating as partial on-chip reflector is proposed and discussed.

In Chapter 5, a MZI based polarization beam splitter (PBS) is designed on the silicon nitride platform. The proposed device has a relative compact size compare to other PBS designs on silicon nitride. The device provides both low insertion loss and wide working bandwidth for both the TE and TM modes. To further improve the device performance, we also introduce the details about the device design and proposed a potential solution to optimize the device.

Chapter 6 presents a layer-to-layer coupling mechanism for both silicon and silicon nitride platforms. The device performance is analysed using 3D FDTD simulations. Both low insertion loss and wide working bandwidth are achieved. In addition, this method allows relatively wide gap between two transmission layers without using very thin device layers, which significantly reduced the interlayer crosstalk.

Chapter 7 gives a summary of the main findings and conclusions of the thesis, and a discussion of possible future work.

1.3 Original Contributions

The original contributions of this thesis are as follows:

- Develop the fabrication process for silicon photonic devices at Melbourne Centre for Nanofabrication (Chapter 3). The details of the fabrication process are included.
Introduction

- Design and demonstration of a circular high index contract grating reflector on SOI (Chapter 4). The device was fabricated and experimentally demonstrated. Key parameters such as reflectivity and bandwidth have been measured and discussed.

- Design and demonstration of polarization beam splitter on silicon nitride platform (Chapter 5). The device fabrication process and performance are discussed.

- Introduce a feasible optimization solution to further improve the polarization beam splitter (Chapter 5). Principles and simulation results are discussed.

- Propose a layer-to-layer coupling method for both silicon and silicon nitride platforms (Chapter 6). Detailed design and simulation results are investigated and discussed.
2 Key Components and Technologies in Silicon Photonics Design

2.1 Silicon Waveguides

2.1.1 Slab, Strip and Ridge Silicon Waveguides

The first silicon waveguide was demonstrated in mid 1980s [49, 50]. The early stage silicon-on-silicon waveguide has a low refractive index difference of 0.01 between the substrate and the device layer. The propagation loss was reported as 5 to 13 dB/cm in the slab waveguide and 15 to 20 dB in the rib waveguide [50]. The high propagation loss is mainly due to the low light confinement between the substrate and the device layer which causes light power leakage to the substrate.

In order to improve the light confinement problem, modern silicon waveguides are normally fabricated on SOI wafers. The first slab silicon waveguide on SOI was proposed in 1988 [51]. After that strip waveguide was proposed to reduce the waveguide dimension [52], and low loss rib waveguide was proposed as well [53, 54]. In Figure 2.1(a) and (b), we show the cross-sectional structure of the two basic silicon waveguide structures, strip waveguide and ridge waveguide. An SOI wafer consists of three layers. The bottom layer is the silicon substrate, which normally comes with a thickness of 500–600 μm. The buried oxide layer (BOX) is grown on top of the substrate with a refractive index around 1.44. The thickness of the BOX layer is normally 2 ~ 3 μm to provide sufficient gap between the substrate and device layer and avoid light leakage. Then 220 ~ 250 nm crystalline silicon (c-Si) with a refractive index of 3.474 is served as the device layer. On top of the fabricated waveguide, a SiO₂ layer with refractive index of 1.51 is deposited as the over cladding. Light is then confined in
the silicon core and propagates along the waveguide direction. Due to the large index difference between the device layer and the BOX layer, light is high confined in the waveguide core and the leakage loss is significantly reduced and compact device design becomes possible. However, due to the high index contrast, the waveguide loss is sensitive to the sidewall roughness due to scattering loss and requires high quality control of the etching process during fabrication. Strip waveguide with oxidation smoothing was reported to have a loss low to 0.8 dB/cm [55]. In Figure 2.1(c), we show the SEM image of the fabricated strip waveguide with a dimension of 450 nm × 220 nm. Low index contrast waveguides on silicon nitride were proposed with a lower propagation loss, due to its lower sensitivity of scattering loss from sidewall roughness [56-58].

![Figure 2.1: Schematic of the cross-sectional view of a silicon waveguide, (a) strip waveguide and (b) ridge waveguide. (c) SEM image of a fabricated silicon waveguide on SOI wafer, without oxide over-cladding.](image)

### 2.1.2 Slot Waveguides

Besides the conventional strip and ridge waveguides, a silicon slot waveguide was proposed in 2004 [59]. The schematic of a silicon slot waveguide is shown in Figure 2.2(a). Unlike the conventional waveguides that light propagates in the high index silicon core, for slot waveguides, light propagates in the narrow slot with low index between two high index contrast silicon bars. In Figure 2.2(b), we show the e-field profile of a slot waveguide, with 220 nm silicon device layer, 250 nm wide silicon bar, and 100 nm wide slot. Compare to the conventional silicon waveguide structures, the slot waveguide provides higher index changes by directly manipulating the high power confinement region, and hence, provides additional flexibility for device designs.
Applications such as microring resonators [60-62], modulators [63, 64], polarizers [65] and polarization splitter [66], directional couplers [67] and biosensors [68-70] were proposed and demonstrated during the past a few years.

Figure 2.2: (a) Schematic of a silicon slot waveguide, and (b) e-field profile of a slot waveguide.

2.1.3 Guided Modes

There are two different guided modes in a silicon waveguide, the transverse electric (TE) like modes and transverse magnetic (TM) like modes, respectively. For the TE modes, the electric fields of the waves are perpendicular to the plane of incidence. While for the TM modes, the electric fields of the waves are perpendicular to the plane of incidence. It is important to design the waveguide to provide single mode condition. An efficient approach to calculate the required waveguide dimension is to use the eigenmode solver. In Figure 2.3, we show the simulated effective index of a strip waveguide with 220 nm height. It is clear to see that the TE\(_1\) mode is cut-off when the waveguide width is smaller than about 470 nm. In this case, we normally use the width of 450 nm or 460 nm as the standard single mode waveguide. Another thing we can notice here is the overlap between the lines of the TM\(_0\) and the TE\(_1\) modes. This property has been widely used to realize polarization converters [71-73].

In Figure 2.4, we show the e-field distribution of the fundamental TE and TM modes operation using a 460 nm × 220 nm strip silicon waveguide. Due to different power distribution and effective index of the TE and the TM modes, the performance is different in some cases. The TM modes normally have a lower sensitivity of sidewall roughness, and hence, have lower scattering loss. Because under the TM mode operation, power mainly distributed on the top and bottom interface of the silicon
waveguide, and the surface is normally smooth and flat when using commercial SOI wafers. However, the TE modes operation suffers significant scattering loss from the sidewall roughness. In addition, the TE modes can sustain a smaller bend radius compare to the TM modes. Because most power of the TE mode operation is confined in the waveguide core and have relatively lower radiation loss with small bending radius [74].

![Figure 2.3: Effective refractive index of a strip silicon waveguide vs. different waveguide widths based on simulation results using eigenmode solver.](image)

![Figure 2.4: E-field profile of a 460 nm × 220 nm strip silicon waveguide with (a) TE mode; and (b) TM mode.](image)
2.2 DIRECTIONAL COUPLER

Directional coupler is one of the most widely used optical component for power splitting and combining. In Figure 2.5, we show a simple symmetric directional coupler.

\[ \kappa = \frac{2k_{xc}^2 k_{xg} e^{-k_{xg}g}}{\beta w (k_{xg}^2 + k_{xc}^2)} \]  \hspace{1cm} (2.1)

where \( \beta \) is the propagation constant along the waveguide, \( w \) is the waveguide width, \( g \) is the gap between two waveguides, \( k_{xg} \) is the \( x \)-directed (between the waveguides) decay constant and \( k_{xc} \) is \( x \)-directed propagation constant. Based on this equation, we can see that the gap width \( g \) and the decay constant \( k_{xg} \) have strong impact to the coupling coefficient. Smaller gap and lower decay constant normally provides stronger coupling. Furthermore, different operation wavelength and polarization provides different parameters (\( \beta, k_{xg} \) and \( k_{xc} \)), the directional coupler is both wavelength and polarization dependent. It indicates that appropriate fabrication quality control is required for the waveguide and gap width to ensure the coupler performs properly. Recent research has shown that the fabrication tolerance and operation bandwidth can be improved by using optimized structures [76, 77].

The critical coupling (100%) length can be calculated using the following equation:
\[
L_c = \frac{\lambda}{2(n_{\text{even}} - n_{\text{odd}})}
\]  

(2.2)

where \( \lambda \) is the central wavelength, \( n_{\text{even}} \) and \( n_{\text{odd}} \) are the even and odd supermode effective index, which can be easily calculated using an eigenmode solver.

### 2.3 Microring Resonator

Microring resonator plays an important role in silicon photonic designs, especially for wavelength selective function. It has a broad range of applications, such as filters [78-83], modulators [84-87] and biosensors [88, 89], due to its compact size and high performance. The microring resonator has been extensively studied during the last decades [90-92], so here we only briefly summarize some key parameters for the microring resonator design. The basic structure of a microring resonator can be shown in Figure 2.6.

![Microring Resonator Diagram](image)

*Figure 2.6: Schematic of (a) all-pass, and (b) add-drop microring resonators.*

For the all-pass structure, shown in Figure 2.6(b), the resonant wavelength is the wavelength where the phase change after travel a cycle of the microring is a multiple of \( 2\pi \), and it can be easily calculated using the following equation:

\[
\lambda_{\text{res}} = \frac{2\pi R \times n_{\text{eff}}}{m}
\]  

(2.3)
where $R$ is the radius of the microring, $n_{\text{eff}}$ is the effective index of the waveguide, and $m$ is an integer. So, smaller microring radius can provide denser through-port spectrum. Then the free space range (FSR), which is the wavelength range between two adjacent resonant wavelengths, can be calculated as:

$$\text{FSR} = \frac{\lambda^2}{2\pi R \times n_g}$$

(2.4)

where $n_g$ is the group index which takes into account the dispersion of the waveguide. Another key parameter we need to take into consideration when design the microring resonate is the quality factor (Q-factor), which measures the sharpness of the resonance. For the add-drop microring resonator, the Q-factor is [79]:

$$Q = \frac{2\pi R \times n_g \pi \sqrt{r_1 r_2 a}}{\lambda_{\text{res}} (1 - r_1 r_2 a)}$$

(2.5)

In equation (2.5), $r$, $r_1$ and $r_2$ are the self-coupling coefficient as shown in Figure 2.6. The self-coupling coefficient is $1 - k^2$ assume there is no coupling loss and $k$ is the cross-coupling coefficient as we introduced in Section 2.2. $a$ is the single pass amplitude transmission, which includes both propagation loss in the microring and the coupling loss ($a = r$ under critical coupling).

As we can assee from these equation, the coupling coefficient and the loss mainly determine the quality of the microring. Since the coupling coefficient is sensitive to the coupling gap width, the microring resonator also has a tight fabrication tolerance. In Figure 2.7, we show the SEM image of a fabricated microring resonator with 460 nm waveguide width and 200 nm coupling gap. The microring radius is also a critical parameter in the design. Smaller radius gives larger FSR, but also brings higher wavelength bending loss and reduces the Q-factor. Under careful design, microring with a radius of 1.5 μm and a Q-factor of 9,000 has been demonstrated [93].
Key Components and Technologies in Silicon Photonics Design

Figure 2.7: SEM image of microring resonator with 460 nm waveguide width, 220 nm device thickness and 200 nm coupling gap.

2.4 **Mach-Zehnder Interferometer**

Mach-Zehnder Interferometer (MZI) is another widely used component in silicon photonics systems. Compare to the microring resonator, MZI has a broader bandwidth, and the two arms provide additional flexibility to realize different applications, such as temperature insensitive filters [94, 95], modulators [96-99], optical switches [100, 101], and sensors [102-106]. In Figure 2.8, we show a simple structure MZI with two 3 dB directional couplers. The phase difference $\Delta \phi$ of the lower arm can be achieved by using either different waveguide width or length, or using thermal or electric active control to change the effective index of the waveguide. The Output power can be simply derived as:

$$P_{\text{out}} = \frac{1}{2} E_{\text{in}}^2 + \frac{1}{2} E_{\text{in}}^2 \cdot \cos(\pi + \Delta \phi)$$  \hspace{1cm} (2.7)
where $E_{in}$ is the input electric field. By tuning the phase difference $\Delta \phi$, we can manipulate the output power for different purposes.

![Figure 2.8: Schematic of a MZI with two 3 dB directional coupler.](image)

### 2.5 Fiber-to-Chip Coupling

Fiber-to-chip coupling technique is an indispensable part of silicon photonics technology, from silicon photonic device characterisation to packaging. There are two main approaches for coupling light from and to a fiber, the grating coupler based approach [107-114] and the edge coupling approach [115-123]. Normally, grating couplers have a better misalignment tolerance, but with the cost of lower coupling efficiency and narrower bandwidth (tens of micro meters). Better performance can be achieved with complicated fabrication process [111-113]. On the other hand, edge coupler uses a spot size converter to match the fiber output mode. The insertion loss of the edge coupler is about 1 dB but smooth end-chip facet or polymer overlay waveguide is required to ensure the performance. The operation bandwidth of the edge coupler is over hundreds micro meters but the misalignment tolerance is much tighter compare to the grating couplers.

#### 2.5.1 Grating Coupler

In Figure 2.9, we show the schematic of the grating coupler based fiber-to-chip mechanism. Light is injected from the fiber with a small incident angle, and then reflected into the waveguide by appropriate designed grating. The grating is normally wavelength and polarization dependent, and hence, brings a few limitations to the
grating coupler. Also in Figure 2.9(b), we can see there is also some power leaks into the bottom layer, which explains the reason of higher loss with grating coupler.

*Figure 2.9: Schematic of the grating coupler mechanism, (a) 3D view, and (b) cross-sectional view.*

### 2.5.2 Spot Size Converter

In Figure 2.10, we show the structure of the edge coupler. The lensed fiber is normally utilized with on-chip edge couplers to provide a smaller spot size and reduce insertion losses. The design of the spot size converter is very simple. Normally, on a SOI wafer with 220 nm device layer, the tip width is around 180 nm to 200 nm. Through a taper of 100 μm, the injected light is then coupled into the waveguide. Smaller tip size and longer taper length can efficiently reduce the insertion, but it subjects to the lithography resolution. The misalignment tolerance is normally smaller than 1 μm for 1 dB, which brings difficulties for measurement and packaging. Polymer overlay waveguide can help to reduce coupling loss [116, 117, 119, 121], but again, it brings additional fabrication complexity. The edge coupler can provide an operation bandwidth over 100 μm and its performance is not significantly impacted by different injected light polarization.
We use the edge coupling method in all the following measurement. In addition, smooth end-chip facet is required to reduce coupling loss as we mentioned before. The detailed fabrication process will be discussed in Chapter 3. In Figure 2.11, we show the experiment setup with the edge coupling method and the SEM image of a fabricated spot size converter with 200 nm tip width.

**Figure 2.11:** (a) Experiment setup with edge coupling, and (b) SEM image of a fabricated spot size converter with 200 nm wide tip.

### 2.6 Summary

In this chapter, several important silicon photonics components such as silicon waveguides, directional couplers, ring resonators and MZIs are introduced and reviewed based on literature survey. Two fiber-to-chip coupling methods are reviewed as well. The components are highly useful in the following technical chapters. For the fiber-to-
chip method, the spot size converter provides wide operation bandwidth and polarization independent properties. The spot size converter based solution is more suitable for our device designs and is chosen as our fiber-to-chip coupling method in the following research work. However, on the other hand, the grating coupler based solution provides a better alignment tolerance but requires different depth etching process.
3 Fabrication Techniques for Silicon Photonics

3.1 Overview

The fabrication techniques for silicon photonic devices have been rapidly developed during the last decades. As we discussed in Chapter 1, SOI wafers with 220 nm or 250 nm device layer are popular platforms for silicon photonic designs. Materials such as silicon nitride and germanium are developed to support various applications as well.

There are three key steps in silicon photonics fabrication: lithography, etching and film deposition. The resolution of the lithography process determines the smallest feature size that can be achieved. Generally, two lithography processes are used in silicon photonics fabrication. One is deep-UV lithography, which uses exposure light wavelength of 248 nm or 193 nm. Due to the fast-repeating attribute of deep-UV lithography, this technique is utilized where high volume fabrication is required. On the other hand, electron-beam lithography (EBL) can provide a resolution low to 1-2 nm in a research lab environment. However, it has to write the pattern one by one, and hence, takes more time for the lithography process. The details of EBL will be discussed in the following section.

For the lithography process, a resist layer is first coated on top of the device layer. Then the resist is exposed to a pattern of light or electron and the exposure causes chemical changes of the resist. For positive resist, the exposed area then can be removed by a resist developer. While for negative resist, the unexposed area would be removed during the develop process. In Figure 3.1, we show the schematic of the lithography process. One thing we should notice here is that, unlike deep-UV lithography, EBL directly writes the pattern on the resist instead of using a mask. The quality control of the lithography is critical for silicon photonic device performance, such as pattern size error and roughness.
There are generally two etching methods, wet etching and dry etching. For wet etching, materials are removed by using liquid chemicals with defined etching resist. Wet etching is normally isotropic and used to form curve sidewall, which is not suitable for silicon photonic devices in most cases. Because for silicon waveguides, as we introduced in Chapter 2, smooth and straight sidewall is required to ensure low loss light propagation. Dry etching technique has been well developed for silicon photonics fabrication. Reactive ion etching (RIE) combines both chemical and physical etching to support anisotropic material removal. For a 220 nm SOI wafer, the device pattern can be etched within 2 minutes. High quality sidewall can be achieved as well. The etching resist on top the sample substrate is important for the etching process, not only for the patterning but also for the etching quality. The details will be discussed in Section 3.3.

Thin film deposition techniques are widely used in CMOS and silicon photonics fabrication. Materials such as silicon oxide, silicon nitride and metals are used in the device designs. Plasma enhanced chemical vapour deposition (PECVD) is mainly used for over-cladding deposition. While Low pressure chemical vapour deposition (LPCVD) is used to deposit high quality silicon nitride layer. Furnace can be used to grow oxide layer under high temperature and electron beam evaporator is used to deposit metal layers as etching resist. Since most thin film deposition techniques are quite mature, the details will not be included in this thesis.

As we mentioned in Chapter 2, spot size converter is used to realized fiber-to-chip coupling. Therefore, smooth chip facet is required to ensure low insertion loss. In Figure
3.2, we show the full fabrication steps used for the following research work. The details will be discussed in the following sections.

Figure 3.2: Full fabrication processes for a passive single layer silicon photonics device. (a) bare SOI wafer; (b) EBL resist spin coating; (c) EBL exposure and development; (d) chromium deposition using e-beam evaporator; (e) lift-off; (f) device layer etching; (g) etching mask removal; (h) over-cladding deposition using PECVD; (i) side view of the spot size converter; (j) thick SU8 spin coating; (k) UV lithography and development; (l) silicon dioxide etching; (m) bosch process, silicon substrate deep etching; (n) SU8 removal; (o) dicing; (p) complete sample chip. Y-z plane is the cross-sectional view of the device and x-z plane is the side view of the spot size converter (SSC).

Figure 3.2(a) – (h) show the fabrication processes for a single layer passive silicon photonics device. In Figure 3.2(i) – (p), we show the processes to generate the small
chip facet for fiber-to-chip measurement purpose. SU8 was used as lithography resist and etching mask for these steps. UV lithography with around 1 \( \mu \)m resolution was used to generate the pattern for silicon dioxide etching and Bosch process. The chip measurement facet was fabricated using RIE instead of dicing to ensure the smoothness. The last step is to dice each single chip off the wafer along the trenches.

### 3.2 ELECTRON-BEAM LITHOGRAPHY

#### 3.2.1 Overview of EBL

Electron-beam lithography (EBL) is an advanced technology to achieve a resolution of sub-10 nm. EBL uses a focused electron beam to directly draw patterns on the resist layer which is a thin electron-sensitive film. The first EBL was developed in the late 1960’s by modifying a scanning electron microscope (SEM) [124]. State of art EBL systems are fully integrated systems that can support high brightness electron beam for fast writing and high resolution. The write time \( T \) of EBL process can be estimated by using the following equation [125]:

\[
T = \frac{D \times A}{I}
\]

where \( D \) is the dose used, \( A \) is the size of beam exposed area, \( I \) is the beam current. As we can see from this equation, the EBL process is only suitable for small volume fabrication requirement due to its limited writing speed and mainly used in research lab environment. But its high-resolution attribute makes EBL widely used in silicon photonics design and fabrication.

The beam spot size (bss) and the step size are two important parameters in EBL process. Basically, the beam spot size determines the feature size of the EBL process. Equation 3.1 can be rewrite as:

\[
F(MHz) = 0.1 \times \frac{I(nA)}{D(\mu C/cm^2) \times bss^2(\mu m)}
\]
where $F$ is the writing frequency.

The relation between the beam spot size and the step size can be shown in Figure 3.3. While the step size is the distance the beam moves between two adjacent beam spots. The ratio between the beam spot size and step size will affect the exposure quality since the electron strength is not evenly distributed along the exposure direction. Normally, the step size is set the same as the beam spot size to keep the edge of the pattern smooth.

![Figure 3.3: Schematic of beam spot size and step size.](image)

### 3.2.2 EBL Resists

The first step of the EBL process is to coat the EBL resist on top of the sample. Similar to UV lithography, there are two kinds of EBL resist, positive and negative. Positive EBL resists include PMMA and ZEP520A. Hydrogen silsesquioxane (HSQ) is used as negative resist in EBL process. The resist layer is coated by using a spinner and baked on a hot plate. HSQ can be directly used as etching resist after the EBL process. PMMA and ZEP520A normally require metal deposition after development and the lift-off process to generate the etching mask. However, ZEP520A is a highly sensitive material and requires very low dose ($\sim 200 \mu C/cm^2$) to clear the pattern. The writing time is much faster with ZEP as resist compare to other resist material based on equation 3.1. ZEP also provides high etching durability and stability, which makes it suitable as etching mask as well [126, 127]. However, ZEP is more expensive compare to PMMA. The minimum resolution that ZEP and PMMA can support is around 30 nm. On the other hand, HSQ can support a higher resolution ($\sim 10$ nm) and provide better sample quality compare to other resists [128]. However, HSQ is hard to remove after the EBL
process and normally be used as over-cladding in silicon photonics fabrication, which may cause some problem in certain designs.

The typical process for positive and negative resists is shown in Figure 3.4. For positive resists, 20 to 30 nm metal (normally chromium) is deposited on the sample using electron beam evaporator for high quality purpose, and then the lift-off process is required to form the etching mask.

**Positive resist**

- **Exposure**
- **Development**
- **Deposition**
- **Lift-off**

**Negative resist**

- **Exposure**
- **Development**

*Figure 3.4: Flow of EBL process to form the etching resist.*

The thickness of the resist layer is important in the process. Different thickness will need different base dose to clear the pattern. The ratio between the resist thickness and the feature size of the sample also needs to be considered. Thick resist normally cannot support very small feature size (< 100 nm) and will collapse during the process. In Figure 3.5, we show the SEM image of 380 nm thick ZEP520A resist with 20 nm line patterns.
The resist collapse because of very high aspect ratio (19:1 in this case) and makes the exposure failed. For ZEP, the safe aspect ratio is normally below 4:1 for resist thickness to feature size.

In addition, the following tables show the typical parameters used for spin coating in this thesis work.

<table>
<thead>
<tr>
<th>Resist material</th>
<th>1:2 diluted ZEP520A</th>
<th>HSQ</th>
</tr>
</thead>
<tbody>
<tr>
<td>Spin speed (rpm)</td>
<td>1000</td>
<td>1000</td>
</tr>
<tr>
<td>Spin time (sec)</td>
<td>42</td>
<td>62</td>
</tr>
<tr>
<td>Baking temperature (°C)</td>
<td>180</td>
<td>80</td>
</tr>
<tr>
<td>Baking time (sec)</td>
<td>180</td>
<td>240</td>
</tr>
</tbody>
</table>

_Table 3.1: Parameters for EBL spin coating process with 1:2 anisole diluted ZEP520A and HSQ._

### 3.2.3 Dose Test

The base dose is the first dose value that can give a clear pattern. The base dose is a key parameter in the EBL process. For doses under the base dose value, the resist will not be fully cleared during the development process. The residual resist causes device pattern errors after the RIE process. While for over dosing, patterns will be wider than the design and will cause problems such as merging and shape changing. It is difficult to calculate the right base dose using the equations. A dose test based on experiment called
dose test is normally used to get the base dose. We draw a 25 μm × 25 μm rectangle with 0.1 nA and 100 kV beam. The dose value is increased in 10 μC/cm$^2$ each step. In this case, we use 1:2 anisole diluted ZEP520A as resist. The resist was spin coated using the parameters in Table 3.1. The results are shown in Figure 3.6.

![Image of dose test results for 1:2 diluted ZEP520A with 0.1 nA and 100 kV beam.](image)

*Figure 3.6: Dose test results for 1:2 diluted ZEP520A with 0.1 nA and 100 kV beam.*

The difference of the results is not visible under the microscope after 140 μC/cm$^2$. Then we draw a 100 μm × 100 μm straight line grid to see if the pattern is cleared. The SEM image of the line grid with different dose value is shown in Figure 3.7.
Chapter 3

Figure 3.7: SEM image of a $25 \mu m \times 25 \mu m$ line grid with different dose.

There are visible residues when the dose value is lower than 190 $\mu C/cm^2$. Here, 190 $\mu C/cm^2$ is the first dose value to fully clear the pattern, and is chosen as the base dose in the following experiment. In addition, PMMA and HSQ normally have a base dose over 1500 $\mu C/cm^2$, the details of the dose tests of PMMA and HSQ are not included in this thesis, while the approach is similar.

Under further measurement, we notice that the dimension of the pattern with ZEP520A is normally 5 nm wider than the designed parameter even with the base dose. Therefore, 5 nm bias is set in the software when generating the exposure file.

The dose test is only valid for the same resist property. The change of resist liquid concentration, spin speed, baking temperature, baking time and beam property will all affects the base dose value and requires to re-perform the dose test.
3.2.4 Scattering

The state of art EBL systems can support resolution low to sub-10 nm level. However, the scattering problem usually limits the actual final resolution to a worse level. When electrons inject into the resist layer, some of the electrons will gradually lose their energy and change the inject direction. This fact is called forward scattering and normally more seriously with lower beam energy and thicker resist [129-130]. The forward scattering will cause the pattern broader than the design. Another scattering is the backscattering problem. Some of the inject electrons will be reflected by the substrate and go through the resist a few micrometres away again, especially with higher energy. This phenomenon is called proximity effect [131-133]. The proximity effect will cause over dose problem when expose high density patterns. The schematic of both forward scattering and backscattering is shown in Figure 3.8. Both forward scattering and proximity effect limit the actual resolution of the EBL exposure, especially for high density patterns.

![Figure 3.8: Schematic of forward scattering and backscattering.](image)

Proximity effect correction is normally used to optimize the exposure of small feature size and high-density patterns [134-136]. Software such as BEAMER [137] provides a powerful simulation tool for the optimization by taking the material property and layer thickness into consideration.

3.3 Etching

Reactive-ion etching (RIE) is a type of dry etching and generally used as the etching technique in micro- and nano-fabrication. RIE uses the combination of chemical gas and
reactive plasma to provide anisotropic etching profile and fast etching speed. These advantages make RIE preferred in many silicon photonics fabrication steps. Since RIE is a highly developed technology, details of its principle will not be included in this chapter.

RIE is widely used in our fabrication processes, including silicon device layer etching, silicon dioxide etching and Bosch process for deep silicon etching. Especially for silicon device layer etching, we use Pseudo Bosch silicon etching which use SF$_6$ and C$_4$F$_8$ gas mixture. This etching provides a relative slow etching rate and good quality control for nanoscale etching. Based on our experience, the sidewall roughness is also improved with this etching method. Some study of the Pseudo Bosch silicon etching can be found in [138]. The key parameters of the etching recipes are included in Table 3.2.

<table>
<thead>
<tr>
<th>Recipe</th>
<th>Silicon</th>
<th>Silicon oxide</th>
<th>Silicon nitride</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gas 1 (sccm)</td>
<td>30-35 SF$_6$</td>
<td>2 O$_2$</td>
<td>50 CHF$_3$</td>
</tr>
<tr>
<td>Gas 2 (sccm)</td>
<td>50-60 C$_4$F$_8$</td>
<td>45 C$_4$F$_8$</td>
<td>20 O$_2$</td>
</tr>
<tr>
<td>Temperature (°C)</td>
<td>12-15</td>
<td>12-15</td>
<td>12-15</td>
</tr>
<tr>
<td>ICP power (W)</td>
<td>1000-1200</td>
<td>2100</td>
<td>2500</td>
</tr>
<tr>
<td>Forward Power (W)</td>
<td>10-20</td>
<td>200</td>
<td>50</td>
</tr>
<tr>
<td>Pressure (mT)</td>
<td>10</td>
<td>7</td>
<td>6</td>
</tr>
<tr>
<td>Etching ratio (nm/min)</td>
<td>180</td>
<td>360</td>
<td>70</td>
</tr>
</tbody>
</table>

Table 3.2: Parameters of etching recipes used in this thesis.

One thing brings our attention during the process is the necessity of using Fomblin oil between the holding wafer and the sample when doing RIE. Otherwise, serious undercut may happen with metal etching mask. In Figure 3.9, we show the SEM image of an undercut silicon waveguide, with 20 nm chromium mask on top. The same issue
happened in [138], while the reason and the solution were not provided. Based on our test, using tape or simply putting the sample on the holding wafer will cause this problem. The possible reason is because of the temperature changing during the process. Without Fomblin oil, the sample will be heated during the process and cannot be cooled down by the substrate. The temperature change of the sample then causes the undercut problem. Heat can be better transferred between the holding wafer and the sample through Fomblin oil and eliminate the undercutting problem. Etching without a holding wafer or using non-metal etching mask such as HSQ or silicon oxide will reduce the impact of this issue. But for diced chip sample, Fomblin oil still provides the best performance based on our experiments.

![SEM image of a undercut silicon waveguide with 20 nm chromium mask.](image)

*Figure 3.9: SEM image of a undercut silicon waveguide with 20 nm chromium mask.*

With proper pre-process preparation, stable etching quality was achieved. In Figure 3.10, we show the SEM images of the fabricated silicon devices with previous mentioned using Pseudo Bosch silicon etching.
Figure 3.10: SEM images of fabricated silicon devices with Pseudo Bosch silicon etching.

As we can see, the etching gives a well sidewall straightness. However, there are still some visible sidewall roughness. This is mainly due to the use of metal etching mask and can be further improved by using HSQ as EBL resist and etching mask. The fabricated silicon waveguide has a loss lower than 3 dB/cm based on our measurement.

In addition, we show the SEM image of the cross section of a silicon nitride waveguide in Figure 3.11.

Figure 3.11: Cross section view of a silicon nitride waveguide, with 600 nm thick device layer and 20 nm chromium etching mask on top.
The straightness of the silicon nitride waveguide is slightly worse compared to the silicon waveguide and requires further improvement. However, due to the low material index, the silicon nitride waveguide has much lower propagation loss (< 1 dB/cm).

As we mentioned in Section 3.1, Bosch process was used for silicon substrate deep etching, so the fiber will not be touched by the substrate during measurement. The Bosch process includes an etch step and a deposition step. During the etch step, plasma with SF$_6$ will react with silicon and remove it away. While for the deposition step, plasma with C$_4$F$_8$ will form a thin polymer layer on the surface of the wafer. The polymer layer will protect the silicon being further etched and it must be removed before the next etch step. The removal of the polymer layer is done by using the ions in the plasma. Since the ions are accelerated and highly directional (vertical to the sample), only polymer at the bottom of the trench will be removed, while the rest will protect the silicon trench sidewall being further etched. The process will be repeated over 100 times to etch hundreds of micro-meters silicon substrate with very high resist selectivity (~1:100).

About 10 μm SU8 negative resist is used during the process from Figure 3.2(i) – (p). During the experiments, we noticed that SU8 will lose adhesion if it is directly spin coating on top of PECVD oxide. In Figure 3.12, we show a wafer with peeled off SU8 resists. The reason of this issue is still under investigation, while a possible solution is to coat and bake 10 nm OmniCoat [139] on top of the PECVD oxide.

Figure 3.12: Peeled off SU8 on top of PECVD oxide.
3.4 **Summary**

In this chapter, we mainly discuss the detailed fabrication processes for silicon photonics devices. Especially, we focus on the optimization of the EBL process and the RIE process. The quality of the EBL process plays an important role in the fabrication. We introduced the impact with different EBL resists and the process for dost test. PEC was used in the EBL optimization to reduce the impact from the scattering problem. By several rounds of process development and optimization, we achieved straight and smooth sidewall for our SOI based devices. The fabricated waveguide has a reasonable and competitive propagation loss of less than 3 dB/cm. The chip facet is fabricated by using RIE for oxide layer etching and Bosch process for deep silicon substrate etching to ensure smoothness. Using this polish-free process can significantly reduce the insertion of the spot size converter. During the fabrication, the undercut problem can be overcome by using Fomblin oil between the sample chip and holding wafer. The SU8 peel off problem with PECVD oxide layer can be addressed with an additional OmniCoat layer. In addition, we also introduce the RIE process for silicon nitride etching. The waveguide propagation loss is lower than 1 dB/cm for the silicon nitride waveguide due to lower scattering loss from the waveguide sidewall roughness.
4 High Contrast Circular Grating on Silicon on Insulator Platform

4.1 OVERVIEW

Silicon photonics is a rapidly developing and promising technology to break the bottleneck of short range on-chip interconnect systems due to its compact size, high power efficiency and low cost [140-142]. Among key integrated optical devices, the on-chip Bragg gratings, which serves as optical mirrors, have been utilized in a wide range of applications such as laser cavities and filters [143, 144]. On the silicon-on-insulator (SOI) platform, waveguide core index modulation based gratings have been realized by using either ion implantation [145, 146] or periodic change of the waveguide geometry in the vertical or the lateral direction [147-151]. The waveguide based gratings have been widely used as reflectors to construct resonators and hybrid lasers [152-154]. However, the periodic effective index change ($\Delta n$) for such devices is small on the popular thin SOI platform which normally has a silicon device layer of 220 nm, thus requiring a large number of periods to achieve high reflectance. This results in both large devices and wavelength dependent gratings with limited bandwidth. In order to increase the effective index change, high-index-contrast gratings with fully etched straight silicon/trench interfaces have been proposed and demonstrated. The fully etched structure maximizes the effective index change between silicon bars and trenches and thus providing much broader reflection band. High reflectance (> 90%) over a wide bandwidth (> 200 nm) has been realized with only a few grating periods (< 10) on SOI wafers with thick silicon layers (> 1 μm) [155, 156]. But if we simply transfer the fully etched straight structure to the thin device layer SOI platform, the performance would dramatically reduce or even fail to work due to the large diffraction loss [157]. The diffraction loss is mainly from the mismatch between the inevitable circular optical
wavefront from the sub-wavelength waveguide end and the rectangular shape of silicon/trench interface.

On the other hand, loop mirrors [158, 159] are able to provide wide bandwidth and comparable reflectance with careful design of the Y-junction splitters. But the mirror size is limited by the bending radius to ensure low bending loss. Furthermore, unlike grating reflector, loop mirror has polarization independent characteristic, which means it may increase polarization degeneracy for applications such as tunable lasers without other specific designs.

A HCG reflector with broadband operation, high reflectance and solid polarization selectivity on thin SOI platform becomes challenging and necessary. Considering the compactness and design simplicity, we proposed a HCG on the SOI with 220-nm-thick silicon layer with circular silicon/trench interfaces which effectively reduce the diffraction loss by using the circular structure to fit the wavefront from the waveguide end [160, 161].

In this Chapter, the detailed circular HCG design and the optimization procedures are presented is introduced in Section 4.2. The optimized circular HCG is capable of achieving high reflectance (> 90%) over a wide wavelength range (> 300 nm). In addition, the circular HCG can provide high polarization extinction ratio (PER) to reduce the polarization degeneracy and maintain the polarization stability. Then the fabrication processes for the circular HCG is introduced in Section 4.3. The details of the circular HCG experimental demonstration are discussed in Section 4.4. The footprint of the fabricated device is only $4.03 \times 4.32 \, \mu m^2$. Based on experimental measurement results, the device achieves an average reflectance of over 94.15% across the measured wavelength range with a PER exceeding 13 dB. In Section 4.5, we proposed an application using the proposed circular HCG. The circular HCG can be used to construct the external cavity of a hybrid silicon laser. Potential improvements by using such a laser are discussed.

4.2 New High Contrast Circular Grating Reflector

4.2.1 Structure of the Proposed High Contrast Circular Grating

The structure of proposed circular HCG reflector is shown in Figure 4.1. It consists of an input waveguide and several silicon blades with fully etched trenches. The device is designed and fabricated on a SOI wafer with 220-nm-thick thin silicon layer and 2-μm-thick buried oxide (BOX) layer. The width of the input waveguide is chosen as $W_0 =$
460 nm for single-mode operation. The widths of each silicon blade and trench are $W_s$ and $W_t$, respectively. The trenches are filled with top cladding material (in this case is 2-μm-thick SiO2). Basically, the device performance reduces with larger gap (when $W_g$ is larger than 15 nm) [161]. Here, a gap with width of $W_g = 30$ nm is set between the input waveguide and the first silicon blade to avoid merging by taking both device performance and fabrication limitations into consideration. The silicon blade ends are aligned so as to form an angle $\theta$ with respect to the waveguide direction.

![Schematic of the proposed circular HCG reflector, (a) 3D view, (b) 2D top view.](image)

**Figure 4.1:** Schematic of the proposed circular HCG reflector, (a) 3D view, (b) 2D top view.

### 4.2.2 Device Performance Optimization

To achieve the best device performance, four parameters, namely $W_s$, $W_t$, $\theta$, and number of periods ($N$), are optimized. First of all, a commercial eigenmode solver [162] was used to calculate the effective refractive index of the fundamental transverse-electric (TE) mode in the silicon blades and the SiO2 trenches at 1550 nm. The exact effective refractive index of the circular structure is difficult to calculate; thus a 220-nm-thick slab silicon waveguide was used to calculate the approximate effective index of the blades, which gives $n_s \approx 2.848$, and the refractive index of SiO2 was taken as the approximate effective refractive index of the trenches, which is $n_t \approx 1.440$. Then the period length $\Lambda$ is calculated based on the Bragg grating equation [163].
\[
\Lambda = \frac{m\lambda_c}{2n_{\text{eff}}} = \frac{m\lambda_c}{2(dc \times n_s + (1-dc) \times n_t)},
\]  \quad (4.1)

where \( m \) is an integer which represents the grating order, \( \lambda_c \) is the center wavelength (Bragg wavelength) of the circular HCG and \( n_{\text{eff}} \) is the effective refractive index of the straight silicon/trench interface which is used as an estimation of the effective refractive index of the circular HCG. The effective refractive index \( n_{\text{eff}} \) can be further calculated by the geometric mean between \( n_s \) and \( n_t \) with the duty cycle \( dc \) included. Here \( dc \) is defined as the ratio of \( W_s \) with respect to \( \Lambda \). The first order \( (m = 1) \) period length \( \Lambda \) is calculated to be 361.47 nm when the duty cycle is 50% and is then used as the starting point for the following optimizations.

A commercial three-dimensional finite-difference time-domain (3D-FDTD) simulator [164] was used to optimize the device performance. A fundamental TE mode source input was launched into the waveguide as shown in Figure 4.1(a). During the first optimization process, the silicon blade angle \( \theta \) was fixed at 25° and 6 periods were used while the trench width \( W_t \) and the silicon blade width \( W_s \) were swept. The results of reflectance and operational bandwidth (continuous band where \( R > 90\% \)) are shown in Figure 4.2. The regions with reflectance higher than 95% at 1550 nm and operational bandwidth (continues band where \( R > 90\% \)) broader than 350 nm are marked. It can be seen from Figure 4.2(a) that the reflectance at 1550 nm gradually reduces from the peak region (marked out by the white lines). Similar trend can be observed for the operational bandwidth from Figure 4.3. By taking both parameters into consideration, here \( W_s = 190 \) nm and \( W_t = 170 \) nm \((dc = 53\%) \) are selected to provide sufficient fabrication tolerance.
Figure 4.2: Contour map with simulation results of the circular HCG showing the relationship between the width of silicon blades, the width of gaps and the reflectance at 1.55μm. θ is fixed at 25° and 6 periods are used.

Figure 4.3: Contour map with simulation results of the circular HCG showing the relationship between the width of silicon blades, the width of gaps and the operation bandwidth (R > 90%). θ is fixed at 25° and 6 periods are used.

With the selected silicon blade width and trench width, the impacts of the silicon blade angle θ on the proposed circular HCG reflectance (at 1550 nm) and operational bandwidth were
investigated. The simulation results are shown in Figure 4.4 (number of periods is 6). As we can see, the operational bandwidth drops sharply when $\theta$ is smaller than 20°. This is due to that the ends of circular silicon blades are too close to the input waveguide when $\theta$ is smaller than 20°, thus interferes the propagation mode and produce unexpected loss. Both reflectance and operational bandwidth increase sharply as $\theta$ approaches 25° and start to drop off when $\theta$ is larger than 110°. The decrease for angles greater than 110° is due to that the reflection interfaces are unable to cover the whole wavefront, which leads to leakage at the edge. The peak operational bandwidth of 418 nm is achieved at $\theta = 25^\circ$. Here, $\theta = 28.5^\circ$ is selected as a trade-off between reflection and operational bandwidth. We also noticed that there are some dips in the simulated results, where $\theta = 40^\circ$ for the operation bandwidth and $\theta = 70^\circ$ for the reflectance. The exact reason which causes this problem is still under investigation. But we believe this is more likely due to the device structure change which causes potential interference for the light mode.

![Figure 4.4: Simulated circular HCG reflectance at 1.55 μm and operation bandwidth vs. angle $\theta$ (N=6, $W_s = 190$ nm, and $W_s = 170$ nm).](image-url)
The performance of the proposed circular HCG is affected by the number of grating periods as well. With more periods, higher reflectance can be expected while the cost is less compact device. Simulation results are shown in Figure 4.5. It is clear that when the number of periods is smaller than 6, both reflectance and operational bandwidth increase with the number of periods. When the number of periods reaches 6, and further increase does not significantly improve the device performance. Therefore, the number of periods is chosen to be 6.

![Figure 4.5: Simulated circular HCG reflectance at 1.55 μm and operation bandwidth vs. number of periods (N) (θ = 28.5°, W₁ = 190 nm, and W₂ = 170 nm).](image)

### 4.2.3 Simulation Results with Optimized Parameters

Based on the FDTD simulation results, the optimized circular HCG has a period length of 360 nm with 53% duty cycle. The angle θ is set as 28.5°. Totally 6 periods are used considering both device performance and compactness. With all the optimized parameters, the simulated reflectance spectrum of the circular HCG is shown in Figure 4.6. We can see that the operational bandwidth is broad, ranging from 1283 nm to 1668 nm (over 380 nm). In addition, a peak reflectance of over 97% can be achieved in the C band. The reflectance spectrum with the fundamental transverse-magnetic (TM) mode source is also presented. For the TM mode
operation, the effective index of the silicon blades changes to \( n_{\text{c-TM}} \approx 2.01 \), which consequently shifts the reflection central wavelength to 1250 nm. The lower silicon/trench index difference of TM mode reduces the reflection and the operational bandwidth as well. It can be seen that a \( \text{PER} \) of greater than 17 dB can be maintained throughout the C and L bands.

Figure 4.6: (a) Simulated reflectance spectrums of the circular HCG with TE and TM mode sources and straight bar HCG with TE mode source.

Figure 4.7(a) and Figure 4.7(b) show the electric field distribution of the circular HCG at 1550 nm for TE and TM modes, respectively. Most power is reflected back to the waveguide with the TE mode operation; whilst the TM mode light propagates through the circular HCG without being reflected. The high \( \text{PER} \) effectively reduces mode degeneracy without any other specific designs, especially for broadband tunable laser cavities. In comparison, the reflectance spectrum of a fully etched straight bar HCG reflector is shown as well. The input waveguide, duty cycle, period length and number of periods of the straight structure are the same as the optimized circular HCG. The length of the straight bar is set as 10 μm to avoid power leakage. It can be seen from on the simulation result that the straight structure fails to work due to high diffraction loss as shown in Figure 4.7(c). Therefore, the circular structure is a more efficient approach to significantly improve the reflector performance on the thin SOI platform.
**Figure 4.7:** Circular HCG with (a) TE mode, (b) TM mode, and (c) straight bar HCG with TE mode.

### 4.3 Fabrication of the High Contrast Circular Grating Reflector

#### 4.3.1 Fabrication Process

The fabrication process of the proposed circular HCG reflector is shown in Figure 4.8.

**Figure 4.8:** Fabrication process for the proposed circular HCG. (a) A bare SOI wafer with 220 nm device layer and 2 μm BOX layer; (b) spin coated with 1:2 diluted ZEP520A as EBL resist; (c) patterned with EBL; (d) coated 30 nm chromium using e-beam evaporation; (e) lift off; (f) ICP-RIE; (g) chromium remove using wet etching; (h) PECVD oxide as top cladding.
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The reflector was fabricated using a SOI wafer (220 nm device layer and 2 μm BOX layer). The device was patterned with e-beam lithography (EBL) by using diluted ZEP520A as resist. Cr was deposited as the etching resist using e-beam evaporation. Lift-off process was performed before etching by reactive-ion etching (RIE) with a SF\textsubscript{6}/C\textsubscript{4}F\textsubscript{8} gas mixture. Cr was then removed after etching using wet etching. Finally, 2-μm-thick SiO\textsubscript{2} was deposited on top of the chip as the top-cladding by Plasma-enhanced chemical vapor deposition (PECVD). The SEM image of the fabricated circular HCG (without top-cladding) is shown in Figure 4.9. 2 nm Gold is coated on the sample to avoid charging. The footprint of the optimized device was 4.03 × 4.32 μm\textsuperscript{2}. Based on the scanning electron microscope (SEM) measurements, the fabrication error was estimated to be about ± 5 nm.

![SEM image of the fabricated circular HCG](image)

*Figure 4.9: SEM image of the fabricated circular HCG, 2 nm gold was coated to avoid SEM charging problem.*

4.4 **EXPERIMENT DEMONSTRATION**

4.4.1 **Experimental Setup**

The performance of the fabricated circular HCG was characterized experimentally using the setup shown in Figure 4.10. An ASE light source followed by a polarization beam splitter
(PBS) was used to generate single polarized light. A manual polarization controller (PC) was then used to switch the polarization of the light injected into the chip between TE and TM modes. A circulator was employed to measure the back-reflected signal. In the forward direction, light propagated from port 1 to port 2 of the circulator before being injected into the chip. In the backward direction, the back-reflected signal was characterized by an optical spectrum analyser (OSA) connected to the port 3 of circulator.

![Figure 4.10: (a)Schematic of the experiment setup with (b) SEM image of the fabricated circular HCG. ASE: ASE noise source; PBS: polarization beam splitter; PC: polarization controller; OSA: optical spectrum analyser.](image)

### 4.4.2 Measured Reflector Performance

The measured reflectance spectrums of the circular HCG reflectors are shown in Figure 4.11 and Figure 4.12. Devices have the same period length \( \Lambda = 360 \text{ nm} \), but with varying combinations of duty cycle and silicon blade angle \( \theta \) were fabricated and characterized. Figure 4.11 shows the reflectance variation with different duty cycles whilst \( \theta = 28.5^\circ \). Some data points are over 100% reflection due to inevitable measurement/reference errors. To reduce the impact of these errors, the average reflectance (shown in Table 4.1 and Table 4.2) is taken to characterize the devices. As shown in Table 4.1, The circular HCGs, with duty cycles of 53% and 60%, perform similarly. An average reflection of 94.15% and 93.94% can be respectively achieved. Due to measurement limitations, only the reflections from 1525 nm to 1610 nm were
measured, and over the entire measured wavelength range, the reflectance is higher than 90%. When the duty cycle is reduced to 40%, the reflectance is comparable between 1525 nm to 1550 nm but then begins to drop off. The trend of the device performance change observed in the experiments agrees well with the simulation results as shown in Figure 4.2.

![Graph](image)

*Figure 4.11: Measured reflectance spectrums of the circular HCGs with TE polarized light with different duty cycles (when θ = 28.5°). The period length is fixed at 360 nm.*

<table>
<thead>
<tr>
<th>duty cycle</th>
<th>Reflectance</th>
</tr>
</thead>
<tbody>
<tr>
<td>dc = 53%</td>
<td>94.15%</td>
</tr>
<tr>
<td>dc = 40%</td>
<td>93.94%</td>
</tr>
<tr>
<td>dc = 60%</td>
<td>86.81%</td>
</tr>
</tbody>
</table>

*Table 4.1: Measured average reflectance of the proposed circular HCG with dc = 53%, 40%, and 60%, when θ = 28.5°.*

The impact of the silicon blade angle θ on the device performance was characterized, and is illustrated in Figure 4.12. The corresponding average reflectance of the reflector is shown in Table 4.2. Here the duty cycle was fixed at 53% while the silicon blade angle θ was varied to 90° and 135°. Compare to the optimized parameter θ = 28.5°, the average reflectance at θ = 90° slightly decreases to 93.3%. However, when θ is increased to 135°, the reflectance is lower with an average reflectance of 86.71%. The measured impact of θ matches our simulation results shown in Figure 4.4.
Figure 4.12: Measured reflectance spectrums of the circular HCGs with TE polarized light with different $\theta$ (when dc = 53%). The period length is fixed at 360 nm.

<table>
<thead>
<tr>
<th>$\theta$</th>
<th>Reflectance</th>
</tr>
</thead>
<tbody>
<tr>
<td>28.5°</td>
<td>94.15%</td>
</tr>
<tr>
<td>90°</td>
<td>93.3%</td>
</tr>
<tr>
<td>135°</td>
<td>86.71%</td>
</tr>
</tbody>
</table>

Table 4.2: Measured average reflectance of the proposed circular HCG with $\theta = 28.5^\circ$, $90^\circ$, and $135^\circ$, when dc = 53%.

4.4.3 Polarization Extinction Ratio Characteristics

The PER of the circular HCG was measured and the reflectance of both TE and TM polarized light are shown in Figure 4.13. The TM polarized light suffers much higher loss compare to the TE polarized light. In addition, the PER is always larger than 13 dB across the measured wavelength band, which is slightly lower than the simulation results shown in Figure 4.6. This is mainly due to fabrication errors and measurement equipment extinction ratio limits.
Figure 4.13: Measured reflectance of the circular HCG with both TE (blue) and TM polarized (red) light.
5 Polarization Beam Splitter Based on Silicon Nitride Platform

5.1 Overview

Silicon photonics technology has been widely studied during the last decade due to its promising future to break the bottleneck of short range on-chip interconnects [165-167]. Integrated photonic devices on the silicon platform with compact size, high efficiency and low cost have been well developed using the CMOS-compatible processes [168, 169]. However, realizing three-dimensional (3D) structures is still challenging, especially based on the crystalline silicon. On the other hand, silicon nitride (SiN) are attracting more attention due to its easy deposition using either low-pressure chemical vapor deposition (LPCVD) or Plasma-enhanced chemical vapor deposition (PECVD), which provides better flexibility for complicated 3D structures [170-171]. In addition, due to the low refractive index, SiN waveguides exhibit much lower scattering loss from the sidewall roughness compared to silicon waveguides, which leads to higher fabrication tolerance [173-175]. On the SiN platform, integrated devices such as ring resonators with high quality factor ($Q$) have been demonstrated [176-178]. However, due to the low birefringence property, it is challenging to realize other devices like polarization beam splitters (PBS) on the SiN platform, since normally large effective index difference ($\Delta n_{\text{eff}}$) between TE and TM polarized lights is required.

On the silicon-on-insulator (SOI) platform, directional coupler [179-181] and multimode interferometer (MMI) [182, 183] based PBSs with low loss, high extinction ratio (ER) and wide bandwidth have been demonstrated. However, these kinds of devices become considerably long on the SiN platform due to the reduction in $\Delta n_{\text{eff}}$
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between the fundamental TE and TM polarizations. In addition, realizing mode evolution based [184] and mode coupling based [185, 186] PBSs on SiN is difficult as well, because of the small $\Delta n_{eff}$ between fundamental modes and higher order modes. On the other hand, the Mach-Zehnder interferometer (MZI) based structure is a promising approach to realize polarization splitting devices even with low index material. In [187], a MZI based silicon PBS has been proposed and the device performance has been limited by low fabrication tolerance. With the low index SiN material, the fabrication tolerance can be significantly improved and such devices have been demonstrated [188]. However, the SiN PBS had a length of 1 mm (250-μm-long phase control section), which leads to dense integration challenges.

In Section 5.2, a more compact 2×2 MZI based SiN PBS is proposed [189]. Two polarization independent asymmetric 3-dB couplers with an ultra-short parallel-coupling length of 1.2 μm are designed to reduce the device length. The total device dimension is only 5.6 μm × 113 μm (including s-bends) with a 27.7-μm-long phase control section. The fabrication processes are introduced in Section 5.3. In Section 5.4, we present the measurement results of the fabricated PBS. It achieves a minimum insertion loss of 0.13 dB and 0.34 dB for TE and TM polarized lights, respectively. The ER is higher than 20 dB throughout the entire measured band from 1530 nm to 1610 nm for the TE polarization. For the TM polarization, an ER of > 20 dB can be maintained over the C band. In Section 5.5, an optimized design is proposed to improve the PBS performance. The optimized PBS is less sensitive to wavelength change with TM polarization operation.

5.2 NEW POLARIZATION BEAM SPLITTER ON SILICON NITRIDE PLATFORM

5.2.1 Structure of the Proposed Polarization Beam Splitter

The schematic of proposed SiN 2×2 PBS is shown in Figure 5.1(a). The device was designed with 600-nm-thick SiN device layer on top of 2-μm-thick SiO2 to reduce the required low-loss bending radius. The thickness of the top SiO2 cladding is 2 μm as well. The PBS consists of two identical asymmetric directional couplers at the input (Port 1 and Port 2) and output (Port 3 and Port 4), and two arms with different widths as the phase control section to provide different phase changes for TE and TM
polarizations. The asymmetric directional couplers are optimized to achieve the same 3 dB coupling central wavelength at 1550 nm for both polarizations, to reduce the polarization dependence and simplify the phase control section design. The fabricated SiN layer has a refractive index of \( n \approx 2.125 \) based on ellipsometry measurements, which is used in the device design.

As shown in Figure 5.1(b) and Figure 5.1(c), the upper waveguide of asymmetric coupler has a width of \( W_1 = 600 \) nm and the lower waveguide has a width of \( W_2 = 540 \) nm. The s-bends have a bending radius of \( R_s = 60 \) μm and an angle of \( \theta = 10^\circ \), and they are used as inputs and outputs of the couplers. The parameters are optimized to reduce the bending loss to lower than 0.015 dB per s-bend.

**5.2.2 Structure of the Asymmetric 3 dB Coupler**

For the asymmetric coupling region, the gap between the upper and lower arm is \( W_g = 380 \) nm and the parallel-coupling length is \( L_c = 1.2 \) μm. The asymmetric coupler is optimized to have the same parallel-coupling length for both TE and TM polarized lights using a commercial eigenmode solver [162] and a three-dimensional finite-difference time-domain (3D FDTD) simulator [164]. \( W_1 \) is fixed at 600 nm to simplify the design while \( W_2 \) and \( W_g \) are varied to find the optimized solution. The eigenmode solver is first used to calculate the supermode index.
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matching condition for the coupler. The parameters are then further optimized by 3D FDTD simulations due to the residual coupling in s-bends, with both device compactness and polarization independent operation being considered simultaneously. The simulated transmission spectrums of the optimized coupler for TE and TM polarizations are shown in Figure 5.2 and Figure 5.3. Due to the supermode index matching, the asymmetric 3 dB coupler shows polarization independent performance, where TE and TM polarized lights have the same 3 dB coupling wavelength at 1550 nm. Compared with conventional polarization independent directional couplers and 3 dB MMI power splitters, the asymmetric directional coupler based solution eliminates the polarization dependence in an ultra-short parallel-coupling length of only 1.2 μm.

Figure 5.2: Simulated transmission spectrums of the asymmetric coupler with TE and TM polarized sources, respectively, using port 1 as input.
5.2.3 Phase Control Section Design

In the phase control section, the upper waveguide is fixed at $W_1 = 600 \text{ nm}$ to simplify the design. The lower waveguide consists of two tapers with fixed length of $L_t = 10 \mu\text{m}$ to widen and narrow the waveguide, and a strip waveguide with width $W_3$ and length $L_1$. In order to separate TE and TM polarized lights, the phase change difference $\Delta \phi$ from point (a) to point (b) (as shown in Figure 5.1(c)) between the upper and lower arms should be $m\pi$ and $(m \pm 2n + 1)\pi$ for TE and TM polarizations, respectively ($m$ and $n$ are integers). The phase change difference of each pair of $s$-bends for TE and TM polarizations can be calculated using

$$\Delta \phi_{s\text{-bend--TE}} = 2\pi \left( n_{2s\text{-TE}} - n_{1s\text{-TE}} \right) L_s / \lambda_0,$$  

and

$$\Delta \phi_{s\text{-bend--TM}} = 2\pi \left( n_{2s\text{-TM}} - n_{1s\text{-TM}} \right) L_s / \lambda_0,$$

where $n_{1s}$ and $n_{2s}$ are the bending effective index of the upper and lower $s$-bends, which are 1.709 and 1.674 for the TE polarization, and 1.710 and 1.688 for the TM polarization.
polarization based on eigenmode simulation; \( L_\text{s} \) is the length of the s-bend, which is 20.94 \( \mu \text{m} \); and \( \lambda_0 = 1550 \text{ nm} \) is the central wavelength. The phase difference due to s-bends can be calculated to be \(-0.96\pi \) for the TE polarization and \(-0.59\pi \) for the TM polarization.

Then the total phase change from point (a) to point (b) can be calculated by

\[
\Delta \phi = 2\Delta \phi_{\text{s-bend}} + 2\Delta \phi_{\text{taper}} + \Delta \phi_{W_3-W_1},
\]

(5.3)

where \( \Delta \phi_{\text{taper}} \) is the phase difference due to tapers in the phase control section, and \( \Delta \phi_{W_3-W_1} \) is the phase difference between the lower waveguide (\( W_3 \)) and the upper waveguide (\( W_1 \)). The upper waveguide width \( W_3 \) affects both \( \Delta \phi_{\text{taper}} \) and \( \Delta \phi_{W_3-W_1} \). The effective index of both polarizations with respect to the waveguide width are shown in Figure 5.4(a) with \( W_1, W_2 \) and \( W_3 \) highlighted to calculate the optimized parameters. Since linear tapers are used, the phase difference due to each taper is calculated by

\[
\Delta \phi_{\text{taper}} = 2\pi \frac{(n_i - n_t) L_1}{\lambda_0},
\]

(5.4)

where \( n_i \) is the taper effective index. From Figure 5.5, it is clear that the effective index change with the waveguide width is nonlinear. Although it is difficult to calculate the exact value of \( n_i \), here \( n_i \) is estimated by taking the weighted mean of the values of the marked points from 550 nm in Figure 5.4 which is effective index of every 50 nm width variation segment. Furthermore, the phase change difference of the waveguide part can be obtained by

\[
\Delta \phi_{W_3-W_1} = 2\pi \frac{(n_3 - n_1) L_1}{\lambda_0},
\]

(5.5)

where \( n_3 \) is the effective index of the strip waveguide with width \( W_3 \). By combining Equation (5.3 - 5.5), the relationship between the waveguide width \( W_3 \) and the length \( L_1 \) to achieve different phase differences between TE and TM polarizations can be calculated and are shown in Figure 5.5. It can be seen that only the lines satisfying \( \Delta \phi_{\text{TE}} = 3\pi \) and \( \Delta \phi_{\text{TM}} = 2\pi \) overlaps substantially, which are capable of the PBS function.
Considering the fabrication tolerance, $W_3 = 1.5 \, \mu m$ and $L_1 = 7.7 \, \mu m$ are selected. More compact design can be achieved when wider $W_3$ is used at the cost of higher insertion loss at the taper part and lower fabrication tolerance on waveguide width.

![Simulated relationship between the strip SiN waveguide width and the corresponding effective index with TE and TM polarized lights, respectively.](image)

**Figure 5.4:** Simulated relationship between the strip SiN waveguide width and the corresponding effective index with TE and TM polarized lights, respectively.

![Calculated relationship between the phase control section waveguide width $W_3$ and length $L_1$ by required phase change of TE and TM modes, respectively.](image)

**Figure 5.5:** Calculated relationship between the phase control section waveguide width $W_3$ and length $L_1$ by required phase change of TE and TM modes, respectively.
5.3 **Fabrication of the High Contrast Circular Grating Reflector**

5.3.1 **Fabrication Process**

The fabrication process is described in Figure 5.6. The process starts with a silicon handle wafer, 2-μm-thick thermal SiO$_2$ was deposited as the bottom cladding layer. 600-nm-thick SiN device layer was then deposited using LPCVD. The device was patterned with e-beam lithography (EBL) by using diluted ZEP520A as resist. Cr was then deposited as the etching resist using e-beam evaporation. Lift-off process was performed before reactive-ion etching (RIE) with a CHF$_3$/O$_2$ gas mixture. Cr was then removed and SiO$_2$ was deposited on top of the chip as the top-cladding by PECVD. The optical microscope image of the fabricated PBS is shown in Figure 5.7(a) and the scanning electron microscope (SEM) image of the SiN waveguide (cross section) is shown in Figure 5.7(b). The waveguide sidewall is almost vertical (less than 1° error) after 600 nm SiN etching.

![Fabrication process for the proposed polarization beam splitter.](image)

Figure 5.6: Fabrication process for the proposed polarization beam splitter. (a) Start with a P type bare silicon wafer; (b) deposited 3-μm-thick thermal oxide (c) deposited 600 nm silicon nitride layer using LPCVD; (d) spin coated with 1:2 diluted ZEP520A as EBL resist; (e) patterned with EBL; (f) coated 60 nm chromium using e-beam evaporation; (g) lift off; (h) ICP-RIE; (i) chromium remove using wet etching; (j) PECVD oxide as top cladding.
Fig. 5.7: (a) Optical microscope image of the proposed 2×2 PBS. (b) SEM image of the SiN waveguide (cross section view).

5.4 EXPERIMENT DEMONSTRATION

5.4.1 Experimental Setup

The performance of fabricated SiN 2×2 PBS was experimentally characterized using the setup shown in Figure 4.8. An ASE source followed by a polarizer was used to generate a broadband single polarized input signal. The polarization of the signal was switched between TE and TM polarizations using a polarization controller (PC). The signal was injected into the chip through a lensed fiber. The output signal was collected using another lensed fiber and then characterized by an optical spectrum analyzer (OSA). Considering the relatively thick SiN device layer, the waveguide width was narrowed to 200 nm at the edge of the chip through a 100-μm-long taper which served as a spot size converter (SSC) to couple the signal between the lensed fibers and the chip.

Figure 5.8: Schematic of the measurement system setup. ASE: amplified spontaneous emission source; PC: polarization controller; OSA: optical spectrum analyser.
5.4.2 Measured Reflector Performance

The measured transmission spectrums of TE and TM polarized input signals are shown in Figure 5.9 and Figure 5.10, respectively. In order to characterize the performance of the proposed PBS, reference waveguides with 800 nm width were fabricated on the same chip, which is the same as the transmission waveguide of the PBS. Multiple measurements were taken and the average tested results for corresponding polarizations were used for device performance normalization to minimize the measurement error. The references are used to eliminate the influence from the fiber-to-chip coupling loss and the polarization dependent transmission waveguide propagation loss across the chip. In the PBS, 100-μm-long tapers are used to narrow the transmission waveguide from 800 nm to the input waveguide widths which are not include in the reference waveguide since the loss of the 100 μm taper is very low and negligible (lower than 0.005dB based on simulation result). It can be seen that the device has consistent performance regardless of the input port (Port 1 or Port 2). It is clear that the TE polarized light propagates out of the chip from the through ports while the TM polarized light propagates to the cross ports, and the PBS functions is successfully achieved.

![Figure 5.9: Measured transmission spectrum of the proposed PBS with TE polarized source.](image)

Figure 5.9: Measured transmission spectrum of the proposed PBS with TE polarized source.
Figure 5.10: Measured transmission spectrum of the proposed PBS with TM polarized source.

In Figure 5.11 and Figure 5.12, the measured insertion loss of the PBS is compared with the simulation results. In general, the measurement results agree well with the simulation results. The measurement error from experiment setup and fiber-to-chip alignment is around ±0.15 dB. The PBS has a minimum insertion loss of 0.13 dB for the TE polarization, which is close to the simulation results, whilst the minimum insertion loss of the TM polarized light is 0.34 dB, which is slightly higher compare to simulations. The excess loss mainly comes from the s-bends bending loss (around 0.06 dB for both polarizations based on the simulation results) and fabrication errors which lead to the central wavelength mismatch between the 3dB asymmetric coupler and the phase control section. In addition, it can be seen that there is about 0.2 dB difference on the output power when Port 1 or Port 2 is used as the input. This is mainly due to measurement errors, including the alignment error and setup stability.
Figure 5.11: Insertion loss of the proposed PBS (measured and simulated) when Port 1 or Port 2 is used as the input with TE polarized source.

Figure 5.12: Insertion loss of the proposed PBS (measured and simulated) when Port 1 or Port 2 is used as the input with TM polarized source.

The ER of the PBS is calculated as the power ratio between outputs (Port 3 and Port 4) and the results are shown in Figure 5.13 and Figure 5.14. For the TE polarized light, the ER is higher than 20 dB throughout the entire measured band from 1530 nm to 1610 nm.
Although the ER for the TM polarized light is more wavelength dependent, it is still higher than 20 dB over the entire C band before it eventually decreases at longer wavelengths. The measurement results agree with the simulation results as well.

**Figure 5.13:** Extinction ratio of the proposed PBS (measured and simulated) when Port 1 or Port 2 is used as the input with TE polarized source.

**Figure 5.14:** Extinction ratio of the proposed PBS (measured and simulated) when Port 1 or Port 2 is used as the input with TM polarized source.
5.5 FUTURE IMPROVEMENT

In the previous section, we proposed a high efficient, broadband and compact 2×2 polarization beam splitter on silicon nitride platform. However, the proposed device shows strong wavelength selectivity for TM mode operation. In this section, we further discuss the reason that causes this problem, and propose a possible solution to improve the TM mode operation performance.

5.5.1 Analysis of the 2×2 Polarization Beam Splitter Design

Firstly, in order to get an insight view of the PBS performance, we need to derive the transmission equations for both outputs. In Figure 5.15, we define the input electric field as $E_{in}$. For the asymmetric coupler section, the through coupling ratio is $k$, and correspondingly, the cross-coupling ratio is $1-k$. Assume both the propagation loss and coupling loss are zero, then the output electric field equations can be derived as:

$$E_{a_{-out}} = kE_{in} + (1-k)e^{-j\frac{\pi}{2} + \Delta \phi}E_{in}$$  \hspace{1cm} (5.6)

and

$$E_{b_{-out}} = \sqrt{k(1-k)}e^{-j\frac{\pi}{2}}E_{in} + \sqrt{k(1-k)}e^{-j\frac{\pi}{2} + \Delta \phi}E_{in}$$  \hspace{1cm} (5.7)

where $\Delta \phi$ is the phase difference between the upper and lower arms after light travels through the PBS.
Figure 5.15: Schematic of the previous 2×2 PBS design, 1-k is the cross coupling ratio for the asymmetric 3 dB coupler.

Then we can further derive the transmission power both outputs as:

\[ P_{a_{\text{out}}} = [k^2 + (1-k)^2] E_{\text{in}}^2 + 2k(1-k)E_{\text{in}}^2 \cdot \cos(\pi + \Delta\phi) \]  
(5.8)

and

\[ P_{b_{\text{out}}} = 2k(1-k)E_{\text{in}}^2 + 2k(1-k)E_{\text{in}}^2 \cdot \cos(\Delta\phi) \]  
(5.9)

Obviously, both the coupling ratio \(k\) and the phase change \(\Delta\phi\) are wavelength dependent. The trend of \(k\) can be seen from Figure 5.2 and Figure 5.3. Clearly, only when \(k = 0.5\) (which happens at the central wavelength of the PBS in this design), the output power at the through port can be zero with appropriate value of the phase change \(\Delta\phi\). If we use port 1 as the input, then the through coupling ratio \(k\) is around 0.41 at 1600 nm wavelength, based on the simulation results in Figure 5.2. Then the through port output power is

\[ P_{a_{\text{out}}} = 0.516E_{\text{in}}^2 + 0.483E_{\text{in}}^2 \cdot \cos(\pi + \Delta\phi) \]  
(5.10)

The minimum value can be achieved from equation (5.10) is \(P_{a_{\text{out}}} = 0.33\) (when \(\Delta\phi = 2m\pi\)), which is around -14.8 dB (at 1600 nm wavelength). This calculation result agrees well with the simulation result in Figure 5.14, where TM mode operation uses the cross port as the output.

On the other hand, the phase change \(\Delta\phi\) can be calculated as:

\[ \Delta\phi = \frac{2\pi \cdot \Delta n}{\lambda} L \]  
(5.11)

where \(\Delta n\) is the effective index difference between the upper and lower arms, and \(L\) is the corresponding length of each section. Since \(\Delta n\) can be expressed as a linear function
with wavelength $\lambda$ (within a relatively narrow wavelength range $< 100$ nm), and $L$ is a constant for a specific design, Equation (5.11) can be further simplified as:

$$\Delta \phi = a + \frac{b}{\lambda} \quad (5.12)$$

where $a$ and $b$ are the constants depend on the chosen upper and lower waveguide width. The relationship between $\Delta n$ and $\lambda$ can be calculated by using the eigenmode solver. With the calculated effective index of a certain upper and lower waveguide width pair at different wavelength and the length of each arm, we can use a linear regression fit line to get the function of $\Delta n$, and then use this function to calculate $a$ and $b$.

### 5.5.2 Proposed Optimized Design

For the PBS design, the waveguide width and length of each section can be determined by using the method shown in Section 5.2.3. Therefore, the phase change $\Delta \phi$ is determined during this process. In addition, the previous calculation shows that the coupling ratio $k$ has a more significant impact on the PBS wavelength dependent performance. In order to optimized this issue, a 1×2 splitter is used to replace the asymmetric 3 dB coupler at the input. The proposed optimize solution is shown in Figure 5.16.

![Figure 5.16: Schematic of the optimized PBS design.](image)

For the optimized PBS, assume the splitter has a perfect 50:50 splitting ratio with no loss, the output power can be derived as:

$$P_{\text{out}} = \frac{1}{2} E_{\text{in}}^2 + \sqrt{k(1-k)}E_{\text{in}}^2 \cdot \cos\left(\frac{\pi}{2} + \Delta \phi\right) \quad (5.13)$$

and
By using this design, the insertion loss for TE mode operation would be slightly higher compare to the previous design. However, extinction ratio of TM mode operation would be less wavelength dependent. Using the previous coupling ratio \( k = 0.41 \) at 1600 nm and again, assume the idea case with no coupling loss and propagation loss, we can get:

\[
P_{a_{\text{out}}} = \frac{1}{2} E_{in}^2 + \sqrt{k(1-k)} E_{in}^2 \cdot \cos(\frac{\pi}{2} - \Delta \phi)
\]  

(5.14)

From Equation (5.15), we can get the minimum value of \( P_{a_{\text{out}}} \) as 0.008, which gives the extinction ratio of TM mode operation at 1600 nm is around -20.9 dB.

The performance of the optimized PBS is compared with the previous design by using 3D FDTD simulation. In Figure 5.17, the simulated insertion loss of both TE and TM mode operations are shown. As we can see, the insertion loss of TE mode is about 0.1 dB higher compare to the previous design. For TM mode operation, the insertion loss of the previous design quickly drops after the central wavelength (1550 nm). But for the optimized design, it shows relatively flat spectrum and the maximum insertion loss is only -0.21 dB. The results agree well with the calculation using Equation (5.13) and Equation (5.14).

![Figure 5.17: Simulated insertion loss of the optimized PBS compare to the previous design.](image)
The simulated extinction ratio for the optimized design and previous design are also compared and presented in Figure 5.18. The extinction ratio for TE mode is more wavelength dependent compare to the previous design, but both the minimum and maximum extinction ratio are improved. For TM mode, the difference between the minimum and maximum extinction ratio is reduced to 9 dB compare to 18 dB of the previous design. The results agree well with the theoretical calculation and show that the wavelength dependent operation for TM mode has been improved.

![Figure 5.18: Simulated extinction ratio of the optimized PBS compare to the previous design.](image)

5.6 SUMMARY

In this chapter, a 2x2 PBS based on SiN has been proposed and experimentally demonstrated. Two polarization independent asymmetric 3-dB directional couplers with ultra-short parallel-coupling length of 1.2 µm and a phase control section with only 27.7 µm length have been used in the proposed PBS. The proposed device has been fabricated and measurement results have shown that the PBS has a minimum insertion loss of 0.13 dB and 0.34 dB for TE and TM polarized lights, respectively. It has also been shown that the ER is higher than 20 dB for the TE polarization throughout the
measured band from 1530 nm to 1610 nm, and over the entire C band for the TM polarization. The measurement results show a good agreement with the simulation results. In addition, a possible solution was proposed and discussed to improve the wavelength dependent problem of the TM mode operation. By replacing the input asymmetric coupler with a 3-dB splitter, the difference between the minimum and maximum extinction ratio is reduced to 9 dB compare to 18 dB of the previous design for the TM mode operation. The maximum insertion in the working bandwidth is only -0.21 dB based on the simulation results. However, the cost is additional 0.1 dB insertion loss for the TE mode operation.
6 Interlayer Coupler for Silicon Photonic Integrated Circuits

6.1 OVERVIEW

The silicon photonics technology is promising to break the bottleneck of conventional data transmission systems. Optical devices such as waveguides, filters and modulators have been realized on silicon-on-insulator (SOI) substrates with reliable performance [190]. However, this type of single layer integration scheme limits the maximum possible integration density. Therefore, stacked multi-layer silicon photonic large-scale integrated circuits (LSIs) are proposed and investigated. For multi-layer silicon photonics integration based on the SOI platform, hydrogenated amorphous silicon (a-Si:H or a-Si) has been widely studied, mainly due to its low absorption loss and ultra-fast nonlinear effects [191, 192]. In addition, the fabrication of a-Si based three-dimensional (3D) silicon photonic integrated circuits is comparatively simple, since a-Si layers can be directly deposited.

For 3D integrated silicon photonic circuits, signal coupling between layers is required. Recently, several vertical coupling methods have been proposed and studied [193, 194]. However, the directional coupler based design [193-195] can only support 200 nm gap between the two layers or require very thin device layer, which results in optical isolation issues after the vertical coupler. On the other hand, the vertical coupling solution based on grating coupler [196, 197] can support a much larger gap. Nevertheless, the efficiency is limited to only 22%. Furthermore, both methods are polarization dependent. Therefore, a polarization independent vertical coupler with high efficiency and sufficient optical isolation is highly demanded.

On the silicon nitride platform, inverse tapers were used to realized ultra-low coupling
loss [198]. However, relatively thin device layer was used (200 nm), which requires wide waveguide to reduce interlayer crosstalk and reduces the total chip density. Single mode operation cannot be guaranteed for such wide waveguide. In order to improve the device compactness, wide interlayer gap and relative thick device layer are required. This is still challenging on the silicon nitride platform with its low material index.

In this chapter, we propose two vertical directional couplers for low loss inter-layer signal transfer. Both coupler structures are simple, polarization independent, and compatible with deep ultraviolet (UV) lithography. In Section 6.2, a coupler on the silicon platform is introduced. The simulation results show that the coupling loss is only 0.29 dB for the TE mode and 0.2 dB for the TM mode. In addition, the proposed device has a broad operation bandwidth, where the 1 dB bandwidth is 193 nm for the TE mode and 185 nm for the TM mode. In Section 6.3, we introduce an optimized coupling method for the silicon nitride platform. Similarly, the FDTD simulation results and fabrication tolerance are discussed.

6.2 DIRECTIONAL COUPLER BASED VERTICAL COUPLER ON SILICON

6.2.1 Device Structure

Firstly, we recall Equation (2.1) [195] in Section 2.2 as Equation (6.1):

\[
\kappa = \frac{2k_x^2 k_{xg} e^{-k_{xg}g}}{\beta w (k_{xg}^2 + k_{xc}^2)}
\]  

(6.1)

where \( \kappa \) is the coupling coefficient, \( \beta \) is the propagation constant along the waveguide, \( w \) is the waveguide width, \( g \) is the gap between two waveguides, \( k_{xg} \) is the \( x \)-directed (between the waveguides) decay constant and \( k_{xc} \) is \( x \)-directed propagation constant.

From Equation (2.1), we can see that the waveguide spacing \( g \) and the \( x \)-directed decay constant \( k_{xg} \) have strong impact on the coupling coefficient. Even small change of the waveguide spacing will cause the shift of central operation wavelength. The sensitivity increases with smaller required waveguide spacing. In addition, the directional coupler normally works polarization dependently without specific design. Large waveguide
spacing will reduce the impact from spacing error, but will reduce the decay constant, and therefore, the coupling coefficient. It normally requires longer coupling length to achieve critical coupling with large spacing. The critical coupling length can be calculated using Equation (2.2) (recall as Equation 6.2 here).

\[ L_c = \frac{\lambda}{2(n_{\text{even}} - n_{\text{odd}})} \]  

(6.2)

where \( \lambda \) is the central wavelength, \( n_{\text{even}} \) and \( n_{\text{odd}} \) are the even and odd supermode effective index, which can be easily calculated using an eigenmode solver. Based on Equation (6.2), we can see that for a fixed waveguide spacing, we can get different critical coupling length by using different waveguide width. In Figure 6.1, we present the supermode effective index change and the required critical coupling length requirement with different waveguide width and fixed 1 \( \mu \text{m} \) waveguide spacing. The supermode effective index \( (n_{\text{eff}} = n_{\text{even}} - n_{\text{odd}}) \) were calculated by using a commercial eigenmode solver [196] and the critical coupling length is calculated based on Equation (6.2).

![Figure 6.1: TE and TM modes (a) supermode effective index; and (b) critical coupling lengths, with varied waveguide width, using fixed 1 \( \mu \text{m} \) waveguide spacing.](image)

From the simulation results in Figure 6.1, we can see the supermode effective index decreases with wider waveguide, and hence, the critical coupling length increases with
the increasing of waveguide width. The main reason is that more power is squeezed outside the waveguide core to the free space, so it increases the $x$-directed decay constant $k_x$ (between the waveguides). The simulated electric field TE mode profile of a silicon waveguide with 220 nm thick device layer can be shown in Figure 6.2. Clearly, most power is distributed outside the silicon waveguide core with waveguide width smaller than 250 nm. For the TM mode, more power is distributed outside the waveguide even with large waveguide width. Therefore, the supermode effective index is flatter along the waveguide width change and higher at larger waveguide width. The simulated electric field TM mode profile is not shown in this section (see Figure 2.4).

![Electric field TE mode profile of a silicon waveguide with 220 nm thick device layer and varied waveguide widths.](image)

By using this property, it is possible to design a vertical coupler with short coupling length but remain low crosstalk for parallel waveguides in different layers. In addition, it is also feasible to make the device support polarization independent operation by choosing appropriate waveguide width (the cross-point of the TE and TM mode supermode effective index based on Equation (6.2)).

The structure of the proposed vertical coupler is shown in Figure 6.3. The lower layer is the c-Si of SOI wafer and the upper layer is deposited a-Si. The cladding of coupler is SiO$_2$. The vertical coupler consists of silicon input and output waveguides, tapers and a directional coupling region.
In the design, the thickness of both layers is $H_1 = H_2 = 220$ nm, and the input and output waveguides have a width of 460 nm ($W_{sw1} = W_{sw2} = 460$ nm). Tapers are used to change the waveguide width between $W_{sw1}$ and $W_{t1}$ (or $W_{sw2}$ and $W_{t2}$). The length of tapers is 20 μm ($L_{t1} = L_{t2} = 20$ μm), which is relatively long to avoid substantial losses. In the coupling region, the waveguides have constant width and the coupling length is defined as $L_c$. In addition, the vertical spacing $H_g$ between two silicon layers should be large enough to suppress inter-layer interferences. Here, $H_g = 1$ μm is chosen for the following device characterization. 3D finite-difference time-domain (FDTD) simulations were carried out to study the performance of our vertical inter-layer coupler design. The refractive index of c-Si and SiO$_2$ are $n_{c-Si} = 3.474$ and $n_{cladding} = 1.44$, respectively. Typically, the refractive index of a-Si varies from 3.3 to 3.7 depending on the fabrication process [191, 193, 194], and here $n_{a-Si} = 3.5$ is used in the simulation. Since the indices of c-Si and a-Si are close, we use the same waveguide width for the two layers in the coupling region. A relatively long coupling length ($L_c = 60$ μm) is used to simulate the coupler efficiency at 1.55 μm wavelength. When the waveguide width is 180 nm, 200 nm, 220 nm, or 240 nm, the simulated power profiles are shown in Figure 6.4.
Figure 6.4: Simulated power profile of the coupling region at 1.55 μm wavelength with $W_{t1} = W_{t2} =$, (a) 180 nm; (b) 200 nm; (c) 220 nm; (d) 240 nm. In this case, $L_c = 60 \mu m$ is used.

It is clear that when the waveguide width is smaller than 220 nm, the proposed vertical coupler has almost constant cross-over coupling length, since the effective index changes of the waveguides are inconspicuous. In addition, we can see that the colour which indicates the power intensity in the figure is lighter for waveguide with smaller than 200 nm. This suggests that the total power loss is considerably high when the waveguide width is small than 200 nm, and this is mainly due to the weak mode confinement and large diffraction loss.

It was found by an eigenmode solver that when the waveguide width is about 220 nm, the TE and TM modes have similar effective refractive indices (around 1.51). As a result, the coupling region waveguide width is chosen to be 220 nm and the coupling length is set at 24 μm in this design.

### 6.2.2 Simulation Results and Fabrication Tolerance Discussion

The performance of the proposed silicon integrated vertical coupler was simulated based on 3D-FDTD method, and the results are shown in Figure 6.5. It is clear that the maximum coupling efficiency is 93.6% (0.29 dB loss) for the TE mode and 95.5% (0.2 dB loss) for the TM mode. Furthermore, the 1 dB bandwidth for both modes are over 180 nm, which covers both the C band and the L band.
The fabrication tolerance is also studied in terms of the misalignment in the $x$ and $y$ directions (as defined in Figure 6.3), and the impact of a-Si refractive index variation. The results are shown in Figure 6.6(a) to Figure 6.6(c), respectively. It can be seen from Figure 6.6(a) that impacts of the $x$-direction misalignment ($\Delta x$) are negligible, and this can be mainly attributed to the long coupling length used. On the other hand, the impacts of the $y$-direction misalignment ($\Delta y$) are more obvious since it changes the gap $H_g$, as shown in Figure 6.6(b). It should be noticed that the impacts of $\Delta y$ are relatively low when $\Delta y \leq 400$ nm, and such alignment accuracy can be achieved by most alignment technologies. In addition, it is clear from Figure 6.6(c), that the device performance is more sensitive to a-Si deposition process when $n_{a\text{-Si}} > 3.6$. It indicates that precise refractive index measurement of the deposited a-Si is necessary to ensure the device satisfy the effective index matching condition in the coupling region. For small refractive index variation, the proposed device still has an efficiency of $>80\%$. 

*Figure 6.5: Coupling efficiency from c-Si layer to a-Si layer with TE and TM mode source, respectively.*
Figure 6.6: Coupling efficiency from c-Si layer to a-Si layer with (a) TE mode source, with alignment error range in x direction $\Delta x = -1000 \text{ nm}, -500 \text{ nm}, 0 \text{ nm}, 500 \text{ nm}$ and $1000 \text{ nm}$; (b) TE mode source, with alignment error in y direction $\Delta y = 0 \text{ nm}, 200 \text{ nm}, 400 \text{ nm}, 600 \text{ nm}$ and $800 \text{ nm}$; (c) TE mode source, with $n_{a-Si} = 3.3, 3.4, 3.5, 3.6$ and $3.7$.

6.3 **Directional Coupler Based Vertical Coupler on Silicon Nitride**

Besides the SOI platform, silicon nitride is also an attractive material for micro- and nano-scale on-chip optical interconnect systems as we discussed in Chapter 5. However, the design on silicon nitride platform is more challenging compare to silicon platform, due to its lower material index property. Generally, lower material refractive index requires longer critical coupling length and longer taper length for low insertion loss. In addition, the gap between the two layers needs to be further extended for low crosstalk design purpose. The other challenge for silicon nitride platform is the thickness limitation. High quality silicon nitride layer for optical purpose normally has a thickness limitation of 400 nm. There is a risk to cause crack on the device layer if the thickness is over 400 nm. Several approaches have been proposed to overcome this issue [199-201], but they all bring additional fabrication complexity. In the following design, we use 350 nm thick silicon nitride with material index of 2.0 as the device layer and for simulation purpose. The inter-layer gap is set as 2.4 $\mu$m filled with silicon dioxide. The chosen
thickness and gap can avoid the cracking problem of high quality silicon nitride and provides lower interlayer crosstalk without using very wide waveguide width.

### 6.3.1 Device Structure

The key parameters are designed using the same designing method in Section 6.2. we found that when the waveguide width is 353 nm, the device can work polarization independently. At the meantime, when the waveguide width is over 1.2 μm, the device has very low inter-layer crosstalk. However, we as we discussed before, the low material index of silicon nitride will lead to higher insertion loss for short taper designs. The relationship between the taper length and the insertion loss is presented in Figure 6.7.

![Figure 6.7: Linear inverse taper insertion loss vs. different taper length from 20 μm to 100 μm, on 350 nm silicon nitride platform with the TE and TM modes, respectively.](image)

The insertion loss is higher than 0.1 dB (> 0.2 dB for a pair of tapers) for both modes even with 100 μm long taper and it increases sharply to around 0.3 dB when the taper is 20 μm long. Our target here is to design a taper with an insertion loss lower than 0.05 dB, so for a pair of tapers, the total loss is lower than 0.1 dB.

For lower insertion loss, the device length has to be sacrificed using the linear structure. Based on our further investigation, we found that the high insertion loss is mainly due
to the power leakage at the narrow waveguide width part. The insertion loss will be
doubled if the taper is used in both layers. In order to keep the impact of the taper at a
minimum level, we need to optimize the taper structure while keep the device length at
an acceptable level. Here, a nonlinear taper is designed to improve the insertion loss
based on the following logarithmic function:

\[
y = \frac{W_1}{2} - \frac{W_1}{2} - \frac{W_2}{2} \cdot \log(ax + 1)
\]

The parameters in Equation (6.3) can be explained by using the schematic of the
nonlinear shown in Figure 6.8.

![Figure 6.8: Schematic of the nonlinear (logarithmic function based) inverse taper, coordinate system uses \( \mu m \) as units.](image)

where \( W_1 \) and \( W_2 \) are the waveguide width at the taper start and the end, \( L \) is the total
taper length and \( a \) is a variable to control the taper width changing ratio. In the real
design, the edge of the taper is constructed with several straight lines instead of a
continues curve. Higher resolution comes with more points and lines. So here, the step
size is defined as the length in \( x \)-direction for each \( x \) coordinator output (point) based on
Equation (6.3). In each step, the shape of the edge is a straight line instead of a curve. In
another word, the change of waveguide width is linear in each step. In order to keep the
insertion loss lower than 0.05 dB for each taper, we choose 60 \( \mu m \) as the taper length. In
Figure 6.9, we show the 3D FDTD simulation results of the taper insertion loss with
different parameter \( a \) and number of steps. The taper changes the waveguide width from 1.2 \( \mu \text{m} \) to 353 nm \((W_1 = 1.2 \mu \text{m} \text{ and } W_2 = 0.353 \mu \text{m})\).

![Graph showing taper insertion loss vs parameter \( a \) and step number](image)

\( \text{Figure 6.9: The insertion loss of a 60} \mu \text{m} \text{ long nonlinear taper with (a) different parameter} \ a \ \text{in Equation 6.3; and (b) different number of steps} \ldots \)

As we can see in Figure 6.9(a), the insertion loss of the taper is minimized when \( a \) equals to 10. Then we use this value for the next step simulation. In Figure 6.9(b), step number of 4 clearly gives the best performance. So, the equation to generate the required points along the taper edge can be calculated by rewriting Equation (6.3) as:

\[
y = 0.6 - 0.1524 \cdot \log(10x + 1)
\]

(6.4)

Here, \( x \) is determined by the number of steps and the total taper length. The optimized inverse taper significantly improves the insertion loss compare to the insertion loss of the conventional linear taper with the same length (in Figure 6.7).

![Schematic of the layer-to-layer coupler on silicon nitride platform with optimized nonlinear tapers](image)

\( \text{Figure 6.10: Schematic of the layer-to-layer coupler on silicon nitride platform with optimized nonlinear tapers} \ldots \)
The complete design of the silicon nitride inter-layer coupler can be shown in Figure 6.10. The coupler is designed with two 350 nm silicon nitride layers. The material index used in the simulation is 2.0. The interlayer gap is 2.4 μm. The input and output transmission waveguides at different layers have a waveguide width of 1.2 μm to reduce interlayer crosstalk. The total length of the nonlinear inverse taper is 60 μm on both layers, which converts the waveguides from 1.2 μm to 353 nm. The coupling region consists of two parallel straight waveguides, with 353 waveguide width and 120 μm length. The total device length is 240 μm long.

6.3.2 Simulation Results and Fabrication Tolerance Discussion

The 3D FDTD simulation results are shown in Figure 6.11. The interlayer coupler has a minimum total insertion loss of -0.31 dB for the TE mode operation and -0.03 dB for the TM mode operation, includes the inverse taper insertion loss. Better performance is achievable for the TE mode operation with longer taper length (low to -0.21 dB). The device works polarization independently as we designed with central wavelength set at 1550 nm. The coupler can support broadband operation as well. For the 1500 nm to 1600 nm working bandwidth, the insertion loss variation is 0.22 dB for the TE mode operation and 0.18 dB for the TM mode operation.

![Figure 6.11: 3D FDTD simulated spectrums of the silicon nitride interlayer coupler, with the TE and the TM modes, respectively.](image-url)
With careful chemical-mechanical polishing process, the thickness of the silicon dioxide layer between the two layers can be very accurate (< 20 nm error). Therefore, the error from z-direction will not be discussed here. The major concern comes from the y-direction alignment. Here we show the 3D FDTD simulation results of the coupler performance in Figure 6.12. The insertion loss is simulated using a TE mode source at the single 1550 nm wavelength.

![Graph showing Y-directed error vs. coupler insertion loss with the TE mode at 1550 nm wavelength, using 3D FDTD simulation.]

As we can see, the total insertion loss of the coupler with y-directed alignment error up to 1 μm is still lower than 0.7 dB (> 85% coupling efficiency). The additional loss causes from misalignment is only 0.39 dB. Especially for misalignment error lower than 400 nm, the impact is negligible. The high fabrication tolerance is mainly due to the relatively low coupling coefficient and long coupling length. While 1 μm misalignment is sufficient for up-to-date lithography techniques. We further show the TE mode spectrum with 1 μm x-directed misalignment in Figure 6.13. The minimum insertion loss is 0.32 dB, which gives only 0.01 dB misalignment loss. The result matches our expectation since the device has a long coupling region and the x-directed misalignment mainly impact the real coupling length.
6.4 SUMMARY

In this chapter, we introduced a broadband and polarization independent interlayer coupler for high efficiency and low interlayer crosstalk purpose. The design is optimized for the silicon and the silicon nitride platform, respectively. For the silicon nitride platform, a nonlinear inverse taper was designed and optimized two reduce the taper length and insertion loss. For a single taper, the total insertion loss is lower than 0.05 dB with 60 μm taper length. Fabrication tolerance was also discussed by using 3D FDTD simulation. For the silicon platform design, the x-directed misalignment shows lower impact due to the strong coupling between the two layers. The material index difference is also a concern for the device performance. While for the silicon nitride platform, due to the relatively large gap between the two layers, the device is more sensitive the y-directed misalignment error instead of the x-directed misalignment error. Both designs show acceptable performance with misalignment up to 1 μm in either x or y direction.
7 Conclusions

7.1 Thesis Summary

This thesis has investigated several important aspects of silicon photonics technology. The fabrication processes for silicon photonic devices and facet smoothing technique for low loss fiber-to-chip measurement were introduced. Three passive high performance devices, the silicon circular HCG, the 2×2 silicon nitride polarization splitter and the interlayer coupler for both the silicon and the silicon nitride platforms, were proposed and discussed. Both devices come with very low insertion loss and able to support broadband operation, which are two important aspects for optical devices. Furthermore, potential applications and optimization solutions were discussed. The research work in thesis were based on novel ideas and independent research work in the group.

In Chapter 2, a literature survey of selected silicon photonic components was presented. Devices such as silicon waveguide, directional coupler, MZI, and microring resonator, were introduced and discussed. These components are highly related to the following research work. The silicon waveguide is the most basic component in the on-chip optical interconnect system. Single mode operation and low propagation loss is required to ensure the system performance. In addition, the understanding of the waveguide properties is useful for the research work. The directional coupler is used in both the polarization splitter and the interlayer coupler designs. Its simplicity and high efficiency are attractive in many areas. The MZI is the key component in the polarization splitter design. With its phase control abilities, different functions can be realized. The microring resonator is widely used for modulator and filter designs. In our research work, it was used to construct the external cavity of the hybrid silicon in Chapter 4, which is a potential application for the circular HCG.

In Chapter 3, the fabrication processes were introduced. We also highlighted some details which need to be done carefully during the processes to avoid failure. The EBL
Conclusions

process and the RIE process were discussed in detail. The quality of the EBL process
plays an important role in the fabrication. We introduced the impact with different EBL
resists and the process for dos test. PEC was used in the EBL optimization to reduce
the impact from the scattering problem. The chip facet is fabricated by using RIE for
oxide layer etching and Bosch process for deep silicon substrate etching to ensure
smoothness. Using this polish-free process can significantly reduce the insertion of the
spot size converter. In addition, we also introduce the RIE process for silicon nitride
etching. The waveguide propagation loss is lower than 1 dB/cm for the silicon nitride
waveguide due to lower scattering loss from the waveguide sidewall roughness.

In Chapter 4, a silicon integrated compact circular HCG reflector with a footprint of 4.03 \times
4.32 \mu m^2 was proposed and experimentally demonstrated. Measurement results showed that the
circular HCG with optimized parameters has an average reflectance of 94.15\% from 1525 nm
to 1610 nm wavelength and the PER is higher than 13 dB over the entire measured wavelength
range. The impacts of different parameter settings were demonstrated as well. The results
agreed well with the simulations. The broadband performance was investigated through 3D-
FDTD simulation. The results showed that for $R > 90\%$, a continues band of up to 385 nm can
be achieved which gives $\Delta \lambda / \lambda = 24.83\%$. The proposed device provides low mirror loss, large
tuning range and reduced polarization degeneracy for most of its applications, especially silicon
based hybrid tunable laser cavities. We also proposed a conceptual hybrid silicon laser
design using the modified circular HCG with an output waveguide to construct the
external cavity. The reflection wavelength of the external cavity can be dynamically
changed potentially in less than 100ps. The energy consumption is calculated and shows
promising performance compare to the previous designs.

In Chapter 5, a 2×2 PBS based on SiN was proposed and experimentally demonstrated.
Two polarization independent asymmetric 3-dB directional couplers with ultra-short
parallel-coupling length of 1.2 \mu m and a phase control section with only 27.7 \mu m length
were used in the proposed PBS. The proposed device was fabricated and measurement
results showed that the PBS has a minimum insertion loss of 0.13 dB and 0.34 dB for
TE and TM polarized lights, respectively. It was also shown that the ER is higher than
20 dB for the TE polarization throughout the measured band from 1530 nm to 1610 nm,
and over the entire C band for the TM polarization. The measurement results showed a
good agreement with the simulation results. In addition, a possible solution was
proposed and discussed to improve the wavelength dependent problem of the TM mode operation. By replacing the input asymmetric coupler with a 3-dB splitter, the difference between the minimum and maximum extinction ratio is reduced to 9 dB compared to 18 dB of the previous design for the TM mode operation. The maximum insertion in the working bandwidth is only -0.21 dB based on the simulation results. However, the cost is additional 0.1 dB insertion loss for the TE mode operation.

Two interlayer couplers for the silicon platform and the silicon nitride platform were introduced in Chapter 6. Both designs support low insertion loss, broadband and polarization independent operation, and low interlayer crosstalk. For the silicon nitride platform, a nonlinear inverse taper was designed and optimized to reduce the taper length and insertion loss. For a single taper, the total insertion loss is lower than 0.05 dB with 60 μm taper length. Fabrication tolerance was also discussed by using 3D FDTD simulation. For the silicon platform design, the x-directed misalignment shows lower impact due to the strong coupling between the two layers. The material index difference is also a concern for the device performance. While for the silicon nitride platform, due to the relatively large gap between the two layers, the device is more sensitive to the y-directed misalignment error instead of the x-directed misalignment error. Both designs show acceptable performance with misalignment up to 1 μm in either x or y direction.

## 7.2 DIRECTIONS FOR FUTURE WORK

### 7.2.1 Hybrid Silicon Laser

In [202], a hybrid silicon laser using the proposed circular HCG was proposed and discussed. We show the impact of energy consumption using such a laser design. However, the laser itself has not been experimentally demonstrated yet. In the future work, the laser will be fabricated and demonstrated.

Flip-chip technique can be used to mount the SOA chip on the wafer substrate [203, 204]. Precise wavelength alignment is required to realize the hybrid laser. An additional metal heater layer can be added as the thermal controller to stabilize the temperature and
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pre-set the wavelength to required position [205, 206]. The modified circular HCG needs to be designed and optimized in the future to keep the insertion loss at a low level.

Besides the flip-chip technique, other fabrication processes such as ion implantation for the mirroring modulators, metal deposition for heaters need to be developed. The measurement setup for high speed active devices need to be investigated as well.

7.2.2 Demonstration of the Interlayer Coupler

The interlayer coupler introduced in Chapter 6 shows only the 3D FDTD simulation results. The good device performance needs to be further demonstrated by real measurement results. The key challenges for the fabrication include interlayer lithography alignment and chemical-mechanical polishing process. These fabrication steps need to be developed during the future work. In addition, the deposition quality of a-Si and silicon nitride should be further confirmed. The experiment demonstration can be realized by using the existing measurement platform introduced in Chapter 2 since only passive devices are included.

7.2.3 Optical On-Chip Phase Array

The previous mentioned interlayer coupler is an important component for the next stage work, which is the demonstration of an optical on-chip phase array system [207-209]. With the combination of the broadband and low loss 3 dB splitter [210], it is possible to realize a high efficiency phase array system with simple design and wide tuning range. Compare to the grating based phase array, our multi-layer designs can support much higher power efficiency and also reduced spacing between each antenna, due to the low crosstalk advantage of our design.

The interlayer coupler on the silicon nitride platform can also be used to design a phase array with visible light, since silicon nitride is transparent in the visible light band. The recent demonstrated silicon nitride phase array with visible light was realized by gratings [211], which have a high insertion loss compare to the waveguide based design. Similar to the silicon platform design, our interlayer coupler supports low crosstalk and can efficiently reduce the antenna spacing for the phase array, and hence, provides wider tuning angle range.
References


resonators.” Optics Express 20(7): 7672-7684.


References


wideband interlayer grating couplers in multilayer Si/SiO2/SiN platform for 3D integration of optical functionalities,” Optics Express 22(14), 16767–16777.


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