Study of Silicon Photonic Waveguides Towards on chip Electro-optic Integration

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In the Name of Allah, the Most Gracious, the Most Merciful
Abstract

Nanophotonic technologies have attracted a lot of attention to co-develop optical and electronic devices on Silicon (Si) that further modern optical communications in miniaturization. Photonic devices with significantly high bandwidth as well as reduced power dissipation have offered attractive solutions for circumventing the problems of interconnect bottlenecks in the dense integration of electronic devices, signal delay and electronic power dissipation. To benefit from photonic devices and combine them with mature and low-cost complementary metal-oxide semiconductor (CMOS) manufacturing technology, the area of Si photonics has gained a widespread interest in both academic and industrial research efforts. Si, with its inherent excellent linear and nonlinear optical characteristics in infrared, adequate thermal conductivity and a high optical damage threshold, has shown the ability to be engineered for concepts and design of a new class of modern photonic devices. The high-index-contrast waveguide, together with the unique bandgap structure, has allowed Si to be considered for various state-of-the-art passive and active photonics devices.

The research goal of this thesis is to investigate design options and pathways for improvements towards realization of monolithic integration of CMOS-compatible optoelectronic devices suitable for high speed applications. Investigation, characterization and new design for improvement of different miniaturized Si waveguides to fit for specific applications achieving low loss and high performance are the main focus points. One such application is the photonic time stretched analog-to-digital converter (TS-ADC), in which the typically used long fibers are proposed to be replaced by dispersive Si waveguides. Design trade-offs involved in the design of suitable waveguides to meet this required dispersion profiles are thoroughly investigated. Results of a systematic evaluation of the most popular forms of passive Si wire, rib and photonic crystal waveguides with and without bends are presented and analysed. However, none of these passive waveguides are dispersive enough to be used in the proposed TS-ADC design. While cascaded waveguides could potentially be used to achieve the dispersion levels required, this option will require significantly larger photonic integrated circuits making it practically infeasible from the cost as well as the loss perspectives. This leads to investigate active Si waveguides, where with geometry, the control of biasing and doping concentrations provide greater control to tailor dispersion. As a result, dispersion is considerably enhanced in active waveguides compared to passive waveguides.

Photodiode (PD), which is an essential component of PICs, has also been investigated in this thesis. It considers a vertical n-i-p photo diode (PD) to characterize dark current, photocurrent and responsivity by incorporating changes in physical dimensions and bias voltages. Distributed Bragg reflectors (DBR) are introduced at the end of the Ge layer to reflect back the residual un-
absorbed light, which effectively increases absorption length without adding any device capacitance. An increase in transit time limited bandwidth is achieved with a graded doping profile instead of constant doping which enhances the electron transport towards intrinsic collection layer and decreases the transit time. With the proposed design options, it is shown that the resulting PDs with high responsivity, high bandwidth and low dark current properties making them highly suitable for on-chip integration of proposed TS-ADC.

One of the key challenges with submicronic waveguide devices is enabling efficient coupling with fiber, which is mainly due to the mode-field differences between the fiber and the waveguide, and the relative misalignments. Conventional butt coupling schemes suffer from strong back reflection due to the large mismatch between the fiber core and Si waveguide refractive index and also require additional processing steps that complicates the fabrication. A performance-enhanced butt coupling mechanism incorporating a vertically and laterally tapered SiON polymer core to tunnel and widen confined optical modes from adiabatic tapers is proposed. The performance of the design is characterized for distinct features including tapering length, coupling efficiency, coupling bandwidth, and is also compared with the performance of grating couplers. Although grating couplers are “friendlier” for wafer scale testing, the proposed coupling scheme offers low-loss high-coupling efficiency with greater bandwidth.

To integrate many discrete functional blocks into a larger PIC suitable for applications such as TS-ADC, controlling polarisation within the PIC becomes a challenge. Due to anisotropy in cross-sectional geometry or stress distribution, guided TE and TM modes behave differently in waveguides and therefore require polarization management. In this thesis, the design and operation of a CMOS compatible polarization rotator based on asymmetrical Si waveguide is presented. New structural designs are proposed by introducing 1D PhC structure. A novel approach of lateral tapering is introduced in the rotator device which further reduces the device length. Addition to these, a CMOS compatible SiN/SiO₂ structure is proposed. Numerical evaluation of the proposed design shows rotator length less than 4 μm with high operational bandwidth of >700nm which covers the entire short and long haul telecommunication bands.
Preface

The main motivations of this research were primarily related to the proposal, theoretical analysis and numerical evaluations of various Si based waveguides to realize single chip solution of the TS-ADC target application. None of the text of the dissertation is taken directly from previously published or collaborative articles.

There are total 8 chapters in this dissertation out of which Chapter 3, 4, 5, 6 and 7 are the main contributory chapters. The main ideas and investigations of these chapters are done by me and my supervisors Dr. Masuduzzaman Bakaül, Prof. Thas Nirmalathas and Prof. Stan Skafidas have helped me to shape them. All major concept formations, simulations, analysis, compositions and writings are performed by me. Time to time discussion with supervisors has helped me to successfully implement the ideas and to tune them in right direction. My colleague, Md Asaduzzaman has helped time to time to perform simulations as well as with fruitful discussions. Also very effective suggestions in the earlier stages of developing the models of the waveguides were provided by Prof. W.-Y. Choi from Yonsei University, Seoul, Korea and Dr. Faruq Hossain.

Most of the works presented in this dissertation have already been published in three journals and six conferences, where I am the principle author. The papers are co-authored by Dr. Masuduzzaman Bakaül, Md. Asaduzzaman, Prof. Stan Skafidas, and Prof. Thas Nirmalathas all of whom have contributed in discussion of the results and improving the writing and presentation of the papers. All the conferences are funded by National ICT Australia (NICTA) and one journal based on Chapter 4 of the thesis is funded by Commonwealth Scientific and Industrial Research Organisation (CSIRO).

The writing of the thesis is proofread by Greg Rowe from New Zealand. He is a professional proof-reader and has completed a correspondence course in editing and proofreading provided by an Australian university. Mr. Greg has assisted to check the spelling and grammatical errors and has improved the quality of overall writing.
Declaration

This is to certify that

1. This thesis comprises only my original work towards my PhD candidature.
2. Due acknowledgement has been made in the text to all other materials used.
3. The thesis is less than 100,000 words in length, exclusive of tables, maps, bibliographies, and appendices.

Md Rezwanul Haque Khandokar
Acknowledgements

I thank Allah (Almighty God) for providing me with the opportunity and the ability to pursue this research and for blessing me with the means, the environment and the people who have helped me to get through it in the best of ways. After thanking Allah, it is a great opportunity to express my utmost gratitude to my supervisors, Dr. Masuduzzaman Baul, Prof. Thas Nirmalathas, and Prof. Stan Skafidas for their support and encouragement to my work both intellectually and mentally. I am really grateful to them for their continuous guidance, constructive suggestions, and much helpful advice throughout the journey. I would like to thank Prof. W.-Y. Choi from Yonsei University, Seoul, Korea and Dr. Faruq Hossain for their advice in earlier stages of developing the models of the waveguides. Very special thanks to my group mate Md Asaduzzaman for all effective discussions about many obstacles. I am also grateful to all the staff of the Department of Electrical and Electronic Engineering and the School of Graduate Research for providing the necessary administrative support and obviously to The University of Melbourne. Thanks also go to National ICT Australia (NICTA) for its scholarship, publications and travel funding throughout the candidature.

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Finally but certainly not least, my heartiest gratitude and thanks to my beloved parents, Md Reazul Haque Khandokar and Raihana Jafri, whom Allah has blessed me with. Their utmost care, support and indispensable guidance have brought me here. Anything that I have done or will do is nothing but a fruit of their kind efforts and sacrifice. I would like to deeply thank my beloved wife, Naznin Sultana, my loving daughter, Mahdiya, and my loving son, Musab, for their sacrifices and continuous encouragement to complete this thesis. Throughout the journey they were my tranquillity and inspiration.
Contents

Chapter 1
1.1 Silicon Photonics ................................................................. 1
1.2 Silicon-on-Insulator (SOI)...................................................... 2
1.3 Towards on chip electro-optic integration ................................. 3
1.4 Si photonic components and applications .................................. 3
1.5 Research motivations .......................................................... 5
1.6 Thesis Outline ........................................................................ 8
1.7 Main findings and contributions ............................................... 11
1.8 Publications ........................................................................... 14
  1.8.1 Publications directly related to this thesis ............................. 14
    1.8.1.1 Journal Papers ............................................................ 14
    1.8.1.2 Submitted and prepared to submit papers: ....................... 14
    1.8.1.3 Conference papers ...................................................... 15
  1.8.2 Other Publications ............................................................ 16
    1.8.2.1 Journal papers ................................................................ 16
    1.8.2.2 Submitted and prepared to submit: ................................ 16
    1.8.2.3 Conference papers ...................................................... 16

Chapter 2
2.1 Introduction ............................................................................. 18
2.2 History .................................................................................... 19
2.3 Photonic analog-to-digital converter (ADC) ............................... 20
2.4 Passive devices ........................................................................ 23
  2.4.1 Si waveguide ....................................................................... 23
    2.4.1.1 Si waveguide properties and applications ......................... 24
  2.4.2 Coupler ............................................................................... 25
  2.4.3 Polarization splitter/rotator ................................................... 27
2.5 Active devices .......................................................................... 30
  2.5.1 Lasers ................................................................................ 30
    2.5.1.1 Emission in bulk Si ......................................................... 30
    2.5.1.2 Quantum confinement ................................................... 31
    2.5.1.3 Doping with rare earth ions ........................................... 32
    2.5.1.4 Si Raman laser ............................................................ 32
    2.5.1.5 Epitaxial growth III-V materials on Si ............................... 33
    2.5.1.6 Epitaxial growth of Ge on Si laser ................................. 33
    2.5.1.7 Hybrid lasers on Si ....................................................... 34
List of Figures

Fig. 1.1: Few basic components in Si photonics interconnect platform................................. 1
Fig. 1.2: Schematic of a SOI wafer: simple planar structure................................................ 2
Fig. 1.3: Cross-sectional view of few basic Si photonic components in PICs .......................... 4
Fig. 1.4: Schematic of Time Stretched ADC technique.......................................................... 5
Fig. 1.5: Typical structure of coupling techniques.................................................................... 7
Fig. 2.1: Some application fields of Si photonic platform....................................................... 20
Fig. 2.2: Conventional Time Interleaved ADC architecture.................................................... 21
Fig. 2.3: Photonic sampled, demultiplexed and electrically Quantized ADC.......................... 22
Fig. 2.4: (a) Schematic of SOI waveguide. (b) AWG polarization splitter ............................... 28
Fig. 2.5: Energy band diagram showing carrier transition process......................................... 31
Fig. 2.6: Schematic of hybrid Si laser ..................................................................................... 34
Fig. 2.7: Schematic of a SOH modulator ................................................................................. 35
Fig. 2.8: Absorption coefficients for various semiconductors ................................................. 37
Fig. 2.9: Schematic of a typical UTC PD.................................................................................. 41
Fig. 2.10: Schematic of fabrication processes........................................................................... 42
Fig. 3.1: Time stretching of high speed signal......................................................................... 46
Fig. 3.2: Proposed CMOS-compatible on chip TS ADC design.............................................. 47
Fig. 3.3: Visualization of the cylindrical coordinate system from different angles.................. 49
Fig. 3.4: Bend of the confined mode with cross section of the waveguide in xy plane............. 50
Fig. 3.5: E-field intensity of the confined mode in log scale for Si wire.................................... 51
Fig. 3.6: (a): Dimensions of the Si wire, and (b): E-field intensity of the confined mode........... 52
Fig. 3.7: Changes of optical parameters of a Si wire waveguide with different core heights... 52
Fig. 3.8: Sharp change in loss near cut-off wavelength for different core heights..................... 53
Fig. 3.9: Changes of optical parameters of a Si wire waveguide with different core widths.... 54
Fig. 3.10: Changes of optical parameters of a Si wire with different cladding height............... 54
Fig. 3.11: E-field intensity of the confined mode in log scale with different cladding heights. . 55
Fig. 3.12: Influence of bending on Si wire.............................................................................. 56
Fig. 3.13: E-field intensity of the confined mode with micro bends......................................... 56
Fig. 3.14: (a) Dimensions of rib Si waveguide, (b): E-field intensity of the confined mode..... 57
Fig. 3.15: Changes of optical parameters of a rib waveguide with core heights.................... 58
Fig. 3.16: Changes of optical parameters of a rib waveguide with core widths...................... 59
Fig. 3.17: Changes of optical parameters of a rib waveguide with cladding height................. 59
Fig. 3.18: E-field intensity of the confined mode in log scale with cladding heights................ 60
Fig. 3.19: Characteristics of rib waveguide.............................................................................. 61
Fig. 3.20: E-field intensity of the confined mode with micro bends......................................... 61
Fig. 3.21: (a) Dimensions of 1D PhC waveguide, (b) E-field intensity ...................... 62
Fig. 3.22: Changes of optical parameters of a PhC waveguide with core heights .......... 62
Fig. 3.23: Changes of optical parameters of a PhC waveguide with core widths .......... 63
Fig. 3.24: Changes of optical parameters of a PhC waveguide with cladding height ....... 64
Fig. 3.25: E-field intensity of the confined mode in log scale with cladding heights ....... 64
Fig. 3.26: Characteristics of the PhC waveguide .............................................. 65
Fig. 3.27: E-field intensity of the confined mode with micro bends ....................... 65
Fig. 4.1: (a): Primary geometry of active Si waveguide (b): Specified doping regions .... 73
Fig. 4.2: Functionality of the waveguide ...................................................... 75
Fig. 4.3: Carrier distribution (n-type) as a function of applied bias ....................... 75
Fig. 4.4: Changes of waveguide parameters with uniform doping concentration ......... 76
Fig. 4.5: Changes of waveguide parameters with non-uniform doping concentration ..... 77
Fig. 4.6: Changes of waveguide parameters with respect to Hp ................................ 78
Fig. 4.7: Mode Field Distribution for different Hp ............................................. 78
Fig. 4.8: Changes of waveguide parameters with respect to the changes in Wd ............ 79
Fig. 4.9: E-field intensity (in log scale) of the confined mode for different Wd .......... 79
Fig. 4.10: Changes of waveguide parameters with respect to Ww ................................ 80
Fig. 4.11: Mode field distribution (Ex) of TM polarized light ................................ 81
Fig. 4.12: Changes of waveguide parameters for TM polarization ....................... 82
Fig. 4.13: Field profile of the confined mode ................................................. 82
Fig. 4.14: Changes of waveguide parameters with the changes in doping concentrations ...... 83
Fig. 4.15: Contribution of radiative bending loss to total loss for various bending radius ...... 83
Fig. 4.16: Changes of dispersion in active waveguide ........................................ 84
Fig. 4.17: Initial dimension of active PIN Si PhC waveguide under investigation ....... 86
Fig. 4.18: (a) Mode field distribution (Ex); (b) Electrostatic at -4v bias voltage ............. 86
Fig. 4.19: Electron distribution as a function of applied bias ................................. 87
Fig. 4.20: Changes of optical parameters with uniform changes in doping concentration ...... 87
Fig. 4.21: Changes of optical parameters with on-uniform changes in doping concentration ..... 88
Fig. 4.22: Changes of optical parameters with respect to changes in Ww ................. 89
Fig. 4.23: Changes of waveguide parameters with respect to the changes in Hp ............ 90
Fig. 4.24: Mode field distribution for different Hp: (a): Hp = 50 nm, (b): Hp = 120 nm ...... 90
Fig. 4.25: Mode Field Distribution (Ex) of TM polarized light ................................. 91
Fig. 4.26: Changes of waveguide parameters for TM polarization .......................... 92
Fig. 4.27: Field profile of the confined mode .................................................. 92
Fig. 4.28: Changes of waveguide parameters with changes in doping concentrations ....... 93
Fig. 4.29: Contribution of radiative bending loss to total loss for various bending radius ...... 93
Fig. 4.30: Changes of dispersion in active 1D PhC waveguide ............................. 94
Fig. 5.1: Absorption of photons in intrinsic layer and corresponding band diagram
Fig. 5.2: Coupling schemes of PDs.
Fig. 5.3: Primary geometry of the Ge on Si n-i-p vertical photo diode.
Fig. 5.4: Electric Field profile: (a) z-x plane; (b) z-y plane.
Fig. 5.5: Changes in spot size conversion efficiency over tapering length.
Fig. 5.6: Changes of characteristics parameters with respect to changes in Ge height.
Fig. 5.7: Changes of characteristics parameters with respect to changes in Si height.
Fig. 5.8: Primary geometry of the Ge on Si n-i-p vertical PD.
Fig. 5.9: Changes of responsivity with respect to changes in bias voltage and DBR length.
Fig. 5.10: Wavelength dependence of the DBR.
Fig. 5.11: Changes in frequency response for various bias voltages.
Fig. 5.12: For varying Ge height (a): impulse and step response; (b): frequency response.
Fig. 5.13: For varying Si height (a): impulse and step response; (b): frequency response.
Fig. 5.14: Schematic of the simulated UTC PD.
Fig. 5.15: Changes of characteristics parameters with respect to changes in InP thickness.
Fig. 5.16: Changes of characteristics parameters with respect to changes in PD length.
Fig. 5.17: Changes of BW over PD area.
Fig. 5.18: Current travelling in the InP collection layer at different thickness point.
Fig. 5.19: Changes of RC limited, transit time limited and overall BW with InP thickness.
Fig. 5.20: Comparison of BW over InP thickness.
Fig. 6.1: Lateral SSC under investigation.
Fig. 6.2: Conversion efficiency Vs Tapering length.
Fig. 6.3: Initial dimension of SSC with a polymer (SiON) second core under investigation.
Fig. 6.4: Field profile: (a) lateral conversion; (b) vertical conversion.
Fig. 6.5: Comparison of transmission over tapering length.
Fig. 6.6: Changes of transmission over tapering length with down and up SSC.
Fig. 6.7: Initial dimension of SSC with a laterally and vertically tapered core.
Fig. 6.8: Changes of conversion efficiency over tapering length.
Fig. 6.9: Changes of efficiency over tapering length for different core dimensions.
Fig. 6.10: Electric field profile and frequency response.
Fig. 6.11: Schematic diagram of tapered SSC based butt coupler.
Fig. 6.12: Overall coupling efficiency with and without proposed improvements.
Fig. 6.13: Initial dimension grating coupler to couple light.
Fig. 6.14: Full field profile of the grating structure without Bragg reflectors.
Fig. 6.15: Coupling efficiency as a function of injection angle.
Fig. 6.16: Coupling efficiency for various distinguishable parameters.
Fig. 6.17: Comparison of coupling efficiency over wavelength.
Fig. 6.18: Performance comparison of grating and tapered SSC based butt coupling.............. 130
Fig. 6.19: Fabrication technique of ultra-narrow inverse taper structure.......................... 131
Fig. 6.20: Fabrication process of a vertical taper.......................................................... 132
Fig. 6.21: SEM images................................................................................................. 132
Fig. 7.1: (a) Waveguide A structure; (b) Waveguide B structure. ..................................... 136
Fig. 7.2: Combined structure of waveguides A and B to perform the PR.......................... 137
Fig. 7.3: E-field intensity.............................................................................................. 137
Fig. 7.4: PR efficiency Vs rotator length: Conversion from TE mode to TM mode............ 138
Fig. 7.5: Beats due to interference with higher order modes ......................................... 139
Fig. 7.6: Compact structures (a) Waveguide A; (b) Waveguide B. .................................. 140
Fig. 7.7: Combined structure of waveguide A and B to perform the PR......................... 140
Fig. 7.8: E-field intensity.............................................................................................. 141
Fig. 7.9: Conversion from TE mode to TM of waveguide A........................................... 141
Fig. 7.10: Impact of varying $W_b$ values....................................................................... 142
Fig. 7.11: Wavelength response of the designed rotator................................................ 143
Fig. 7.12: Conversion from TE mode to TM ................................................................. 143
Fig. 7.13: Compact structures (a) Waveguide A; (b) Tapered Waveguide B............... 144
Fig. 7.14: Combined structure of waveguide A and laterally tapered waveguide B........ 144
Fig. 7.15: Conversion from TE mode to TM of waveguide A with lateral tapering........ 145
Fig. 7.16: Impact of varying $W_b$ values....................................................................... 146
Fig. 7.17: Wavelength response of the designed rotator................................................ 146
Fig. 7.18: Beats due to interference with higher order modes........................................ 147
Fig. 7.19: Conversion from TE mode to TM mode with SiN core material..................... 148
Fig. 7.20: Conversion from TE mode to TM mode with $W_s=500$nm............................. 148

List of Tables
Table 2-1: Performance comparison of SSC with existing demonstrations....................... 26
Table 2-2: Overview of different approaches of PRs reported in literature....................... 29
Table 2-3: Overview of different approaches of Ge-based Si PDs reported in literature........ 40
Table 5-1: Dark current dependence on various processes............................................... 101
**List of abbreviations:**

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al</td>
<td>Aluminium</td>
</tr>
<tr>
<td>ASE</td>
<td>Advance Si Etch</td>
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<tr>
<td>BW</td>
<td>Bandwidth</td>
</tr>
<tr>
<td>BESOI</td>
<td>Bond and Etch Back SOI</td>
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<tr>
<td>BOX</td>
<td>Buried Oxide</td>
</tr>
<tr>
<td>CVCS</td>
<td>Continuously Varying Cross-sectional Subcell</td>
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<tr>
<td>CVD</td>
<td>Chemical Vapor Deposition</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal-Oxide Semiconductor</td>
</tr>
<tr>
<td>DBR</td>
<td>Distributed Bragg Reflectors</td>
</tr>
<tr>
<td>DARPA</td>
<td>Defense Advanced Research Projects Agency</td>
</tr>
<tr>
<td>Er</td>
<td>Erbium</td>
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<tr>
<td>EME</td>
<td>Eigen Mode Expansion</td>
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<tr>
<td>EPIC</td>
<td>Electronic and Photonic Integrated Circuits</td>
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<tr>
<td>FCG</td>
<td>Free Carrier Generation</td>
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<tr>
<td>FWM</td>
<td>Four Wave Mixing</td>
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<tr>
<td>FCA</td>
<td>Free Carrier Absorption</td>
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<tr>
<td>FCC</td>
<td>Free Charge Carriers</td>
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<tr>
<td>GVD</td>
<td>Group Velocity Dispersion</td>
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<tr>
<td>Ge</td>
<td>Germanium</td>
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<tr>
<td>ICP</td>
<td>Inductive Coupled Plasma</td>
</tr>
<tr>
<td>IC</td>
<td>Inductively Coupled Plasma</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
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<tr>
<td>LSI</td>
<td>Large Scale Integration</td>
</tr>
<tr>
<td>LEPECVD</td>
<td>Low Energy Plasma Enhanced Chemical Vapor Deposition</td>
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<tr>
<td>LOCOS</td>
<td>Local Oxidation</td>
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<tr>
<td>ML</td>
<td>Mode Loss</td>
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<tr>
<td>MSI</td>
<td>Medium Scale Integration</td>
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<tr>
<td>MBE</td>
<td>Molecular Beam Epitaxy</td>
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<tr>
<td>MMI</td>
<td>Multimode Interferometer</td>
</tr>
<tr>
<td>MZI</td>
<td>Mach-Zehnder Interferometer</td>
</tr>
<tr>
<td>MOS</td>
<td>Metal-Oxide-Semiconductor</td>
</tr>
<tr>
<td>MRR</td>
<td>Microring Resonator</td>
</tr>
<tr>
<td>NIL</td>
<td>Nano Imprint Lithography</td>
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<tr>
<td>NA</td>
<td>Numerical aperture</td>
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<tr>
<td>OPC</td>
<td>Optical Phase Conjugation</td>
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<tr>
<td>Abbreviation</td>
<td>Full Form</td>
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<tr>
<td>PCSPW</td>
<td>Photonic Crystal Surface Plasmon Waveguide</td>
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<tr>
<td>PD</td>
<td>Photo Diode</td>
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<tr>
<td>PICs</td>
<td>Photonic Integrated Circuits</td>
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<tr>
<td>PML</td>
<td>Perfectly Matched Layer</td>
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<tr>
<td>PhC</td>
<td>Photonic Crystals</td>
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<tr>
<td>RF</td>
<td>Radio Frequency</td>
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<tr>
<td>RIE</td>
<td>Reactive Ion Etching</td>
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<tr>
<td>RI</td>
<td>Refractive Index</td>
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<tr>
<td>SMF</td>
<td>Single Mode Fiber</td>
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<tr>
<td>SIMOX</td>
<td>Separation by Implantation of Oxygen</td>
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<tr>
<td>SPEL</td>
<td>Self-Perfection by Liquefaction</td>
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<tr>
<td>SPM</td>
<td>Self-Phase Modulation</td>
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<tr>
<td>SiON</td>
<td>Si-Oxy-Nitride</td>
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<tr>
<td>SSI</td>
<td>Small Scale Integration</td>
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<tr>
<td>SSC</td>
<td>Spot Size Converter</td>
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<tr>
<td>Si</td>
<td>Silicon</td>
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<tr>
<td>SiN</td>
<td>Silicon Nitride</td>
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<tr>
<td>SiO2</td>
<td>Silica</td>
</tr>
<tr>
<td>SOI</td>
<td>Silicon on Insulator</td>
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<tr>
<td>SHINE</td>
<td>Silicon Heterostructure Intersubband Emitter</td>
</tr>
<tr>
<td>SRS</td>
<td>Stimulated Raman Scattering</td>
</tr>
<tr>
<td>SOH</td>
<td>Si Organic Hybrid</td>
</tr>
<tr>
<td>SRO</td>
<td>Si Rich Oxide</td>
</tr>
<tr>
<td>SPEL</td>
<td>Self-Perfection by Liquefaction</td>
</tr>
<tr>
<td>TS-ADC</td>
<td>Time Stretched Analog-to-Digital Converter</td>
</tr>
<tr>
<td>TPA</td>
<td>Two Photon Absorption</td>
</tr>
<tr>
<td>TIR</td>
<td>Total Internal Reflection</td>
</tr>
<tr>
<td>TE</td>
<td>Transverse Electric</td>
</tr>
<tr>
<td>TM</td>
<td>Transverse Magnetic</td>
</tr>
<tr>
<td>ULSI</td>
<td>Ultra Large Scale Integration</td>
</tr>
<tr>
<td>UHVCVD</td>
<td>Ultra High Vacuum Chemical Vapor Deposition</td>
</tr>
<tr>
<td>UTC</td>
<td>Uni-Travelling Carrier</td>
</tr>
<tr>
<td>VPD</td>
<td>Vertical Photo Diode</td>
</tr>
<tr>
<td>VLSI</td>
<td>Very Large Scale Integration</td>
</tr>
<tr>
<td>WDM</td>
<td>Wavelength Division Multiplexing</td>
</tr>
<tr>
<td>XPM</td>
<td>Cross phase modulation</td>
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Chapter 1

Introduction

1.1 Silicon Photonics

Over the last few decades, integrated circuits on Si platform have modernized the electronics industry: the number of transistors per chip has doubled on average every two years as was elegantly described in Moore’s law. As this trend continues further, the increasingly dense integration of electronic devices has approached an interconnect bottleneck and is limited by increased signal delay and electronic power dissipation. On the other hand, photonic devices with significantly high bandwidth as well as reduced power dissipation have offered attractive solutions for circumventing some of these problems. In such circumstances, to benefit from photonic devices and combine them with mature as well as low-cost complementary metal-oxide semiconductor (CMOS) technology, the area of Si photonics has gained a widespread interest in both academic and industrial research efforts [1].

In recent years, Si-based nanophotonic technology has made unprecedented progress to develop highly integrated electronic–photonic platforms [1]. Goal towards realising low cost photonics have been the motivational force for Si photonics research drawing on the integrated circuit (IC) industry and accessibility of suitable silicon-on-insulator (SOI) wafers. Si, with its inherent excellent linear and nonlinear optical characteristics in infrared, a high optical damage threshold and adequate thermal conductivity, has shown the ability to be engineered into devices capable of realising a range of functional concepts and manufacturable designs of modern photonic devices [2]. The high-index-contrast waveguide, together with its unique bandgap structure, has enabled Si to be considered for various state-of-the-art passive and active Si photonics devices shown in Fig. 1.1.

![Fig. 1.1: Few basic components in Si photonics interconnect platform.](image-url)
1.2 Silicon-on-Insulator (SOI)

The SOI platform, where Si is utilized as the substrate and also as waveguiding material, is acknowledged for its compatibility with CMOS technologies for making dense, highly integrated, compact and multifunctional photonic devices. It has distinct advantages compared to Group III-V compounds and polymers and offers suitable monolithic integration of photonic and electronic devices on the same substrate [3]. A wide range of optical devices capable of emitting, guiding, modulating and detecting light, optical switches, spectrometers, attenuators, add/drop filters and wavelength converter have all been realized on the SOI platform [2].

As shown in Fig. 1.2, the basic SOI configuration consists of a Si core, a buried SiO$_2$ cladding layer and a Si substrate. At the operating wavelength of 1550 nm, the cladding layer has a refractive index (RI) of 1.44, which is much lower than that of Si core layer of 3.5. This provides essential optical isolation and prevents the light from passing to the Si substrate. The thickness of the bottom SiO$_2$ cladding has an insignificant effect on the waveguide, as long it is sufficient to prevent optical field penetration. An upper cladding layer of SiO$_2$, nitride or polymers over the Si core, acts as an electrical isolator and also reduces surface contamination.

Although SOI has numerous advantages in integrated optics and photonic devices, this also creates many research challenges. Some properties of Si suggest it to be a poor optical material. Stimulated emission is extremely inefficient in Si due to the indirect bandgap structure which makes laser actions impractical. Si has significant two-photon-absorption (TPA) near telecom wavelengths, which reduces the efficiency of Kerr nonlinear processes [4]. Due to poor responsivity of Si around short and long haul telecommunication bands, Germanium (Ge) is utilized as the active material in photo detection which has a 4.2% lattice mismatch with Si and places barriers to monolithic integration [5].
1.3 Towards on chip electro-optic integration

The presence of a high index contrast between Si and silica (SiO2) layers in the waveguide enables photonic devices with dimensions as low as a few hundred nanometers (nm) and leverages the potential to integrate multiples of such devices into a CMOS-compatible microsystems chip. The major challenges in developing a heterogeneous chip are strongly connected with temperatures in CMOS processing and in operation [6]. They include incompatibility of the CMOS process for Germanium (Ge)-based devices in high temperature post-growth annealing, Si’s indirect bandgap profile, dissipation of higher heat, and on-chip temperature fluctuations in operations. Further, a large lattice mismatch and thermal expansion make monolithic integration a very difficult task. As a compromise, a hybrid approach of integration can alleviate these difficulties to some extent by utilizing both Si and Group III-V semiconductor materials. This takes advantage of mature process technologies both in Group III-V semiconductor materials and in Si to develop various photonic components and subsystems. Wafer bonding-based hybrid integration can overcome the lattice mismatch constraint significantly. By varying Si waveguide geometry and arrangement of the Group III-V layer, fabrication of electrically pumped laser, optical amplifier, modulator and photo detector are possible [7]. However, present research is leading towards CMOS-compatible monolithic integration of all photonic devices on the same chip.

Significant progress has been made to mitigate fabrication challenges in the last few decades to realize photonic waveguides on SOI. Effective and low cost light sources and modulators, efficient coupling between micro or nano waveguides with fiber, miniaturization of photonic integrated circuits (PICs), low stress, versatility, and scalability to mass production have been some areas of continuous research and progress. Along with diverse waveguide structures, different materials are grown on Si to realize Si-based devices: for example, SiO2, SiON, polymers, Ge, Si3N4 and Group III-V semiconductor materials [8-10]. SOI has emerged as a potential platform to realize monolithic integration of PICs which takes advantage of well-established commercial wafers made of a Si layer on top of buried oxide (BOX).

1.4 Si photonic components and applications

Major and basic building blocks of Si photonic integrated circuit include a Si based laser, modulator, waveguide, amplifier, Si compatible photodetector and coupler. Light generated from a Si laser is directed towards a Si modulator through waveguides. The modulator then encodes the signal into light and the modulated output is carried by waveguides towards its destination where the optical signal is converted back to electrical signals by photodiodes for further processing. Depending on the nature of the application, there are many other activities
including amplification, filtering, spot size conversion and coupling, which are performed by modifying architecture and exploiting inherent properties of Si. These components can be broadly classified as passive and active Si devices, depending on the operational requirements of the energy sources. Fig. 1.3 shows a cross-sectional view of few basic Si photonic components in PICs.

The initial stage of Si photonics research involves focusing the individual proof of concept devices including building block circuits, solving fiber to waveguide coupling, realizing fabrication tolerances and feasibility, creating analogous photonic components previously established on III-V material platforms and so on [11, 12]. However, nowadays there are major efforts dedicated towards optimization of existing components, realization of a monolithically integrated optoelectronic platform, expansion of functionality sets, fabrication improvements and further miniaturization.

![Cross-sectional view of few basic Si photonic components in PICs](image)

Additional to the basic Si photonic components described above, Si based waveguides are utilized to explore numerous other photonic applications including dispersion compensation, dispersion manipulation, pulse compression, supercontinuum generation, polarization rotation, mode conversion, switching, slowing light, wavelength conversion and soliton generation. Along with mitigating fabrication challenges, continuous research is still carried out to realize low loss, highly efficient, broad bandwidth and miniaturized design solutions of CMOS compatible Si waveguides for various such applications.
1.5 Research motivations

The research goal of this thesis is to investigate design options and pathways for improvements towards realization of monolithic integration of CMOS-compatible optoelectronic devices suitable for high speed applications. Investigation, characterization and new design for improvement of different miniaturized Si waveguides to fit for specific applications achieving low loss and high performance are the main focus points. One such application where miniaturized waveguides are expected to be used is photonic time stretched analog-to-digital converter (TS-ADC).

The real-time capture and processing of ultrafast electrical signals in wideband communications, image processing, THz detection etc. require ADCs with a sampling rate of 100 GS/s or more. Although, electronic ADCs are continuously evolving with the aid of CMOS technology combined with parallel processing, it cannot meet the incremental demands in sampling rates due to electronic bottlenecks including comparator’s ambiguity, clock jitter and mismatches in parallelism. The time-stretched (TS) technique as shown in Fig. 1.4 is one of the photonic approaches which can substantially overcome these bottlenecks [14, 15]. Here, a single shot ultra-fast RF signal is impressed onto a wideband chirped optical pulse using an optical modulator. The modulated pulse is then stretched in time while propagating through optical fiber utilizing its dispersion effect. The stretched optical pulse illuminates a photodiode and is then directed to an low speed electronic ADC. Comparator ambiguity, jitter and inter-channel mismatch can be reduced with time-stretch as the electronic ADC now needs to digitize slower signals.

![Fig. 1.4: Schematic of Time Stretched ADC technique](image)

However, the long fiber required for dispersing and stretching the white light is unrealistic for single chip integration and we propose to replace it with Si waveguides. Realization of such dispersive Si waveguide will allow the development of such photonic ADCs on a CMOS-
compatible chip so that both the electronic and optical processing can be co-developed monolithically on a single Si-substrate. However, optical properties of miniaturized devices are highly dependent on waveguide geometry and can be altered for small changes which may crucially affect specific applications. These crucial changes may set strict restrictions on fabrication tolerances and should be handled carefully. Using the TS-ADC as a target application, design trade-offs involved in the design of suitable waveguides meeting required dispersion profiles need to be thoroughly investigated. These investigations are also essential in numerous other applications including dispersion compensation, pulse compression, supercontinuum generation, dispersion manipulation, zero dispersion transmission.

Replacement of the fibers in TS-ADC design requires highly dispersive Si waveguides which may not be achievable with commonly used passive Si waveguides. This leads to the investigation of tailoring dispersive properties in active Si waveguides. Here, to attain required changes in the RI and corresponding changes in optical properties, biasing and doping profiles need to be well controlled. Active control in highly doped Si waveguides can also lead to significant loss due to absorption. Again, inadequate separation of the metal contacts from the waveguiding core may severely attenuate the guided mode and so need to be carefully designed. Along with searching for highly dispersive active Si waveguide, investigations of various distinctive guiding parameters by incorporating changes in physical dimensions, carrier concentrations and bias voltages are important to achieve different other applications including electro-optic modulation, optical switching, filtering and slowing light.

Another essential component for on-chip implementation is a CMOS-compatible photo detector. Due to the poor responsivity of Si around short and long haul telecommunication bands, Germanium (Ge) is utilized as the active material. Ge has a 4.2% lattice mismatch with Si and creates challenging obstacles towards monolithic integration. At the same time, various characteristic parameters such as the dark current, photo current, responsivity, transient response, and bandwidth of the photo detector highly depend on geometry and applied reverse voltage. Therefore, it is worthwhile to investigate these interdependent characteristics which are important before making any educated decision to meet specific requirements.

To realize various applications, it is important to couple light from fiber to Si waveguide or vice versa. However, large mode-field differences between the two make it difficult to couple light from one another. Various coupling mechanisms, which are primarily divided into butt and grating couplers, are proposed to combat this challenge. A typical structure of butt couplers is also shown in Fig. 1.5 (a), where the thickness and width of the Si waveguide at the coupling region are increased considerably to a cross-section comparable to that of the fiber, which enables effective coupling with Si nanowire. On the other hand, grating couplers as shown in Fig. 1.5 (b), which mostly perform out of the plane coupling between fiber and waveguide, are
found to be quite attractive as light can be coupled in and out everywhere on the chip, opening the way for wafer-scale testing. Although, the grating coupler is considered friendlier for wafer scale testing, it exhibits low efficiency and bandwidth. Oppositely, butt couplers are preferred for low loss and wideband coupling operations, although it often requires post-fabrication processing for accurate polishing and dicing to taper the waveguide edges. Butt coupling also suffers from back reflections due to a higher index contrast between fiber and the Si core. To overcome these, an alternative approach to tunnel and widen the optical mode from an adiabatic taper is proposed. However, the proposed approach relies on a rectangular SiON polymer core, which causes a portion of light to be wasted instead of being transferred to the adiabatic taper. This wastage of light restricts such structure to achieve higher coupling efficiency and requires further modifications of the spot size converter structure. Hence, an optimal mechanism needs to be devised to offer a compact coupler design with low loss, high coupling efficiency as well as large operational bandwidth.

Fig. 1.5: Typical structure of coupling techniques; (a): Taper based butt coupling, (b): Grating based coupling.

Photonic integrated devices based on SOI nanowires are usually severely polarization-sensitive because of the structural birefringence [16]. Due to anisotropy in cross-sectional geometry or stress distribution, guided TE and TM modes behave differently in waveguides and therefore
require polarization management, such as polarization rotation. Such polarization rotators are essential for polarization-insensitive Si nanowire based planar light wave circuit (PLC) devices [16]. For example, inserting polarization rotators in the middle of arrayed waveguides can achieve a polarization insensitive arrayed waveguide grating (AWG) de-multiplexer [17]. In this way, the TE and TM polarizations will be converted to each other while going through the inserted polarization rotator and thus the light path difference between two adjacent arrayed waveguides for both polarizations will always remain the same.

Compared with Group III–V waveguides of similar dimensions, polarization rotators made of SOI waveguides provide stronger optical confinement and also can be fabricated at relatively low cost. Device length of polarization rotator is a critical parameter. Although longer length provides higher efficiency, from the viewpoint of integration, it needs to be as short as possible. Simultaneous achievement of high conversion efficiency, low loss, high bandwidth and high tolerance to fabrication imperfections are desired for such devices to realize large scale Si photonics integration. However, finding an ultrashort device length with low loss and very high operational bandwidth is still a challenge.

1.6 Thesis Outline

The main objectives of this research are primarily related to the proposal, theoretical analysis and numerical evaluations of various Si based waveguides to create potential pathways for realizing a single chip solution of the TS-ADC target application. These include the thorough investigations of various passive and active Si waveguides to meet required design specifications and to find their inter-dependent phenomena. It also focuses on Si based photodiode and modifications of fiber to chip coupling solutions as well as compact and high bandwidth polarization rotator.

A brief description of each of the chapter is as follow:

Chapter 2: Literature Review

This chapter focuses on a review of the state-of-art Si photonics devices with a brief history of its evolution. Different photonic components are divided into passive and active waveguides and discussed separately including a brief insight into integration challenges and packaging. This thorough discussion gradually sets the research objectives of this thesis including its various scopes. This also provides in-depth backgrounds to the key theory behind the Si photonic integrated circuit applications as well as introduction to design components that are required for photonic TS-ADC to be realised in single Si chip.
Chapter 3: Tailoring Photonic Properties of Different Passive Silicon Waveguides

Using the photonic TS-ADC as a target application, design trade-offs involved in the design of suitable waveguides to meet required dispersion profiles are thoroughly investigated. Results of a systematic evaluation of the most popular forms of passive Si wire, rib and photonic crystal waveguides with and without bends are presented and analysed. Through numerical simulation, Si photonic waveguide designs are compared in meeting target application requirements in terms of their group velocity dispersion and mode loss across 1.2 to 1.6 μm wavelength ranges. These investigations are also essential in numerous other applications including dispersion compensation, pulse compression, supercontinuum generation, dispersion manipulation, zero dispersion transmission.

Chapter 4: Geometry and Depleting Carrier Dependence of Active Silicon Waveguide

Replacement of the fibers in TS-ADC design requires highly dispersive Si waveguides which is not achievable with commonly used passive Si waveguides. Using the photonic TS-ADC as a target application, this chapter continues to investigate the optimal design solutions to meet required dispersion profiles, but with active Si waveguides. It brings a PIN structure with planar and 1D PhC to characterize guiding parameters including perturbation in real RI, mode loss, group velocity dispersion and bending loss. Along with searching for highly dispersive active Si waveguide, investigations of various interdependent distinctive guiding parameters are important to achieve different other applications including electro-optic modulation, optical switching, filtering and slowing light.

Chapter 5: Geometry Dependence and Performance Optimization of Photodiode

Photodiode (PD), which is an essential component of PICs, has been investigated in this chapter. It considers a vertical n-i-p photo diode (PD) to characterize dark current, photocurrent and responsivity by incorporating changes in physical dimensions and bias voltages. Distributed Bragg reflectors (DBR) are introduced at the end of the Ge layer to reflect back the residual un-absorbed light, which effectively increases absorption length without adding any device capacitance. Transient behaviour including impulse and step responses and 3 dB bandwidth dependence on geometry and bias voltage are analysed. These can be instrumental in developing optimal design specifications for Si-based Ge photodetectors. The reduction of dark current with faster response in an InP/InGaAs uni-travelling carrier (UTC) PD is also investigated with elaborate discussions on transit time and RC limited bandwidth. An increase in transit time limited bandwidth is achieved with a graded doping profile instead of constant doping which enhances the electron transport towards intrinsic collection layer and decreases the transit time.
Chapter 6: Performance Enhanced Butt Coupling for Effective Interconnection
This chapter presents highly efficient inverted taper-based spot size converters to enable effective coupling between a single mode fiber and a Si nanowire. New structural designs are proposed by considering laterally- and vertically-tapered SiON polymer as a second core and its suitable placing to prevent a portion of the light from passing through the bottom cladding. The performance of the structure is characterized by distinct features including tapering length, coupling efficiency and coupling bandwidth. Considerable improvements in coupling efficiencies are achieved with these proposed modifications. Optimized coupling of light from and to a single mode fiber is also presented and compared with grating based couplers in terms of coupling length and bandwidth.

Chapter 7: Efficient Polarization Rotation in Si nanowire
This chapter presents the design and operation of a CMOS compatible polarization rotator based on asymmetrical Si waveguide. As we integrate many discrete functional blocks into a larger PIC suitable for applications such as TS-ADC, controlling polarisation within the PIC becomes a challenge. New structural designs are proposed by introducing 1D PhC structure. This structure achieves strict confinement of modes in the asymmetric structure which provides a large difference in the effective RI of two fundamental modes and substantially reduces the rotation length. Additional to these modifications, a novel approach of lateral tapering is introduced in the rotator device which further reduces the device length. Less than 4 μm rotator length is achieved with this design, which makes the polarization rotator suitable for compact and dense integrations. This also achieves very high operational bandwidth of 800nm with more than 90% conversion efficiency which covers the entire short and long haul telecommunication bands.

Chapter 8: Future Works and Concluding Remarks
This chapter draws the conclusions of the key findings carried out in this research. Following on the key conclusions of the research, outstanding issues identified during the course of the research is presented as a future work to provide some inspiration for further research in this exciting area.
1.7 Main findings and contributions

The major contributions stem out of this research are mainly related to design trade-offs involved in the design of suitable passive and active waveguides meeting required dispersion profiles to realize single chip solution of TS-ADC target application. Along with highly dispersive Si waveguide, systematic numerical investigations of various distinctive guiding parameters are also presented which are essential for different Si photonic applications. Photodiode (PD), which is an essential component of PICs, has been proposed with modifications in the structure and doping profile. Another major contribution of this research is the proposal of new structural design to modify the conventional butt coupling structure. This also proposes innovative designs for polarization rotator by introducing 1D PhC structure, replacing Si core by SiN and lateral tapering in the rotator device to achieve modifications in device length and conversion efficiency. Following are the chapter-wise main contributions originated from this research. Detailed publications from this work are listed in Section 1.8.

Chapter 3:

- Proposal of the implementation of a photonic TS-ADC on a CMOS compatible chip by replacing long fiber with highly dispersive Si waveguide.
- Validation of the TS-ADC technique with simulations using VPI platform for time limited input RF signals.
- Thorough investigation of design trade-offs involved in the design of suitable waveguides to meet required dispersion profiles for the target application over 1.2 to 1.6 μm short haul and long haul telecommunication bands.
- Systematic evaluation of the most popular forms of passive Si wire, rib and photonic crystal waveguides with and without bends.
- Investigation of interdependent phenomena of different optical properties such as effective RI, mode loss, dispersion and bend loss with changes in waveguide dimensions. Other than TS-ADC, these are essential in numerous applications including dispersion compensation, pulse compression, supercontinuum generation, dispersion manipulation, zero dispersion transmission.
- Evaluation of suitability of these passive Si waveguides to replace the long fiber in photonic TS-ADC application.
Chapter 4:

- Proposal of utilizing active Si waveguide to replace the long fiber in the implementation of photonic TS-ADC, as investigated passive Si waveguides in chapter 3 do not provide sufficient dispersion.
- Systematic evaluation of PIN structures with planar and 1D PhC with changes in waveguide dimension, doping concentration and applied biasing.
- Analysis of allowable limits of doping concentrations and biasing to achieve higher changes in RI and dispersion profiles with and without waveguide bends.
- Analysis of various structural design considerations. For example, utilization of higher p density compared to n density to achieve higher changes in desired properties without adding any extra loss, right placement of source and drain to avoid overlapping of a guided mode with highly doped regions near metal contacts.
- Investigation of interdependent phenomena for various distinctive guiding parameters including perturbation in real RI, mode loss, group velocity dispersion, and bending loss in depletion mode operations. Other than TS-ADC, these are essential in numerous applications including electro-optic modulation, optical switching, filtering and slowing light.
- Evaluation of suitability of these active Si waveguides to replace the long fiber in photonic TS-ADC application.

Chapter 5:

- Evaluation of geometry dependence and performance optimization of CMOS-compatible Ge on Si vertical photodetector including a lateral spot size converter for PICs.
- Proposal of introducing distributed Bragg reflectors (DBR) at the end of the Ge layer to reflect back the residual un-absorbed light: this effectively increases absorption length without adding any device capacitance.
- Validation of the proposed design and performance characterization of distinct features including dark current, photocurrent and responsivity by incorporating changes in physical dimensions and bias voltages.
- Analysis of transient behaviour including impulse and step responses and 3 dB bandwidth dependence on geometry and bias voltage.
- Investigation of InP/InGaAs uni-travelling carrier (UTC) PD for further reduction of dark current with elaborate discussions on transit time and RC limited bandwidth.
• Proposal of further increase in transit time limited bandwidth with a graded doping profile instead of constant doping: this enhances the electron transport towards intrinsic collection layer and decreases the transit time.

Chapter 6:
• Evaluation of coupling efficiencies of CMOS-compatible lateral and vertical spot size converter (SSC) for interfacing a Si nanowire waveguide with single mode fiber.
• Systematic evaluation of limitations of a conventional butt coupling structure which incorporates a low index second core on top of a Si adiabatic taper to tunnel and widen propagating optical modes.
• Proposal of new structural designs by considering laterally- and vertically-tapered SiON polymer as a second core and its suitable placing to prevent a portion of the light from passing through the bottom cladding.
• Validation of the proposed design and performance characterization by distinct features including tapering length, coupling efficiency and coupling bandwidth.
• Evaluation of the proposed design to couple light from and to a single mode fiber and comparing with grating based couplers in terms of coupling length and bandwidth.

Chapter 7:
• Systematic evaluation of limitations of polarization rotator based on asymmetrical Si waveguide through numerical simulations.
• Proposal of new structural designs by introducing 1D PhC structure. Detailed investigation of the proposed design to estimate modifications in device length and conversion efficiency.
• Introduction of a novel approach of lateral tapering in the rotator device to further reduce the device length.
• Utilization of CMOS compatible SiN/SiO$_2$ waveguide design.
• Validation of the proposed design and achievement of <4μm rotator length: this makes the polarization rotator suitable for compact and dense integrations.
• Achievement of very high operational bandwidth (>700nm) with more than 90% conversion efficiency: this covers the entire short and long haul telecommunication bands.
1.8 Publications

Publications made during the PhD candidature are listed in two categories. In the first category, publications directly related to this thesis are listed and includes some submitted papers. In the second category, other publications are documented.

1.8.1 Publications directly related to this thesis

1.8.1.1 Journal Papers


1.8.1.2 Submitted and prepared to submit papers:


1.8.1.3 Conference papers


1.8.2 Other Publications

1.8.2.1 Journal papers


1.8.2.2 Submitted and prepared to submit:


1.8.2.3 Conference papers


Chapter 2

Literature Review

2.1 Introduction

The revolution in microelectronics and photonics has transformed computing, communications, information science and engineering within the comparatively very short period of the last few decades. Microelectronics and photonics are together one of the most influential areas of engineering that has played such a persuasive as well as dramatic role in the way we live. The key material behind all these is Si which is one of the most abundant elements on earth with simple cubic crystalline structure. Si wafers, having incredible purity, hardness and good thermal conductivity are suitably fit for semiconductor devices. The intrinsic bandgap of Si (1.1 eV), its high RI and transparency at desired wavelengths (1270 nm to 1625 nm) makes it a favourite for optical communication applications. The high index of Si endorses the downscaling of any device footprint to the order of submicron and nanometer sizes [18]. Moreover, matured CMOS technology from microelectronics is readily available for low cost mass production of Si photonic devices. All these benefits make Si a promising solution for opto-electronic integration.

In just the last few years, Si has evolved into a functional platform for PICs. All of the basic building blocks of photonic systems shown in Fig. 1.3, including waveguides [19], modulators [20], detectors [21] and couplers [22] have been demonstrated. Lasers are the most power hungry and challenging component to be integrated in the PIC [2]. However, it has been integrated through a variety of mechanisms, ranging from bonding to epitaxy to package level integration [23, 24]. Nowadays major efforts are dedicated towards optimization of existing components, realization of a monolithically integrated optoelectronic platform, fabrication improvements and further miniaturization. Along with these, continuous research is carried out to realize low loss, highly efficient and broad bandwidth design solutions for various applications. The goal of constructing complex PICs is rapidly becoming the new reality.

This chapter focuses on a review of the state-of-art Si photonics devices with a brief history of its evolution. Different photonic components are divided into passive and active waveguides and discussed separately including a brief insight into integration challenges and packaging. This thorough discussion gradually sets the research objectives of this thesis including its various scopes. This also provides in-depth backgrounds to the key theory behind the Si photonic integrated circuit applications as well as introduction to design components that are required for photonic TS-ADC to be realised in single Si chip, which was the key inspiration for the research focus of the thesis.
2.2 History

The invention of the transistor in 1947 at Bell Laboratories (USA) and, about a decade later, subsequent development of the integrated circuit (IC) revolutionized the electronics industry. Since then, the main research trend has been to realize continuously smaller, faster, reliable and cost-effective ICs and various tremendous successes in turn have achieved remarkable research and manufacturing investments in academy and industry. The degree of miniaturization, which is the number of devices crammed onto a Si chip, reflects the progress in microelectronics and has been increasing exponentially. This has created several generations of IC technology such as small scale integration (SSI), medium scale integration (MSI), large scale integration (LSI), very large scale integration (VLSI), and ultra large scale integration (ULSI) [25]. As this continues, the dense integration of electronic devices has approached an interconnect bottleneck. With continuous increasing requirements of bandwidth, parasitic effects in metallic interconnection hinders further improvements, since signal attenuation and power dissipation increase sharply with higher data rate. On the other hand, photonics can achieve many things better than electronics. For example, it has huge bandwidth, very little transmission loss, is immune to cross-talk and electro-magnetic interference, and does not dissipate heat. Benefiting from the photonics domain combined with matured Si-based microelectronics technology, Si photonics has emerged as a potential solution and has been extensively researched for several decades.

The first nanoscale Si waveguide was demonstrated by Soref and Lorenzo [26] in 1985 and emerged as a potential platform for chip-scale photonic devices. Initiated by Soref and Petermann in the late 1980s and early 1990s [27, 28], Si photonics has expanded rapidly with considerable progress generally in passive devices. Si electronic and photonic integrated circuits (EPIC) was envisioned by Abstreiter and demonstrated in 1993 [29]. Its development was stymied by the inefficiency of light emission in Si and there was little progress in the field until 2003. However, research has been thriving since 2004, in both the industrial and academic realms and was boosted by Defense Advanced Research Projects Agency (DARPA) in 2004 with projects on EPIC to monolithically integrate VLSI electronics with nanophotonics in one chip by utilizing the CMOS platform [1]. The Si Heterostructure Intersubband Emitter (SHINE) program was created after DARPA contributed in quantum cascaded structures. However, the recent blast in Si photonics research has been mainly driven by EPIC chips, photonic integrated circuits (PICs) as well as by discrete photonic devices and hybrid integration techniques. Various specialized companies involved in such research include Intel, IBM, HP, Bell Labs, Luxtera, Kotura, Lightwire and NTT, which are all engaged in exciting developments in active and passive Si photonic components. As a result, these advances of the Si photonics platform are progressively exploring applications in various fields as shown in Fig. 2.1.
Out of these numerous applications, the goal of this research is to investigate design options and pathways for improvements towards realization of monolithic integration of CMOS-compatible optoelectronic devices suitable for high speed ADC. The subsequent sections provide in-depth backgrounds to the photonic ADC options for high speed applications as well as thoroughly discuss state-of-art design solutions of various Si photonic components. This motivates to investigate, characterize and propose new design for the improvement of different miniaturized Si based devices.

2.3 Photonic analog-to-digital converter (ADC)

The requirement of high speed ADC is increasing rapidly for the real-time capture and processing of ultrafast electrical signals. To meet the demand, electronic ADCs are continuously evolving with the aid of CMOS technology combined with parallel processing. Unfortunately, in such parallel techniques shown in Fig. 2.2, mismatch among the digitizers becomes severe with the increment of frequency and is also not free from jitter in sampling clock. Performance of electronic ADC is limited by one or more of the following problems: jitter in the sampling clock, settling time of the sample-and-hold circuit, speed of the comparator or comparator ambiguity, mismatches in the transistor thresholds and passive component values [30].
Fortunately, Photonics with its inherent advantages of manipulating electrical signals has revealed different directions to digitize such ultrafast RF signals [31].

Utilization of photonic components to improve ADC performance started in early 1970s [33]. Different photonic properties utilized in ADC design include stretching through dispersive fiber [34], tunable optical filtering [35], fiber non linearites including polarization rotation [36], cross-phase modulation (CPM) [37], self-phase modulation (SPM) [38], four wave mixing (FWM) [39]. Depending on sampling and quantization processes photonic ADCs can be classified in four major categories [40]. These are: (a) photonic assisted, electrically sampled and quantized [40], (b) photonic sampled and electrically quantized [41], (c) photonic quantized and electrically sampled [42], (d) photonic sampled and quantized [43]. Among these, research in sub-groups (a) and (b) have gained particular interests due to its simplicity and potentials of commercial development.

Photonic sampled and electrically quantized ADC is first introduced by using mode locked laser and electro-optic modulator [44], which is later modified by Optical Demux and parallel electronic digitizers to enhance sampling rate as shown in Fig. 2.3 [45]. However, high speed performance is minimized here due to limited sampling and repetition rate of mode locked laser. Later, this approach is modified by exploiting the benefits of mode-locking, continuous chirped pulse and optical demultiplexing using tuneable filters for continuous operations [46]. But, non-uniform conversion in low-speed ADCs and the sample memory effect which requires strict monitoring and feedback control of the WDM filters, limit its performance.
In early 1978, optical clock pulse shorter than 10 ps was used in opto-electronic switches for electrical sampling [47]. Opto-electronic switches have quick rise time and minimum pulse to pulse jitter but the turn off time is not adequately short for high frequency applications. Although a diode bridge circuit provides solution in some extent, it cannot integrate ultra-stable mode-locked laser. A high speed opto-electronic digitizer is proposed which uses an optical pulse replicator to convert a single signal into a series of time-delayed copies and allows a low-rate ADC to sample the repetitive pulses [48]. However, as the optical link causes imperfect replication, only a few GS/s resolutions are possible to achieve. To overcome this limitation, a new time stretching approach by exploiting dispersive characteristics of fiber is developed as is shown in Fig. 1.4 [15]. As is explained in Section 1.5, Electrical limitations including comparator ambiguity, jitter, inter channel mismatch are greatly reduced in this approach, as the actual digitizer embraces lower speed version of actual high speed signal.

In this TS-ADC technique, few kms of fibers are required for dispersing and stretching the white light and the modulated signal. This is not realistic for single chip integration and we propose to replace it with dispersive Si waveguides. Realization of such dispersive Si waveguide will allow the development of such photonic ADCs on a CMOS-compatible chip so that both the electronic and optical processing can be co-developed monolithically on a single Si-substrate. Rest of this chapter reviews different state-of-art Si photonics devices which are essential for target PICs and investigates different limitations of existing solutions which have been addressed and modified in subsequent chapters. Depending on the requirement of external biasing, these devices are discussed separately as passive and active waveguides.
2.4 Passive devices

Passive devices are the key components of PICs which operate without any biasing and include waveguide, spot size converter, couplers, polarization controller, ring resonator, Mach-Zehnder interferometer and Bragg grating. This section provides in-depth backgrounds to the key passive devices behind the Si PIC applications.

2.4.1 Si waveguide

The waveguide is the most basic form of passive device through which light is transferred from one point to another. Out of many Si-related materials that form the waveguide, silica (SiO$_2$) is most common. Doping ions into silica allows the required change in the RI and makes it suitable to use as a core and cladding with necessary index contrast [49]. Although the alteration in the RI can be tailored by changing the doping density, low RI differences in the core and cladding suffer from weak confinement and result in a thick cladding layer and wide spacing between waveguides [50]. Fortunately, the invention of SOI in the late 1980s resolved these problems and provides an excellent platform for Si/SiO$_2$ waveguides. Due to their large RI contrast, light can be confined strictly in the core and also the size of the waveguides are scaled down to nanometre range.

Evaluating factors of a specific type of waveguide are its size and propagation loss. Downsized Si waveguides offer potential platform for miniaturized ICs and dense integration, but they also cause deviations from ideal characteristics due to insufficient fabrication tolerances. Propagation loss can be caused by intrinsic waveguide properties such as carrier absorption in doped waveguides and by extrinsic waveguide properties such as tight confinement of mode in a smaller dimension and scattering due to surface roughness [51]. Compared to other guiding platforms, SOI encouragingly provides low surface leakage radiation loss where a buried oxide layer provides the necessary isolation to the guided mode. An early demonstrated single mode rib waveguide with dimensions of several microns [52] was reduced gradually with strip or channel waveguide structures [53]. However, such reductions in dimension to the micron or sub-micron scale strongly influence the light propagation due to surface roughness [54, 55]. Extensive research has been conducted to explore suitable fabrication procedures to achieve minimum losses.

Surface roughness has been effectively reduced by a thermal oxidation process where interface roughness is improved through high temperature and longer oxidation times [20, 56]. However, this process results in residual stress in Si. Other attempts to suppress scattering include surface encapsulation and temperature annealing [57] where enhancing the mobility of the Si atom smooths surface roughness. But these processes also suffer from harsh processing conditions, such as high temperatures. They may also lack selectivity, especially in dense
integration. Another approach is to use self-perfection by liquefaction (SPEL) which reduce surface roughness from 13 to 3 nm and also provides ultrafast processing [58]. Although the high index contrast of SOI platform is advantageous for its strong light confinement capability, it suffers from large birefringence which is caused by cross sectional geometry or stress level and results in an effective index difference of TE and TM polarizations [59]. Although, zero birefringence is almost impossible due to fabrication limitations, cladding stress via photoelastic effect can control and reduce it [60, 61].

2.4.1.1 Si waveguide properties and applications

Inherent optical properties of Si waveguides are utilized to explore different applications. As second order nonlinear susceptibility is weak in Si, third order optical nonlinearity is utilized for exploiting wavelength conversion [62]. The utilization of self-phase modulation to generate a continuum of wavelengths on a Si chip and its limiting nature is addressed in [63, 64]. Optical solitons have been observed by controlling nonlinear and dispersion effects where higher-order solitons allow pulse compression [65-67]. Another application of slowing light in Si waveguide leads to the development of optical buffers, filters, memory elements and so on, suitable for optical interconnects [68].

Dispersive effect in Si waveguide has been investigated which has potential applications in dispersion manipulation, pulse compression, supercontinuum generation, dispersion compensation and so on. Group-velocity dispersion (GVD) in Si waveguides is tuned from -2000 to 1000 ps/(nm·km) by tailoring the cross-sectional size and shape of the waveguide [69]. Dispersion tailoring in telecommunication wavelength in Si nitride rib waveguides are studied for different waveguide heights [70]. Analysis and engineering of chromatic dispersion in waveguide bends shows dispersion change up to 1000 ps/(nm·km) for different bending radius [71]. Dispersion manipulation and compensation is more elaborately investigated with PhC structures. Positive and negative dispersion in the order of 100 ps/(nm·km) on a bandwidth of 100 GHz based on modes anti-crossing in PhC line defect waveguides are presented in [72]. Again, two cascaded PhC line defect waveguide structure is used to reduce GVD and is tuned to obtain two matched dispersion relations [73]. Geometry-dependent GI and GVD parameters of PhC waveguide were optimized to achieve flattened dispersion band as well as zero dispersion wavelengths in [71, 74-76]. Recently, the use of Si$_3$N$_4$ as cladding instead of SiO$_2$ or air is investigated to allow waveguide dispersion engineering, while to mitigate the wavelength dependence [77].

Another important aspect of these Si waveguides is bending which is an important part of an integrated design and allows several optical functionalities in a single Si chip [78]. The incorporation of Si-Oxy-Nitride (SiON) and Si-on-Insulator (SOI) technologies can effectively
reduce the bending radius to a few microns [79], although such narrow bending increases propagation loss and introduces significant changes to dispersion profiles [71]. Enhancement of transmission in PhC waveguide bends has been carried out through extensive research in recent years [80, 81]. An organized design of high bandwidth PhC waveguide bends with low dispersion is investigated in [82-84].

Most of these investigations are, however, limited to specific type, geometry and operating wavelength of the waveguide, and have focused on realizing a particular feature only. Optical properties of miniaturized devices are highly dependent on waveguide geometry and can be altered for small changes which may crucially affect specific applications. Most popular forms of passive Si waveguides with and without bends need to be further analysed to investigate design trade-offs involved in meeting required dispersion profiles for TS-ADC application. Trade-offs between high mode loss in various waveguide bends and achievable dispersion should be investigated thoroughly. These investigations are also essential in numerous other applications including dispersion compensation, pulse compression, supercontinuum generation, dispersion manipulation, zero dispersion transmission.

2.4.2 Coupler

One of the key challenges with submicronic waveguide devices is to enable efficient coupling with fiber, which is caused mainly due to the mode-field differences between fiber and waveguide, and the relative misalignments. Various coupling mechanisms, which are primarily divided into grating and butt couplers, are proposed to combat these challenges [85-87]. Typical structures of such couplers are shown in Fig. 1.5. Grating couplers, which mostly perform out of the plane coupling between fiber and waveguide, are found to be quite attractive as light can be coupled in and out everywhere on the chip, opening the way for wafer-scale testing [22, 88-90]. Experimental demonstration of a grating-based coupler shows efficiency of more than 65% at 1550 nm [91]. Several approaches to improve the coupling efficiency have been proposed, including the addition of bottom gold and backside aluminium mirror, advancement in fabrication tolerances, lithography and etching processes [92-97]. However, grating-based couplers are wavelength dependent, and they exhibit poor performance in both coupling efficiency and bandwidth compared to butt coupling.

Butt coupling with a tapered spot size converter (SSC) provides higher efficiency with wide band coupling, where the thickness and width of the Si waveguide is increased considerably to a cross-section equivalent to the fiber [98, 99]. Historically, butt coupling is preferred for low loss and wideband coupling operations, although it often requires post-fabrication processing for accurate polishing and dicing to taper the waveguide edges and also suffers from back
Recent demonstrations have been carried out to achieve low propagation and coupling loss, minimum tapering length, high transmission efficiency with enhanced bandwidth and so on [101, 102]. Performance is largely improved by refining the fabrication process which can afford the use of Si wire waveguides in practical optical devices [54, 101, 103, 104]. However, these schemes suffer from strong back reflection due to a large mismatch between fiber core and Si waveguide RIs and also require additional processing steps that complicate the fabrication [100].

Offering large misalignment tolerances and a low loss polarization independent operation, another approach to tunnel and widen the optical mode from an adiabatic taper to a polymer core was first proposed to facilitate laser to fiber coupling [105] and was recently demonstrated to couple light from and to Si nano wires proposed [106-108]. Confined mode in the waveguide is tapered to a narrow tip which is small enough to allow any propagating mode and thus it gradually tunnels to a wider core and can be efficiently coupled to single mode fiber (SMF). Gradual changes in the effective RIs of a Si inverse taper SSC can fall to those of optical fiber at the coupling ends and require no antireflection coatings. Demonstrations have been carried out to minimize back reflections, achieve low loss, optimize taper size, refine the fabrication process, increase coupling efficiency and so on [107-109]. A summary of a comparison of various existing demonstrations is presented in Table 2-1 for coupling light from fiber to nanowire waveguides.

Table 2-1: Performance comparison of SSC with existing demonstrations.

<table>
<thead>
<tr>
<th>Reference</th>
<th>Dimension of the second core (μm²)</th>
<th>Spot size expansion</th>
<th>Tapering length (μm)</th>
<th>Coupling efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[99]</td>
<td>5.1*9.2</td>
<td>200</td>
<td>2086</td>
<td>13</td>
</tr>
<tr>
<td>[105]</td>
<td>4.0*7.0</td>
<td>140</td>
<td>1000</td>
<td>49</td>
</tr>
<tr>
<td>[106]</td>
<td>3.0*3.0</td>
<td>100</td>
<td>200</td>
<td>44</td>
</tr>
<tr>
<td>[110]</td>
<td>5.0*1.5</td>
<td>71</td>
<td>60</td>
<td>66</td>
</tr>
<tr>
<td>[108]</td>
<td>3.4*3.4</td>
<td>70</td>
<td>300</td>
<td>63</td>
</tr>
<tr>
<td>[102]</td>
<td>3.0*3.0</td>
<td>70</td>
<td>175</td>
<td>65</td>
</tr>
<tr>
<td>[109]</td>
<td>2.0*2.0</td>
<td>40</td>
<td>150</td>
<td>79</td>
</tr>
<tr>
<td>[111]</td>
<td>1.3*1.3</td>
<td>18</td>
<td>195</td>
<td>50</td>
</tr>
<tr>
<td>[112]</td>
<td>2.0*0.34</td>
<td>4</td>
<td>15</td>
<td>20</td>
</tr>
</tbody>
</table>

These approaches rely on a rectangular second core, which causes a portion of light to be wasted instead of being transferred to the adiabatic taper. This wastage of light restricts such structure to achieve higher coupling efficiency and requires further modifications of the spot
size converter structure. Expansion of the guided mode from micro or nano waveguides to nearly fiber cross section is important for efficient coupling; however this comes at the expense of a longer tapering length. Most of the previous tapered butt couplers convert the size only around 3*3 μm² [102, 106, 108-111]. Again, a high spot size expansion which is the ratio of initial and converted spot size is expected with high coupling efficiency and lower tapering length. Hence, an optimal mechanism needs to be devised to offer a compact coupler design with low loss, high coupling efficiency as well as large operational bandwidth.

2.4.3 Polarization splitter/rotator

Due to anisotropy in cross-sectional geometry or stress distribution, guided TE and TM modes behave differently in waveguides and therefore require polarization management [113]. Polarization control can be achieved in a Si tapered waveguide, which is usually made long enough to be adiabatic so that the higher order modes are not excited [114]. This works well for low index-contrast waveguides but the situation becomes complicated for small waveguides with a high index contrast, e.g. submicron SOI waveguides [115]. Mode hybridization, which is significant in such high index contrast waveguides, influences the conversion between a fundamental TM mode and a first order TE mode at some special waveguide widths [116, 117]. Such conversions are not usually expected as these introduce excess loss as well as cross-talk [118]. On the other hand, to realize a polarization controller or splitter/rotator, this can be very useful [117, 119]. Polarization diversity technique is a more feasible solution compared to designing perfect polarization independent waveguides [120]. In this technique, a polarization splitter and rotator are key elements which are based on mode coupling or mode evolution principles [121, 122]. The mode coupling technique is sensitive to wavelength and fabrication processing as this requires precise coupling as well as phase matching. Alternatively, the mode evolution technique offers broad bandwidth and relaxed fabrication tolerances.

Fig. 2.4 shows the schematic of a broadband polarization splitter using an arrayed waveguide grating as demonstrated in [123]. This structure is based on an arrayed waveguide with matching path lengths and two output waveguides to capture TE and TM light. Polarization dependent phase difference is induced through stress in the waveguide cladding which results in spatial separation in focal points of outgoing beams. This particular design is completely passive, although splitters using external power sources or through geometrical modifications are also available [18]. Other polarization beam splitters based on various configurations include multimode interferometers (MMIs) [124], Mach-Zehnder interferometers (MZIs) [125], crystalline structures and directional couplers [126]. Again a low loss, high bandwidth, polarization independent and compact splitter by using tapered Si waveguide is demonstrated for large scale integrations [127].
A polarization rotator (PR) capable of rotating the optical axis is an essential component to realize polarization diversion and has been demonstrated by using thermal or electro-optical strain effects [128]. However, passive approaches to realize polarization rotation is preferred by considering relatively easy fabrication and cost effectiveness [129]. These approaches can broadly be classified based on two different design premises [130]. One is based on mode evolution with asymmetric cross sections [131-133] while the other incorporates birefringent sections [134]. As long as coupling to other modes is suppressed, a mode evolution technique can provide low loss solution. However, it requires a large device length for the rotation operation. On the other hand, use of birefringent sections can provide compact solutions but this method suffers from high loss due to the difficulty of matching the modes at the interfaces [130].

Polarization rotation by loading InP based rib waveguide in a periodic asymmetric way is demonstrated to achieve complete conversion, but requires a long device length (e.g. 3.7mm) and also lossy at the junctions of the alternating sections [135]. Polarization rotation in deeply etched semiconductor bends are also presented where the rotation length is reduced by careful adjustment of the waveguide width, the slant sidewalls and bending radius [136]. However, the conversion length is still high (e.g. 117μm) and the design is quite complex for fabrication. A polarization converter based on angled waveguides in Inp/InGaAsP by combining mode evolution and birefringent techniques keeps the device length as low as 50μm [130].
Although, initially researchers focused on demonstrating highly efficient PRs based on III-V materials, much attention has been given in recent years to Si-based rotators for CMOS compatibility as well as the possibility of achieving high integration density. An orthogonal polarization mode evolution with two attached core layers is presented to achieve Si-based PR, but it requires a relatively long device length (e.g. 100μm) [132]. Micrometric SOI ridge waveguides with slanted sidewalls are also used [137] but these suffer from fabrication complexity. PR based on an off-axis double core (Si wire and Si-oxinitride waveguide) structure offers relatively simpler fabrication procedures as well as lower device length of around 35μm [115], but the rotation angle is only 72 degrees. An integrated PR by forming a strip waveguide with an asymmetric trench on a SOI wafer is presented with a device length of 67μm [138]. Some recent demonstrations of hybrid plasmon based PRs offer much lower device lengths but sometimes suffer from high insertion loss [139, 140]. More compact design solutions are presented with device length of <10μm, but these struggle to achieve suitable operational bandwidth [141, 142].

<table>
<thead>
<tr>
<th>Year</th>
<th>Ref.</th>
<th>Structure (Based on)</th>
<th>Device length (μm)</th>
<th>Bandwidth (nm)</th>
<th>Conversion Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2013</td>
<td>[143]</td>
<td>InP</td>
<td>275</td>
<td>400</td>
<td>97</td>
</tr>
<tr>
<td>2015</td>
<td>[144]</td>
<td>SOI</td>
<td>100</td>
<td>200</td>
<td>96</td>
</tr>
<tr>
<td>2008</td>
<td>[129]</td>
<td>SOI</td>
<td>10</td>
<td>120</td>
<td>97</td>
</tr>
<tr>
<td>2016</td>
<td>[146]</td>
<td>SOI</td>
<td>8.2</td>
<td>104</td>
<td>98</td>
</tr>
<tr>
<td>2007</td>
<td>[130]</td>
<td>InP</td>
<td>50</td>
<td>100</td>
<td>93</td>
</tr>
<tr>
<td>2013</td>
<td>[147]</td>
<td>SOI</td>
<td>3.2</td>
<td>100</td>
<td>97</td>
</tr>
<tr>
<td>2005</td>
<td>[137]</td>
<td>SOI</td>
<td>98</td>
<td>100</td>
<td>87</td>
</tr>
<tr>
<td>2012</td>
<td>[148]</td>
<td>InP</td>
<td>1350</td>
<td>90</td>
<td>-</td>
</tr>
<tr>
<td>2010</td>
<td>[141]</td>
<td>SOI</td>
<td>9</td>
<td>80</td>
<td>95</td>
</tr>
<tr>
<td>2012</td>
<td>[142]</td>
<td>SOI</td>
<td>7.6</td>
<td>80</td>
<td>95</td>
</tr>
<tr>
<td>2014</td>
<td>[149]</td>
<td>SOI</td>
<td>576</td>
<td>80</td>
<td>-</td>
</tr>
<tr>
<td>2014</td>
<td>[150]</td>
<td>SOI</td>
<td>15.3</td>
<td>80</td>
<td>99</td>
</tr>
<tr>
<td>2011</td>
<td>[117]</td>
<td>SOI</td>
<td>100</td>
<td>70</td>
<td>98</td>
</tr>
<tr>
<td>2017</td>
<td>[151]</td>
<td>SOI</td>
<td>5</td>
<td>40</td>
<td>50</td>
</tr>
<tr>
<td>2011</td>
<td>[152]</td>
<td>SOI</td>
<td>44</td>
<td>40</td>
<td>92</td>
</tr>
<tr>
<td>2016</td>
<td>[153]</td>
<td>SOI</td>
<td>15.78</td>
<td>40</td>
<td>-</td>
</tr>
<tr>
<td>2011</td>
<td>[154]</td>
<td>InP</td>
<td>805</td>
<td>35</td>
<td>-</td>
</tr>
<tr>
<td>2016</td>
<td>[138]</td>
<td>SOI</td>
<td>67</td>
<td>20</td>
<td>-</td>
</tr>
</tbody>
</table>
A summary with various demonstrations is presented in Table 2-2 to compare the device length, operational bandwidth and conversion efficiency. Although, some of the demonstrations achieve considerable operational bandwidth, the device length is too high for compact PICs [130, 143, 144, 148, 149]. On the other hand, most of the demonstrations which achieve preferable device length are failed to offer high operational bandwidth [129, 141, 142, 146, 147, 151, 153]. Achieving simultaneously high PR efficiency, low loss, high bandwidth and high tolerance to fabrication imperfections is desired for such devices to achieve large scale Si photonics integration. Hence, finding an ultrashort device length with low loss and especially very high operational bandwidth is still a challenge.

2.5 Active devices

In contrast to passive devices, active devices require external energy source to operate. Key active devices in PIC include Si based lasers, Si modulators and detectors. In this section, brief descriptions of the present advances of these key active components are provided.

2.5.1 Lasers

In Si photonics, among the components of OEIC networks, the light source is the most power hungry and challenging part, and much research has been conducted to realize a Si laser. Providing an indirect bandgap, Si shows very poor emission property and requires special manipulation and engineering to achieve desired lasing. Different approaches towards this can be classified as employing quantum confinement effect, introducing rare earth impurity, raman scattering, hybrid integration with III-V material based lasers, and Ge lasers.

2.5.1.1 Emission in bulk Si

Unlike III-V materials, Si has an indirect bandgap structure where, the valley on conduction band is not lined up with holes residing in valance band. Conceptual direct and indirect energy band diagrams are shown in Fig. 2.5 [155]. In indirect bandgap structure, two major nonradiative processes limit the emission efficiency, known as Auger recombination and free carrier absorption (FCA) [51]. Auger recombination which is opposite of impact ionization, is the process where carriers are moved to higher energy level by absorbing released energy from electron hole recombination. On the other hand, FCA is a process where the free carriers in conduction band absorb photons and jump to higher energy states. Both of the cases increase rapidly with increased carrier density and the electrons residing in higher energy states discharge energy in the form of phonons, but not photons. However, resulting loss is much
higher than the gain and therefore, quantum efficiency is unexpectedly poor [156]. Although research has been carried out to improve this efficiency, but is not comparable to III-V materials. However, continuous attempts have achieved Si based lasers through special engineering as is described in next sections.

Fig. 2.5: Energy band diagram showing carrier transition process: (left) direct band structure results in light emission, (right) indirect band structure results in very poor light emission from [155].

2.5.1.2 Quantum confinement

As the nonradiative recombination in Si is swept compared to radiative recombination, it losses pumped energy to some Si defects in the form of heat. This problem can be successfully solved by quantum confinement effect. The size of Si crystal is reduced to nanometre level, where the carriers are localized with uncertain momentum [51]. This improves the radiative recombination probability and puts obstacles towards nonradiative diffusion while meeting defects in bulk Si. Use of Si nanocrystals has been a popular approach to achieve quantum confinement and this occurs naturally in Si rich oxide (SRO) thin film [157, 158]. Electrical pumping is also applied in MOS structures to observe electroluminescence with bipolar and unipolar injections [159, 160]. However, these observations are difficult to explain on the basis of electron localization and also highly dependent on sample preparation [2]. Additionally, the emission wavelengths are in the range of 800-900 nm, which is outside both short and long haul telecommunication bands. Another attempt at exploiting quantum confinement involve nanometre size holes etched into Si to form periodic nano patterned crystalline Si: this shows evidence of lasing at 1270 nm wavelength [161]. However, narrowing of the emission spectrum with higher pump power
reflects that the mechanism of lasing is from defects on etched Si surfaces [2]. Red shifting the emission band towards telecommunication wavelengths and increasing the stability is important in these approaches.

2.5.1.3 Doping with rare earth ions

Si based structures doped with rare earth ions like Erbium (Er) shows great potential for emitting light at telecommunication bands: this provide alternative solution for lasing. However, in reality, Si is a poor host of Er, which results in negligible emission at room temperature. As an alternative, Si nanocrystals have been used as sensitizer for Er ions and have successfully demonstrated for achieving both photoluminescence and electroluminescence [162]. Research shows the enhancement of photoluminescence by co-planting with other materials, whereas electroluminescence has been improved through device geometry and doping distributions [163]. Multilayer Er doped structures have shown promising results with higher emission efficiency compared to single layer [164]. However, these devices require high pumping power and throw challenges to realize on chip integrations.

Several demonstrations are reported to realize electrically pumped laser on Si [165, 166]. However, main obstacles in these approaches to achieve high emission are the FCA from carrier injection and low solubility of Er in Si rich oxide (SRO) which forms in Er₂O₃. As the dielectric constant of Er₂O₃ is higher than SiO₂, weak electric field cannot accelerate carriers effectively to excite Er ions [167]. So, decreasing threshold voltage and to realize room temperature operation is still a challenge [51]. Nevertheless, recently, electrically pumped Er doped light emitter is presented for on-chip routing of electroluminescence signal at 1.54 μm [168].

2.5.1.4 Si Raman laser

In Si Raman laser, Si acts as the gain medium by utilizing stimulated Raman scattering (SRS) effect. Gain coefficient of SRS in Si is around 10³ to 10⁴ times larger than in fiber and due to large index contrast, light can be confined in 100-1000 times smaller area compared to SMF [2]. These properties drive to use Si as the gain medium via Raman scattering. When light is incident on Si, two radiations with lower and higher frequencies than incident light are generated due to induced electric polarization, which are referred as anti-stokes and stokes transitions. If pump and signal are in resonant with stokes transitions, more Raman stokes generate and amplification is realized through SRS [169]. Though application of SRS attracted attention since 2002 [170], first Si Raman laser operating in pulsed mode was proposed in 2004 [169]. In next year, direct modulation on Si Raman laser [171], highly desired for monolithic integration as well as continuous wave lasing have been reported [172].
Main obstacle of SRS based Si active devices are the two photon absorption (TPA) and the subsequent free carrier absorption (FCA). At high pump intensity, effect of FCA becomes more significant and dominant loss mechanism [173]. Focusing on the reduction of carrier recombination lifetime, reverse PIN diode structure is suggested to sweep out the free carriers under reverse bias condition [174]. In addition, lifetime can be reduced by employing short pump pulse [169], or by defect engineering [175]. Some other approaches include decreasing volume-to-surface ratio to increase rate of surface recombination [176], and employment of bidirectional pumping scheme for effective loss reduction and output enhancement [177]. Recently, a unique design using PhC nanocavity shows continuous wave lasing with low threshold power of ~1 μW [178]. Si Raman laser also has promising applications in the fields of wavelength conversion and amplifiers [172]. However, requirement of optical pumping mechanism makes it impractical for CMOS compatible integrated solution [18].

2.5.1.5 Epitaxial growth III-V materials on Si

Another branch to obtain light sources is to grow Group III-V based materials (like GaAs, InP) on Si, which have direct bandgap [179-181]. However, main challenge here is to determine the fabrication procedures to overcome defects and power loss due to lattice mismatch between Group III-V materials and Si [182]. Moreover, direct growth of III-V materials on Si requires high temperature operation, which is detrimental to other components on same chip [164]. Again in high temperature, III-V materials gradually get resolved into Si layer, which then acts as dopants. To overcome this problem demonstrations to decrease growth temperature include on chip InGaAs nanopiller lasers grown at 400°C [183]. Direct molecule wafer bonding and adhesive bonding are also applied to grow high quality InP layers on Si in low temperature [184, 185]. Utilizing advanced epitaxial techniques, employment of SiGe [186], and GaSb [187] buffer layers have been demonstrated to realize GaAs based lasers on Si at room temperature, though the performance is not yet satisfactory.

2.5.1.6 Epitaxial growth of Ge on Si laser

Growth of Ge on Si is another novel approach which has high compatibility with CMOS processing. This makes it possible to achieve integrated devices such as laser, modulator and photodetector on the same Si chip. Although, Ge is an indirect bandgap material, it has a direct bandgap at 0.8eV: this covers the telecommunication wavelength range of 1550 nm. First theoretical idea of Ge based laser was proposed in 2007 explaining expected lasing and gain at 1550 nm [188]. However, was demonstrated in 2010 working at room temperature [189].
Band structure of Ge is modified by introducing tensile strain by thermal expansion mismatch, since it is not limited by critical thickness of Ge layer [190]. However, this causes the emission wavelength to shift to 2300 nm due to bandgap shrinkage under strain. This has been later modified with 0.25% tensile strain, which shows low threading dislocation defect [191]. But then, complete shift to direct bandgap is not achievable. This can be solved by introducing heavy doping by n-type impurities, which at the same time achieves high emission efficiency [192]. Hetero-epitaxial growth of GeSn and Ge on Si are also investigated for Si-based light emission [193, 194]. Continuous improvement and promising results indicate to achieve monolithically integrated Ge laser on Si using CMOS processing.

2.5.1.7 Hybrid lasers on Si

Hybrid integration by combining several materials on Si for lasing has gained interest over the years. Using wafer bonding technology, hybrid lasers made of other materials are grown on Si to realize on chip integration of optoelectronic devices [195, 196]. An example of lasing in Group III-V materials grown on Si is shown in Fig. 2.6 [197]. After first realization of hybrid laser in 2006, present research is mainly focused to increase emitting efficiency and friendlier wafer bonding processes [198, 199]. Novel integration technique by employing Si epitaxial growth in pre-defined trench with taper structure demonstrates narrow linewidth of 130 kHz with 1.5 mW output power [200]. Electrically pumped hybrid AlGaInAs-Si evanescent laser is demonstrated by showing continuous lasing at 1.8 mW output power and 100’s of such can be fabricated in one bonding step [11]. Another electrically pumped ring laser is fabricated with self-aligned process at 650°C [201]. Another approach of enhancing micro ring lasers is demonstrated by using multiple quantum well structure: this considerably increased the output power [202]. Very recently, fabrication of III–V/Si heterocore microcavity lasers is reported via ultrathin interlayer bonding and dual hard mask techniques and requires only one lithography process in the fabrication [203].

Fig. 2.6: Schematic of hybrid Si laser [197].
### 2.5.2 Modulators

An optical modulator is an essential part of a communications system and should offer high modulation speed with large bandwidth. Low loss, small size and ultralow power consumption are desired in an optimized design of Si based modulators. However, the linear electro-optic effect, which is the basis of LiNbO$_3$ modulators, is not present in Si. So the plasma dispersion effect is utilized as a viable solution to achieve faster modulation, where a change in free charge concentration changes the real and imaginary effective refractive indices (RIIs) [204]. Charge concentration can be varied by carrier accumulation in MOS structure, carrier injection in forward PIN structure or by carrier depletion in reverse PIN structure.

Based on carrier accumulation on a MOS capacitor, the first modulator was demonstrated in 2004 and achieved a bandwidth of 1 GHz [12]. With further progress in device design and material quality, data transmission up to 10 Gbit/s was attained [205]. Operational speed in case of injection is limited due to high recombination lifetime. Bit rates up to 10 and 18 Gbit/s are demonstrated using a Mach–Zehnder interferometer (MZI) and ring resonators respectively [206, 207]. Carrier concentration can also be varied by depletion operation in reverse bias, which is fundamentally a high-speed process. This also benefits from low current due to a reverse-biased diode and safeguards low power dissipation. Utilizing carrier depletion, 15 GHz 3 dB bandwidth is achieved in a lateral pin diode whereas a 30 GHz vertical PIN diode is reported with reduced active length and modulation depth [208, 209]. High-speed carrier-depletion Si Mach-Zehnder optical modulators with lateral PN junctions, which shows high speed operation up to 52Gbit/s is also presented [210].

![Fig. 2.7: Schematic of a SOH modulator from [211].](image-url)
CMOS compatible Si/Ge/Si modulator with a maximum operation frequency of 16 GHz using carrier depletion in Si is proposed. But, these are limited by tunnelling and thermoionic emission at SiGe/Si barriers. Later it is improved by using an all-Si structure to increase the intrinsic frequency up to 100 GHz at temperatures of 400k [212]. Modulators based on diode structures and embedded in ring resonator offer low power consumption and relatively low Vpp, since the light is effectively confined inside the resonator [213]. Different approaches of such modulators are a Si dual-ring modulator with cascaded rings and embedded pn junctions, cascaded uncoupled dual-ring modulator and a ring modulator from hybrid Si and lithium niobate [214-216]. Picowatt sensitivity, modulation bandwidth optimization, and linearity for analog optical links are also addressed and discussed in [217-220].

Si offers strong light confinement but its third order nonlinearities are too weak to realize direct modulation. Polymers have ultrafast nonlinear responses but their refractive index is relatively low. However, a different approach of Si organic hybrid (SOH) integration utilizing advantages of both materials has been proposed to realize Si modulators. An electro-optic effect achieved by an organic cladding having high non-linearity shows a 42.7 Gbit/s electro-optic modulator in Si technology [211] which can potentially operate at low voltages benefiting from the slot and socket configuration. A schematic of a SOH modulator is shown in Fig. 2.7 from [211]. Three different implementations of SOH comprising strip waveguide, slot waveguides and PhC slot waveguide structure are presented in [221]. EO modulators with 100 Gb/s speed is reported with organic cladding on a slow light SOI structure [222]. All these efforts suggest that SOH is a next generation solution of a high speed Si based modulator with low driving voltage.

2.5.3 Photodiodes

After processing and transporting the optical signal in a PIC, a photodiode (PD) converts it back into electrical form. Photons are absorbed by photosensitive material and converted into electron-hole pairs if photon energy is equal to or more than its bandgap energy. These are swept towards electrodes by applying electric field which produces electric current referred as photocurrent. Parameters to determine the performance of a PD include quantum efficiency, responsivity, response time, and detector noise [18]. Quantum efficiency refers to the ratio between the incident number of photons and the number of generated electron hole pairs. Responsivity is the ratio between generated photocurrent and incident optical power which is also wavelength dependent. The response time refers to the time required by a PD to react to an incident photon and is limited by the transit time of free carriers as well as by the RC time constant based on designed circuitry and geometry. This in turn implies the operating bandwidth
which increases with a faster response. Finally, detector noise includes shot noise, leakage and dark current from thermally-generated carriers and needs to be minimized for optimized photo detection.

Fig. 2.8: Absorption coefficients for various semiconductors [223].

Si is naturally transparent in the 1300-1600 nm wavelength range and so is not suitable for photodetection in the short haul or long haul communication bands. However, as absorption is possible below 1000 nm, Si has been demonstrated as X-ray or gamma ray detectors for biomedical and space imaging applications [224, 225]. As Si cannot be used in the telecommunication wavelength range, another material needs to be incorporated in the Si platform. Group III-V materials and Germanium (Ge) have been commonly used; these have excellent absorption capabilities in the wavelength range of interest as shown in Fig. 2.8 [223].

Based on structural differences, a Si PD can be divided into different categories such as Schottky metal-semiconductor-metal (MSM), p-i-n lateral, n-i-p vertical, and avalanche PDs. Another novel approach is a uni-travelling carrier (UTC) PD where only electron is swept as the active carrier to achieve smaller transit times and high bandwidth. In the following subsections, some major classes of PDs and the corresponding advances in research are briefly discussed.

2.5.3.1 Schottky PDs

Unlike typical p-n junction, Schottky detectors manipulate internal photoemissions over a Schottky barrier which is created by deploying a metal layer on a lightly doped Si waveguide and is determined by the kind of metal used, e.g. Au, Al or Pt. Incidental photons will be absorbed by the metal-Si junction which will generate the corresponding photocurrent if photon
energy is larger than the Schottky barrier. This barrier is generally below 0.6 eV for p-Si which offers the detection of photons with energy less than Si bandgap. Schottky detectors are advantageous for high switching speed and also possess simple fabrication which is compatible with standard CMOS processing. However, they suffer from low quantum efficiency caused by photon leakage in the metallic layer, although that efficiency can be increased with metal-semiconductor-metal structures [51]. Other approaches to enhance efficiency include resonant cavity structure [226], merging with dielectric [227], using transparent electrode [228] and deploying surface plasmon polaritons (SPPs) [229]. Both symmetric and asymmetric metal stripes in SSP-based detectors have been proposed for detecting light at 1550 nm wavelength [230, 231]. However, these detectors require further research to achieve improved responsivity.

### 2.5.3.2 III-V detectors

Detection of telecommunication band wavelengths can easily be realized by using III-V materials which possess a direct bandgap structure [232]. III-V material-based detectors are beneficial as they have wide absorption bandwidth and low dark currents [233]. Although previously these detectors were built on GaAs substrate, InGaAs detectors are now built on SOI substrate using a heterogeneous integration technique [234]. Quantum-well and quantum-dot structures are also applied to III-V PDs and enhanced performance in long infrared range with different temperatures are demonstrated for various commercial applications [235, 236]. Again, the two photon absorption (TPA) property in III-V materials is also investigated for low speed detection and can be used as an autocorrelator in laser pulse generation [237].

A small PD with a device footprint of only 50 μm² on SOI using InP membranes is demonstrated which is suitable for dense integration and also offers low power consumption with low junction capacitance [238]. Responsivity, dark current, and 3-dB bandwidth of this PD is achieved as 0.45 A/W, 1.6 nA at -4V bias voltage, and 33 GHz respectively. A demonstration of InAsAs-InGaAs MSM PD on SOI is reported which achieves responsivity of 1.0 A/W with 30 μm long detector length at 1550 nm wavelength [21].

### 2.5.3.3 Ge on Si detectors

Although III-V PDs are efficient for detection at telecommunication bands, enormous efforts have been made to achieve monolithic integration of PDs on Si. A potential candidate is Germanium (Ge) which has strong photon absorption capability in the entire communication wavelength range [5]. Ge growth on Si is also compatible with CMOS processing and thus allows monolithic integration [239]. However Ge has 4.2% larger lattice constant than Si, which creates tensile stain and results in density of dislocation defects and a high dark current.
Different methods have been demonstrated to reduce such dislocations and to increase detection bandwidth with high responsivity and reduced dark current.

While growing Ge on Si, the density of threading dislocations is reduced by using high-low temperature annealing cycles which generate stress within Ge epilayers and enhance annihilation of dislocations [240-244]. It is also proposed to counterbalance strain caused by Ge by incorporating a low lattice material, such as Carbon (C) and is further improved by multiple SiGeC layers as the absorber [245]. However, low solubility in Ge ($10^8$ atoms/cm$^3$) limits the C fraction to as low as 2–3% under metastable conditions. Reverse leakage current which depends on the electric field strength is also effectively reduced by inserting a thin intrinsic (i) Si layer between i-Ge and n-Si [246].

Dark current minimization has been approached in various ways including dopant segregation in NiGe which effectively modulates the Schottky barrier height [247]. Another approach of enhancing the Schottky barrier is reported with metal-Ge-metal PD fabricated on an amorphous Ge epitaxial layer grown on Si substrate [248]. Ge PDs fabricated with low temperature wafer bonding and an ion-cut process shows low dark current with quantum efficiency of 90% [249]. Further enhancement is achieved with optimization of growth process by low energy plasma enhanced chemical vapour deposition and thermal budget [250]. Low dark current for Ge$_{1-x}$Sn$_x$/Si p-i-n photodiodes is also reported by utilizing a sidewall surface passivation technique [251].

A vertical PD with n-i-p junction and a lateral PD with p-i-n junction are compared in terms of dark current, photo current, speed and bandwidth with and without Ge annealing [252]. The bandwidth and response time of a PD rely on applied voltage which reduces at low voltages [253, 254]. These speed of PDs can also be increased by optimizing the intrinsic region and is addressed in [255]. For high speed resonant cavity enhanced Ge PDs on reflecting Si substrate is proposed in [256]. An increment in responsivity and higher bandwidth of 29.4 GHz at -2V bias voltage is achieved by evanesently coupled Ge n-i-p vertical PDs grown on top of a Si rib waveguide [257]. A Ge/SiGe multiple quantum wells photodiode using surface-illuminated vertical p-i-n structure achieves optical bandwidth of 30 GHz at a bias of -7 V [258]. A Ge p-i-n PD integrated in a submicron SOI rib waveguide with reduced detector length of 15 μm shows 3-dB BW of 42 GHz at -4V bias voltage and 1550 nm operating wavelength [21]. 3-dB BW upto 49 GHz is also presented in a vertical Ge p-i-n PD grown by molecular beam epitaxy on bulk Si substrate [259]. Recently, a waveguide PD with bandwidth as high as 120 GHz, responsivity of 0.8 A/W was demonstrated, although with relatively higher dark current of 4 μA [260].

An avalanche PD (APD) is another type of popular detector which benefits from its internal multiplication property and exhibits 5 to 10 dB better receiver sensitivity with a larger gain bandwidth product compared to PIN structures. A large gain-bandwidth product of 340 GHz
and 845 GHz at 1310 nm and 310 GHz at 1550 nm has been demonstrated with Ge on Si APD PDs [5, 261, 262]. Temperature insensitive with low dark current 25 Gb/s normal incident Ge/Si APD was also proposed recently [263]. High speed and better sensitivity of APD PDs pave the way for future upgrades and has been successfully used for various applications such as 3D imaging and single photon detection [264, 265]. A summary of reported Ge-based Si PDs is provided in Table 2-3 as an overview of different approaches.

<table>
<thead>
<tr>
<th>Year</th>
<th>Ref.</th>
<th>Structure</th>
<th>Responsivity (A/W) @1550 nm</th>
<th>3 dB bandwidth (GHz)</th>
<th>Dark current density (A/cm²)</th>
<th>Dark current (μA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2005</td>
<td>[256]</td>
<td>Schottky</td>
<td>0.73</td>
<td>13@-3V</td>
<td>-</td>
<td>0.38@-5V</td>
</tr>
<tr>
<td>2007</td>
<td>[253]</td>
<td>PIN</td>
<td>1.08</td>
<td>7.2@-3V</td>
<td>-</td>
<td>0.9@-1V</td>
</tr>
<tr>
<td>2007</td>
<td>[257]</td>
<td>PIN</td>
<td>1.16@-2V</td>
<td>29.4@-2V</td>
<td>-</td>
<td>0.26@-2V</td>
</tr>
<tr>
<td>2008</td>
<td>[249]</td>
<td>MSM</td>
<td>0.4</td>
<td>40</td>
<td>-</td>
<td>0.1</td>
</tr>
<tr>
<td>2009</td>
<td>[250]</td>
<td>PIN</td>
<td>0.4</td>
<td>-</td>
<td>4.1x10⁻⁴@-5V</td>
<td>-</td>
</tr>
<tr>
<td>2009</td>
<td>[21]</td>
<td>PIN</td>
<td>1@-4V</td>
<td>42@-4V</td>
<td>6x10⁻⁴ @-4V</td>
<td>.018@-1V</td>
</tr>
<tr>
<td>2009</td>
<td>[259]</td>
<td>PIN</td>
<td>0.05@-2V</td>
<td>49@-2V</td>
<td>6x10⁻⁵ @-2V</td>
<td>0.3@-2V</td>
</tr>
<tr>
<td>2010</td>
<td>[266]</td>
<td>Vertical PIN</td>
<td><a href="mailto:0.7@-0.5V">0.7@-0.5V</a></td>
<td><a href="mailto:12@-2.5V">12@-2.5V</a></td>
<td><a href="mailto:.125@-0.5V">.125@-0.5V</a></td>
<td><a href="mailto:0.2@-0.5V">0.2@-0.5V</a></td>
</tr>
<tr>
<td>2011</td>
<td>[258]</td>
<td>PIN</td>
<td>-</td>
<td>30@-7V</td>
<td>-</td>
<td>0.231@-1V</td>
</tr>
<tr>
<td>2012</td>
<td>[260]</td>
<td>PIN</td>
<td>0.78@0V</td>
<td>120@-2V</td>
<td>80@-1V</td>
<td>4@-1V</td>
</tr>
<tr>
<td>2014</td>
<td>[267]</td>
<td>GeSn PIN</td>
<td>0.27@0V</td>
<td>-</td>
<td>6.75@-1V</td>
<td>-</td>
</tr>
<tr>
<td>2015</td>
<td>[251]</td>
<td>GeSn PIN</td>
<td>0.178</td>
<td>-</td>
<td>0.073 @-1V</td>
<td>-</td>
</tr>
<tr>
<td>2010</td>
<td>[268]</td>
<td>APD</td>
<td>16.8@-23V</td>
<td>5@-23V</td>
<td>-</td>
<td>100@-23V</td>
</tr>
<tr>
<td>2012</td>
<td>[262]</td>
<td>APD</td>
<td>12@-28V</td>
<td>8@-28V</td>
<td>-</td>
<td><a href="mailto:100@-29.4V">100@-29.4V</a></td>
</tr>
<tr>
<td>2014</td>
<td>[263]</td>
<td>APD</td>
<td>4.4@-18V</td>
<td>18@-18V</td>
<td>-</td>
<td>700@-18V</td>
</tr>
<tr>
<td>2013</td>
<td>[269]</td>
<td>UTC</td>
<td>0.5@-3V</td>
<td>30@-3V</td>
<td>-</td>
<td>0.68@-3V</td>
</tr>
<tr>
<td>2014</td>
<td>[270]</td>
<td>UTC</td>
<td>0.5@-1V</td>
<td>40@-1V</td>
<td>-</td>
<td>.036@-1V</td>
</tr>
</tbody>
</table>

2.5.3.4 Uni-travelling carrier detectors

In Si/Ge p-i-n PDs photon absorption takes place in the depletion region where both electron and hole affect transit times, and thus limit the achievable bandwidth. However this is solved with a novel concept of transporting only a single carrier in a uni-travelling carrier (UTC) PDs. Here, photon generation takes place in a p-doped layer and only the electron acts as the active carrier in the depletion region. Due to the higher velocity of electrons compared to holes, a
lower transit time and minimized space charge effect can be achieved. Decoupling the absorbing layer from the collection layer optimizes transit times and reveals high speed PDs.

![Schematic of a typical UTC PD from [271]. P-InGaAs acts as the absorption layer whereas i-InP is the collection layer.](image)

UTC PDs utilizing InGaAs/InP III-V materials were first demonstrated in [272, 273] to achieve high speed and output power. Si/Ge UTC PDs are also demonstrated [269, 270], although their performance is inferior compared to InP-based PDs due to lack of velocity overshoot of electrons and incapability to engineer complex bandgap of Si/Ge structure. At the same time heterogeneous integration has been evolved as a favourable technology to realize photonic ICs on Si. Recent demonstrations of InP-based UTC PDs show high power performance with increased bandwidth of operation [271, 274]. A typical UTC PD structure is shown in Fig. 2.9 [271], where the p-doped InGaAs layer acts as the absorption layer and the i-InP depletion region acts as the collection layer and controls the output power, RC and transit time limit.

### 2.6 CMOS integration and packaging

Significant progress has been made to mitigate fabrication challenges in the last few decades to realize photonic waveguides on SOI. Effective and low cost light sources and modulators, efficient coupling between macro or nano waveguides with fiber, miniaturization of photonic integrated circuits, low stress, versatility, and scalability to mass production have been some areas of continuous research and progress. Along with diverse waveguide structures, different materials are grown on Si to realize Si-based device: for example, SiO₂, SiON, polymers, Ge, Si₃N₄ and Group III-V semiconductor materials [8-10]. SOI has emerged as a potential platform to realize monolithic integration of PICs which takes advantage of well-established commercial wafers made of a Si layer on top of buried oxide (BOX).
The fabrication process in simple form consists of three steps, shown in Fig. 2.10. First, the materials are deposited on a handling wafer. There are various deposition techniques such as thermal oxidation, sputtering, molecular beam epitaxy (MBE), chemical vapour deposition (CVD), flame hydrolysis deposition, spin-coating and a sol-gel technique. These are used to grow layered waveguide structures on SOI depending on materials, configurations, and applications. After film deposition, the pattern is defined mostly using photolithography, deep-UV lithography, E-beam or Nano Imprint Lithography (NIL) [275]. In pattern transfer (the third step) various etching techniques are applied. These steps are not always fixed and may require alterations depending on the process and design requirements. For example, after pattern defining, film deposition may again be required, such as metal sputtering in the lift-off process. If no hard mask is used, as in Focused Ion Beam (FIB) etching, the process can follow pattern transfer directly after film deposition. Again repetition of the steps is required in complicated structures.

Fig. 2.10: Schematic of fabrication processes from [275].

Fabrication processes need to be chosen and handled carefully to confirm minimized optical losses. Surface roughness should be low enough and materials must exhibit negligible impurities to prevent absorption of light in the wavelength of interest. The thickness of deposited layers must be controlled accurately as small deviations may result in strong effects in desired output properties, especially in phase-sensitive components. Furthermore, the deposited film should exhibit low stress with sufficient growth rate, the process should be low cost, handy and accessible to mass production. The simplest planar or slab structure can be modified to other structures utilizing photolithography and etching techniques. In photolithography, the patterned resist layer is grown to protect the portion of waveguide before etching. Etching can be performed by dry or wet etching techniques which use gaseous and liquid etchants respectively.

The ultimate goal of optoelectronic integration is to allow all individual components on a single substrate for on-chip incorporation. This has to be achieved by mainly focusing CMOS compatibility for market adoption and commercial success. For optoelectronic integrated circuit
development, suitable bonding of Si wafers is a critical step where bonding strength, electrical conductivity, high transparency and low thermochemical stress are expected. Some bonding techniques such as fusion bonding [276] or thermos-compression bonding [277] cannot achieve all these properties at the same time. Again, several optoelectronic schemes operate at lower temperatures than are required for such bonding and may introduce an alignment error. So low temperature bonding is important. A wafer bonding technique with advanced surface activation was recently demonstrated achieving low temperature nano scale integration, with high transparency and low electrical loss [278].

Some developments in recent years have shown advances towards successful integration by achieving several elementary optical functions into nano-photonic Si-based circuits [279-283]. Of the photonic components, laser is the most challenging and is yet to perfectly develop for successful integration. For successful EPIC implementation, the integrated laser needs to be efficient in emission at the designed wavelength, compatible with CMOS processing, and electrically pumped. However, there have been several approaches towards these goals, including integrated hybrid III-V compound laser on Si, Si/SiGe nanocrystal and Er doped Si rich oxide. These were discussed in Section 2.5.1. In recent years, wafer scale integration of III-V epitaxial materials for lasing on Si by using the transfer printing method has been demonstrated [284, 285]. In order to achieve monolithic integration, several methods have been reported including photonic layers at the last levels of metallization with back-end fabrication, combined frontend fabrication and backside fabrication [286]. Recently, a nanowire single mode laser was monolithically integrated achieving low threshold lasing in vertical cavity GaAs-AlGaAs core on Si performing at low temperature [287]. Examples of femtosecond laser pulses required for the TS-ADC application are also available in literature [288-292].

Packaging CMOS photonic devices is a key point and needs to be considered while designing for a small footprint, dense integration, good thermal resistance, low power dissipation and so on. While targeting mass production, costs should be minimized to get closer to the microelectronics industry model which is nearly 20% of the overall cost [293]. Popular microelectronics packaging techniques adopted for optoelectronic integration include the g-Pack ceramic pin grid array [294] and quad flat no leads air cavity package [295]. Moreover, optical coupling architecture and assembly are also critical to achieve high yield with low cost chip packaging [286, 296].
2.7 Summary

In this chapter, previous research on the state-of-art Si photonics devices with a brief history of its evolution has been comprehensively reviewed and summarized. In-depth backgrounds to the key theory behind the Si photonic integrated circuit applications as well as introduction to design components that are required for photonic TS-ADC to be realised in single Si chip are provided. Depending on the requirement of external biasing, these devices are discussed separately as passive and active waveguides including a brief insight into integration challenges and packaging. Thus, this review of the Si photonic components reveals the necessity of the following research investigations that we conduct in this thesis:

- Using the TS-ADC as a target application, design trade-offs involved in the design of suitable passive waveguides with and without bends to meet required dispersion profiles need to be thoroughly investigated. This is addressed in chapter 3.
- Investigations of various distinctive guiding parameters of active Si waveguides with and without bends to reveal their highly dispersive nature to fit in TS-ADC and different other applications. This is addressed in chapter 4.
- Investigation of geometric dependence of various PD properties and optimization of its performance. This is addressed in chapter 5.
- Proposal of optimal mechanism to offer a compact coupler design with low loss, high coupling efficiency as well as large operational bandwidth. This is addressed in chapter 6.
- Proposal of compact design solutions of a polarization rotator with high conversion efficiency, low loss and very high operational bandwidth. This is addressed in chapter 7.

These findings will be utilized in the contributory chapters to investigate an optimal solution and thereby approaching towards fulfilling monolithic integration of CMOS-compatible optoelectronic devices suitable for high speed TS-ADC application in a bigger picture.
Chapter 3
Tailoring Photonic Properties of Different Passive
Silicon Waveguides

In this chapter, using the photonic TS-ADC as a target application, design trade-offs involved in the design of suitable passive waveguides to meet required dispersion profiles are thoroughly investigated. Results of a systematic evaluation of the most popular forms of passive Si wire, rib and photonic crystal waveguides with and without bends are presented and analysed. Through numerical simulation, Si photonic waveguide designs are compared in meeting target application requirements in terms of their group velocity dispersion and mode loss across 1.2 to 1.6 µm wavelength ranges. Optical properties of miniaturized devices are highly dependent on waveguide geometry and can be altered for small changes which may crucially affect specific applications. Interdependency of different optical characteristics such as effective RI, mode loss, dispersion and bend loss with changes in waveguide dimensions are also investigated. Other than TS-ADC, these investigations are essential in numerous applications including dispersion compensation, pulse compression, supercontinuum generation, dispersion manipulation, zero dispersion transmission.

3.1 On chip photonic TS-ADC
The stretch process in the TS-ADC approach consists of two steps. In step 1, time-to-wavelength mapping is performed by the combination of chirped optical pulse and the electro optic modulator (EOM). A femtosecond pulse is dispersed in a spool of fiber and transforms to a chirped optical waveform. The high speed RF signal is then intensity modulated onto the chirped waveform in an EOM which leads to time-to-wavelength correspondence. In step 2, the modulated output is further dispersed in a second spool of fiber which stretches the envelope in time and leads to wavelength-to-time mapping. The stretched optical pulse then illuminates a photodiode and is directed to a low speed electronic ADC. The stretch factor can be written as, \( M = 1 + L_2/L_1 \), where \( L_1 \) and \( L_2 \) are the lengths of first and second dispersive fibers respectively [14].
Fig. 3.1: Time stretching of high speed signal: (a) chirped and stretched 100fs pump pulse after passing through a 500m fiber link; (b): 100 GHz, 50 ps time limited signal; (c): Input RF is modulated with chirped pump pulse; (d): stretched output with a stretch factor of 21; (e): stretching with different stretch factors by varying fiber lengths.
Here, we validate the TS-ADC technique with simulations using VPI platform for time limited input RF signals. Fig. 3.1(a)-(e) shows the simulation results with 100 GHz RF signal which is converted down to 5 GHz. Fig. 3.1(a) shows the chirped 100fs pump pulse after stretching through 500m of fiber. Fig. 3.1(b) shows the 100 GHz 50ps time limited input RF signal which will be modulated with the chirped pulse. Fig. 3.1(c) shows the modulated output. This is further dispersed through 10km of fiber and then directed to the PD. Fig. 3.1(d) shows the stretched RF signal which now can be digitized with low speed ADCs. Fig. 3.1(e) shows the stretching of the same signal with different stretch factors which is achieved by changing the lengths of the fibers.

As mentioned in earlier chapters, the long fiber required for dispersing and stretching the optical signals is unrealistic for single chip integration and we propose to replace it with Si waveguides. This technique can be extended for continuous signals, introducing passive optical filters and wavelength division multiplexing. Design of the TS-ADC to be implemented is depicted in Fig.
3.2(a)-(b) for both time-limited and a continuous RF signals. Now, the design trade-offs involved in the design of suitable waveguides meeting required dispersion profiles need to be thoroughly investigated.

In this chapter, the widely-discussed passive wire, rib, and 1D PhC Si waveguides are considered with and without bends to systematically evaluate their performances of GVD and mode loss across the 1.2 to 1.6 μm telecommunication bands. The interdependent phenomena of different optical properties are numerically evaluated by manipulating the waveguide dimensions, including corresponding limits which will be instrumental in selecting the correct type and geometry of waveguides for TS-ADC as well as different other applications.

### 3.2 Formulation

The effective index (neff), which is the ratio of phase delays in a waveguide per unit length with respect to that in vacuum is expected to increase with higher cross-sectional areas and decrease with longer wavelengths within same cross-sectional area. This is expressed as:

\[ n_{\text{eff}} = \frac{c\beta}{\omega} \]  \hspace{1cm} (3.1)

where, \( \beta \) is the propagation constant, \( \omega \) is the angular frequency and \( c \) is the speed of light.

Mode loss (ML) is calculated from the imaginary part of the effective refractive index \( (n_i) \) as shown below.

\[ E(z) = E_0 e^{-i n k_0 z} \text{ and Power } \approx E^2, \]

\[ \text{Loss} \left( \frac{dB}{m} \right) = 10 \log_{10} \left( \frac{P(z = 1)}{P(z = 0)} \right) \]

\[ = 10 \log_{10} \left( \frac{e^{-2i n k_0}}{1} \right) \]

\[ = \frac{10 n_i \pi}{\lambda_0 \ln 10} \]  \hspace{1cm} (3.2)

GI, which plays a significant role in distorting pulse, is defined as \( c/v_g \), where \( v_g \) is the group velocity. GVD, which is a combination of material and waveguide dispersion, is defined as the rate of change of the group delay with respect to wavelengths. This can be formulated as:

\[ D = -\frac{\lambda}{c} \frac{d^2 n}{d \lambda^2} = \frac{1}{c} \frac{dn_g}{d\lambda} = \frac{d(\frac{1}{v_g})}{d\lambda} \]  \hspace{1cm} (3.3)
In straight waveguide, modes are solved in the form expressed as below:

\[ E(x, y, z) = f(x, y) \exp(i\beta z) \]
\[ \beta = n_{\text{eff}} k_0 \]
\[ = n_{\text{eff}} \left(\frac{2\pi}{\lambda_0}\right) \]

Solutions of Maxwell’s equations are performed in the Cartesian coordinate system with proper boundary conditions. However in the case of bend waveguides, the effects of ‘narrow bends’ are characterized by solving the modes of the form expressed as:

\[ E(\rho, y', \theta) = f(\rho, y') \exp(i\beta \rho_0 \theta) \]
\[ \beta = n_{\text{eff}} k_0 \]
\[ = n_{\text{eff}} \left(\frac{2\pi}{\lambda_0}\right) \]

where, \((\rho, y', \theta)\) represents a cylindrical coordinate system as shown in Fig. 3.3 from [297]. Radiative losses due to bends are measured by perfectly matched layer (PML) boundaries that absorb any radiation from the waveguide [298, 299].

Fig. 3.3: Visualization of the cylindrical coordinate system from different angles. Different cross-sections in white with a purple arrow indicate the direction of propagation. From [297].
Bend orientation angle, \( \varphi \) determines the direction in which the waveguide bends. In Fig. 3.3, cross section of the Finite Difference Eigenmode (FDE) simulation region is shown in white with a purple arrow indicating the direction of propagation of the mode. When \( \theta = 0 \), FDE simulation region is the cross section of the waveguide and electromagnetic fields return in the Cartesian reference frame (x, y, z=0) [297]:

\[
\vec{E}(\rho, y', \theta) = \vec{E}(x, y, z = 0) = \begin{pmatrix} E_x(x, y) \\ E_y(x, y) \\ E_z(x, y) \end{pmatrix}
\]

\[
\rho - \rho_0 = x\cos(\varphi) + y\sin(\varphi)
\]

\[
y' = -x\sin(\varphi) + y\cos(\varphi)
\]

3.6

Bend orientation angle, \( \varphi \) is set to 0 (zero) degrees in all the bend calculations. This means that the bend under investigation is in the xz plane around an axis parallel to y, where z is the propagation direction and the cross-section of the waveguide is in the xy plane. Bending with the waveguide cross-section in the xy plane and different orientation angles of 0 and 90 degrees are further illustrated in Fig. 3.4 (a)-(b). However if xz is the waveguide cross-section plane and propagation is in y direction, then the bend is in the xy plane parallel to z.

Fig. 3.4: Bend of the confined mode with cross section of the waveguide in xy plane [297]: (a): waveguide bend in xz plane with bend orientation of 0 degrees; and (b): waveguide bend in yz plane with bend orientation of 90 degrees.

### 3.3 Modelling and Characterization

The Si waveguides under investigation consist of a Si core with a refractive index (RI) of 3.5 and SiO\(_2\) cladding with a RI of 1.44. PML boundaries were used with sufficient layers to absorb outgoing waves from the interior of the computational region and also to tightly restrict any reflection from the boundaries. If the boundaries are not far enough away from where the fields are expected to be confined, then PML will contribute to the loss. Simulation size with
sufficient distance from confined fields are maintained by checking and plotting E-field intensity in log scale near the boundaries as shown in Fig. 3.5. A fine mesh consisting of 300*300 number of mesh cells (which corresponds to mesh size of around 5 nm) with minimum mesh step of $10^{-6}$ µm is utilized to characterize the waveguides. Operating wavelengths of 1.2 µm to 1.6 µm were chosen to cover the both short-haul and long-haul telecommunication bands. Different scenarios of the geometry which include variations in core width and height are considered to measure the optical parameters including effective RI, GI, GVD and ML for Transverse Electric (TE) modes. Modeling and characterization of wire, Rib, and 1D PhC waveguides are analyzed and discussed below in separate sections.

![Fig. 3.5: E-field intensity of the confined mode in log scale for Si wire: (a) with simulation size of 1.5µm*2.6µm; (b) with simulation size of 3.6µm*5.2µm.](image)

### 3.3.1 Si wire

The initial Si wire structure consists of a Si core of 300 nm height and 1 micron (µm) width with bottom SiO$_2$ cladding of 1 µm, as shown in Fig. 3.6. Performance is analyzed in three stages. In the first stage, the core width is kept fixed, while core height is varied from 300 nm to 100 nm. In the second stage, the core height is kept fixed and the core width is varied from 1 µm to 350 nm. In the third stage, cladding height is varied and the core dimension is fixed.

Fig. 3.7(a)-(d) shows respectively the changes in effective RI, GI, GVD and ML of the waveguide for fixed core width of 1 µm, but varied core heights of 100, 200 and 300 nm. It shows that effective RI, GI and GVD of the waveguide changes significantly with respect to core heights. In Fig. 3.7(a), effective RI increases significantly with the increase of core heights. When core height increases, light is confined in more Si which has higher refractive index. As a result, effective RI increases. GI also tends to increase with increasing core heights that alter GVD from normal to anomalous due to the stronger effect of waveguide dispersion over
material dispersion. Shown in Fig. 3.7(c), GVD of the Si wire can be tuned from -1296 ps/(nm.km) to +596 ps/(nm.km) by changing the core height from 100 to 300 nm only. Dependence of RI, GI, and GVD on operating wavelengths is also clearly visible as expected, although it is not so significant within the current operating wavelength range.

Fig. 3.6: (a): Dimensions of the Si wire, and (b): E-field intensity of the confined mode.

Fig. 3.7: Changes of optical parameters of a Si wire waveguide with respect to different core heights, but fixed core width: (a): effective RI vs. wavelength, (b): group index vs. wavelength, (c): group-velocity dispersion vs. wavelength, and (d): mode loss vs. wavelength.
Fig. 3.8: Sharp change in loss near cut-off wavelength for different core heights, but with fixed width.

Shown in Fig. 3.7(d), ML also increases with the increase of core heights. However, the sudden change in loss with 100 nm is related with effective mode area, which increases sharply near cut-off wavelengths and adversely affects the propagation of light through the waveguide core. As the cut-off wavelengths for waveguides with different core heights are different, the expected abrupt changes in ML are also spaced apart. For the Si wire under consideration, with a core height of 100 nm, the abrupt change in ML happened at around 1.5 µm, which can be expected to happen at longer wavelengths for core heights of 200 and 300 nm. For better clarity and visualization, the simulation was run for a wider wavelength band of 1.2 µm to 2.6 µm and a new set of curves was collected as shown in Fig. 3.8: this encapsulates the abrupt changes in ML for all three core heights.

Fig. 3.9(a)-(d) shows the changes in characteristic parameters at core widths of 350, 450, 700 and 1000 nm with the core height fixed at 300 nm. Similar to Fig. 3.7(a)-(d), effective RI, GI and GVD of the waveguide change significantly with respect to core widths. At larger widths, effective RI increases as expected, but GI tends to decrease due to increasing group velocity or decreasing group delay. GVD decreases from a higher anomalous to a lower anomalous dispersion, which can be expected to change the polarity at higher values of core widths. For the current values of core widths, GVD changes from +9812 ps/(nm.km) to +596 ps/(nm.km) at 1.6 µm wavelength. Inter-dependence among RI, GI, GVD and operating wavelengths is also clearly visible, similar to the changes in core height. ML is also found to be dependent on core widths and wavelengths, which changes inversely with the change of core widths.
Fig. 3.9: Changes of optical parameters of a Si wire waveguide with respect to different core widths, but fixed core height: (a): effective RI vs. wavelength; (b): group index vs. wavelength; (c): dispersion vs. wavelength, and (d): mode loss vs. wavelength.

Fig. 3.10: Changes of optical parameters of a Si wire with respect to different cladding height, but fixed core dimension: (a): effective RI vs. wavelength; (b): group index vs. wavelength; (c): dispersion vs. wavelength, and (d): mode loss vs. wavelength.
So far, the cladding height was remained fixed at 1 µm each. Dependence of the characteristics properties on cladding is now investigated where its height is varied from 500 nm to 1500 nm whilst core height and width are kept fixed at 300 nm and 1µm respectively. Fig. 3.10(a)-(d) shows the changes in characteristic parameters at cladding heights of 500, 1000, and 1500 nm. As in Fig. 3.10(a), at the lower cladding height, effective RI increases. This can be attributed to the fact that when the bottom cladding is too thin, there is a considerable leak in the mode to the Si substrate which has high RI resulting in increasing mode RI. GI tends to increase with decreasing cladding height due to decreasing group velocity. With a higher cladding height, GVD decreases from a higher anomalous to a lower anomalous dispersion, as shown in Fig. 3.10(c). For the current values of cladding heights, GVD changes from +653 ps/(nm.km) to +577 ps/(nm.km) at 1.2 µm operating wavelength. As the light is mainly confined in the core, changes in RI, GI, and GVD are not significant compared to dimensional changes in the core.

However, ML changes significantly at a lower cladding height. Due to insufficient separation of the core from the Si substrate, part of the confined mode enters the substrate and results in greater loss. The inadequacy of cladding spreads the mode over the Si substrate and needs to be avoided to enable a smaller ML. This is further illustrated in Fig. 3.11(a)-(c) by plotting E-field intensity of the confined mode in log scale with respect to different cladding heights of 500 nm, 1000 nm, and 1500 nm.

In order to characterize the effects of bending on GVD and ML, the waveguide is incorporated with a narrow bending of radii 3 to 10 microns, and the respective plots are shown in Fig. 3.12(a)-(b). In both cases, the fixed dimensions for the core height and width were chosen as 100 nm and 1000 nm respectively. It shows that bending significantly influences the GVD and
ML characteristics. GVD tends to increase with sharp bending and ML maintains an inversely proportional relationship with the bending radii, as expected. Fig. 3.13 shows the E-field intensity of the corresponding confined mode with a bending radius of 3 µm at 1.2 µm operating wavelength. It shows the bending of the mode is in xz plane parallel to y.

![Graph showing influence of bending on Si wire characteristics](image1.png)

**Fig. 3.12**: Influence of bending on the characteristics of Si wire: (a): group-velocity dispersion, and (b): mode loss.

![Graph showing E-field intensity with micro bends](image2.png)

**Fig. 3.13**: E-field intensity of the confined mode with micro bends: (a): in linear scale; (b): in log scale.
3.3.2 Rib Waveguide

![Diagram of rib waveguide](image)

Fig. 3.14: (a) Dimensions of the rib Si waveguide, and (b): E-field intensity of the confined mode.

The primary Si rib waveguide structure consists of core height of 400 nm, core width of 1 µm and a Si strip with a width of 400 nm which is etched to a depth of 200 nm, as shown in Fig. 3.14(a). As with the Si wire, performance is analyzed in three stages. In the first stage, the core width is kept fixed, while core height is varied from 600 nm to 200 nm. In the second stage the core height is kept fixed, while the core width is varied from 1 µm to 500 nm, and in the third stage the core dimension is kept fixed but, cladding height is varied from 500 nm to 1500 nm. With the core heights of 600, 400, and 200 nm, the etching depth of the top Si strip varies as 300, 200, and 100 nm respectively.

Fig. 3.15(a)-(d) shows the respective changes in effective RI, GI, GVD and ML of the waveguide for a fixed core width of 1 µm, but varied core heights of 100, 200 and 300 nm. It shows that effective RI, GI and GVD change significantly with respect to core heights. Similar to the Si wire, effective RI and GI increase with increased core heights that alter GVD from normal to anomalous. As shown in Fig. 3.15(c), the GVD of the rib waveguide can be tuned from -755 ps/(nm.km) to +772 ps/(nm.km) by changing the core height from 100 to 300 nm only. Interdependence among RI, GI, GVD and operating wavelengths is also clearly visible although it is not so significant within the operating 400 nm band. ML is also seen to be dependent on core height and wavelengths which varies directly with the changes of the core heights.
Fig. 3.15: Changes of optical parameters of a rib waveguide with respect to different core heights, but fixed core width: (a): effective RI vs. wavelength; (b): group index vs. wavelength; (c): dispersion vs. wavelength, and (d): mode loss vs. wavelength.

Fig. 3.16(a)-(d) shows the changes in characteristic parameters at core widths of 500, 700 and 1000 nm with the core height fixed at 200 nm. Similar to Fig. 3.15(a)-(d), the effective RI, GI and GVD of the waveguide change significantly with respect to core widths. At larger widths, effective RI increases as expected, but GI tends to decrease, as in the case of Si wires. As a result, GVD decreases from a higher anomalous to a lower anomalous dispersion, which can potentially change the polarity at higher values of core widths. For the current values of core widths, GVD changes from +4091 ps/(nm.km) to +560 ps/(nm.km) at 1.6 μm operating wavelength. Inter-dependence among RI, GI, GVD and operating wavelengths is also clearly visible as similar to the changes in core height. ML is also found to be dependent on core widths and wavelengths, which changes inversely with the change of core widths, similar to the Si wire.
Fig. 3.16: Changes of optical parameters of a rib waveguide with respect to different core widths, but fixed core height: (a): effective RI vs. wavelength; (b): group index vs. wavelength; (c): dispersion vs. wavelength, and (d): mode loss vs. wavelength.

Fig. 3.17: Changes of optical parameters of a rib waveguide with respect to different cladding height, but fixed core dimension: (a): effective RI vs. wavelength; (b): group index vs. wavelength; (c): dispersion vs. wavelength, and (d): mode loss vs. wavelength.
So far, the cladding height was fixed at 1 µm. As with the case of the Si wire, here the dependence of the characteristics properties on cladding is investigated. Keeping the core dimension fixed, the cladding height is varied from 500 nm to 1500 nm and characteristic parameters are plotted in Fig. 3.17(a)-(d) at cladding heights of 500, 1000, and 1500 nm. As in Fig. 3.10(a), at lower cladding heights, effective RI increases due to similar reason explained for Si wire and is shown in Fig. 3.17(a). GI tends to decrease with increasing cladding height, whereas GVD decreases from a higher anomalous to a lower anomalous dispersion according to Fig. 3.17(b)-(c). For the current values of cladding heights, GVD changes from +686 ps/(nm.km) to +654 ps/(nm.km) at 1200 nm operating wavelength.

Fig. 3.18: E-field intensity of the confined mode in log scale with respect to different cladding heights, but fixed core dimension: (a): 500 nm; (b): 1000 nm, and (c): 1500 nm.

Fig. 3.17(d) shows the ML which decreases with more cladding height but increases abruptly at lower height: this is caused by insufficient separation of the core from Si substrate, as explained with respect to the Si wire. For example, with the current dimensions of the waveguide, a decrement in cladding height from 1500 nm to 1000 nm increases ML from 0.995 dB/cm to 1.07 dB/cm at 1.6 µm operating wavelength, whereas it increases sharply to 6.3 dB/cm when the cladding height is decreased to 500 nm. The overlapping of the confined mode with Si substrate is further illustrated in Fig. 3.18(a)-(c) by plotting E-field intensity of the confined mode in log scale with respect to different cladding heights of 500 nm, 1000 nm, and 1500 nm.

In order to characterize the effects of bending on GVD and ML, the waveguide is incorporated with a narrow bending of radii 2 to 5 microns, and the respective plots are shown in Fig. 3.19(a)-(b). In both cases, the fixed dimensions for the core height and width were chosen as 200 nm and 700 nm respectively. It shows that anomalous dispersion tends towards normal dispersion with sharp bends and also increases in loss as expected. Fig. 3.20 shows the E-field intensity of the corresponding confined mode with a bending radius of 2 µm at 1.2 µm operating wavelength. Here, the bending of the mode is in xz plane around an axis parallel to y and z is the direction of propagation.
3.3.3 1D PhC Waveguide

The PhC structure under investigation is composed of periodic etching of Si in y direction leaving 200 nm height and 400 nm width to confine the mode as shown in Fig. 3.21(a). A one micron buried oxide layer is used as the lower cladding. Mode field distribution ($E_x$) within the waveguide is shown in Fig. 3.21(b). Performance is analyzed: firstly, by keeping the core width fixed, but varying the height from 150 to 300 nm; secondly by keeping the core height fixed but varying the width varied 400 nm to 600 nm, and thirdly by keeping the core dimension fixed, while varying the cladding height from 800 nm to 1200 nm.
Fig. 3.21: (a) Dimensions of the 1D PhC waveguide, and (b) E-field intensity of the confined mode.

Fig. 3.22: Changes of optical parameters of a PhC waveguide with respect to different core heights, but fixed core width: (a): effective RI vs. wavelength; (b): group index vs. wavelength; (c): dispersion vs. wavelength, and (d): mode loss vs. wavelength.

Fig. 3.22(a)-(d) shows respectively the changes in effective RI, GI, GVD and ML of the waveguide for a fixed core width of 400 nm, but varied core heights of 150, 200 and 300 nm. It shows that effective RI, GI and GVD of the waveguide change significantly with respect to core heights. In Fig. 3.22(a), effective RI increases significantly with the increase of core heights as expected. GI also tends to increase with the increasing core heights that alter GVD from normal to anomalous due to stronger effect of waveguide dispersion over material dispersion. Shown in Fig. 3.22(c), GVD of the PhC waveguide can be tuned from -12400 ps/(nm.km) to +2770 ps/(nm.km) by changing the core height from 150 to 300 nm only at 1550 nm wavelength. ML
is also seen to be dependent on core height and wavelengths which varies directly with the changes of the core heights.

Fig. 3.23(a)-(d) shows the changes in characteristic parameters at core widths of 400, 500 and 600 nm with core height fixed at 150 nm. At larger widths, effective RI increases as expected, but GI tends to decrease as was the case with Si wire and rib waveguides. GI with 400 nm width decreases sharply compared to the other two cases and also corresponding dispersion parameters. GVD decreases from a higher value towards zero dispersion with higher widths. Interdependence among RI, GI, GVD and operating wavelengths is also clearly visible, similar to the changes in core height. ML is also found to be dependent on core widths and wavelengths, which changes inversely with the changes of core widths, similar to Si wire and rib waveguides.

So far, the cladding height has been fixed at 1 μm but is now varied from 800 nm to 1200 nm and characteristic parameters are plotted in Fig. 3.24(a)-(d) at cladding heights of 800, 1000, and 1200 nm. As with the other cases, at lower cladding heights, effective RI increases and is shown in Fig. 3.24(a). GI tends to decrease with increasing cladding heights, whereas GVD decreases from a higher anomalous to a lower anomalous dispersion and goes towards deep in the normal region according to Fig. 3.24(b)-(c). Fig. 3.24(d) shows the increment in ML, as was
the case with Si wire and rib waveguides. The overlapping of the confined mode with Si substrate is further illustrated in Fig. 3.25(a)-(c) by plotting E-field intensity of the confined mode in log scale with respect to different cladding heights of 800 nm, 1000 nm, and 1200 nm.

![Fig. 3.24: Changes of optical parameters of a PhC waveguide with respect to different cladding height, but fixed core dimension: (a): effective RI vs. wavelength; (b): group index vs. wavelength; (c): dispersion vs. wavelength, and (d): mode loss vs. wavelength.](image)

![Fig. 3.25: E-field intensity of the confined mode in log scale with respect to different cladding heights, but fixed core dimension: (a): 800 nm; (b): 1000 nm, and (c): 1200 nm.](image)

In order to characterize the effects of bending on GVD and ML, the waveguide is incorporated with a narrow bending of radii 3 to 5 microns, and the respective plots are shown in Fig.
3.26(a)-(b). In both cases, the fixed dimensions for the core height and width were chosen as 150 nm and 400 nm respectively. It shows that bending influences the GVD and ML characteristics significantly. GVD tends to increase with sharp bending and ML maintains an inversely proportional relationship with the bending radii, as expected. Fig. 3.27 shows the E-field intensity of the corresponding confined mode with a bending radius of 3 µm at 1.2 µm operating wavelength. It shows the bending of the mode is in xz plane parallel to y.

![Dispersion and Loss Profiles](image1)

**Fig. 3.26:** Characteristics of the PhC waveguide: (a): dispersion profile with and without bending, and (b): loss profile.

![E-field Intensity](image2)

**Fig. 3.27:** E-field intensity of the confined mode with micro bends: (a): in linear scale; (b): in log scale.
3.4 Evaluation of passive waveguides for TS-ADC

To realize the proposed TS-ADC technique for on chip integration, replacement of the long fiber requires highly dispersive Si waveguides. For example, using 100fs pump pulse as the carrier, the target is to stretch 100GHz RF input signal 10 times to finally get a 10GHz signal. To keep the chip size within cm, it will require normal dispersion amount of $3 \times 10^3$ ps/(nm.km) in the first Si waveguide, whereas 10 times more for the second waveguide. If RF signal beyond 100GHz is expected to digitize, more dispersive Si waveguides will be required.

So far, we have evaluated the dispersive nature of commonly used Si wire, rib and 1D PhC waveguides with corresponding ML. Results from Section 3.3.1 suggest that at 1550 nm wavelength the maximum achievable normal dispersion in Si wire is about $2.2 \times 10^3$ ps/(nm.km). Results from Section 3.3.2 suggest that the maximum achievable normal dispersion in Si rib waveguide is about $0.7 \times 10^3$ ps/(nm.km). Relatively higher dispersion can be achieved with PhC structures at the cost of slightly higher ML. Results from Section 3.3.3 show normal dispersion as high as $1.6 \times 10^4$ ps/(nm.km) in waveguide bends at 1550 nm wavelength.

As we see, these passive waveguides are not dispersive enough to replace even the first fiber stage in the TS-ADC design. If we utilize a 50fs pulse source for the chirping, requirement of dispersion in Si waveguide becomes half. However, still the waveguides are not suitable enough to meet required dispersion. Although, 1D PhC waveguides can be cascaded to perform the stretching operation, total number of waveguides required to replace the both fibers will make the design very bulky. This leads to the investigation of tailoring dispersive properties in active Si waveguides. The control of biasing and doping concentrations to attain required changes in the RI and corresponding changes in optical properties in active waveguides will provide greater control to tailor dispersion.

3.5 Summary

Using the photonic TS-ADC as a target application, the performance bounds of passive Si wire, rib, and 1D PhC Si waveguides by manipulating geometry with and without bends are investigated. It shows that the photonic properties can be controlled by tailoring waveguide dimensions and bends. For all types of waveguides, effective RIs increase with an increase of core dimension and decreases with an increase in wavelength of operation. However, RI decreases with increased cladding heights due to having a gradually lesser impact of Si core on the overall waveguide structure. ML also tends to decrease with increasing operating wavelength except that the cut-off wavelength is reached with smaller core dimensions. ML
changes and increases sharply with thinner cladding dimensions due to insufficient separation of the confined mode from the Si substrate. GIs increase only with the increase of core height but decrease with the increase of core widths. For GVD, increased core height tends to move it from normal to anomalous, whereas it behaves oppositely for increased core width. Bending radius also influences the GVD and ML characteristics significantly where anomalous dispersion tends towards normal and loss increases in all cases for sharper bends.

The performance of each waveguide varies significantly with geometry, operating wavelength and bending radius: this requires careful selection depending on the nature of the application. Waveguides with high anomalous dispersion can be utilized for dispersion compensation, pulse compression or soliton propagation. Zero dispersion, which is required for optical interconnects or data transmission, can be achieved by selecting suitable core height and width for each waveguide. A rib waveguide has the benefit of larger spot size and lower propagation loss compared to other structures. PhC waveguides have the potential to introduce very high normal dispersion, and can be suitable for applications like supercontinuum generations or chirped femtosecond pulses at the cost of a slightly higher loss. However, none of the waveguides are dispersive enough to be used in the proposed TS-ADC design in Fig. 3.2. While cascade of waveguides explored in this section could potentially be used to achieve the dispersion levels required, this option will require significantly larger photonic integrated circuits making it practically infeasible from the cost as well as the loss perspectives. This leads us to investigate active Si waveguides, where with geometry, the control of biasing and doping concentrations will provide greater control to tailor dispersion.
Chapter 4
Geometry and Depleting Carrier Dependence of Active Si Waveguide

In chapter 3, design trade-offs involved in the design of suitable passive waveguides to meet required dispersion profiles for TS-ADC application were systematically evaluated. Our research showed that amount of dispersion needed to achieve the time to wavelength mapping in such applications could not be easily met through passive waveguide geometries investigated. In this chapter, we extend our investigation into active Si waveguides. Here, Changes in RI through plasma dispersion effect give greater control to tailor various guiding properties. So, this chapter brings Si PIN structure with planar and 1D PhC to characterize guiding parameters with changes in waveguide dimension, doping concentration and applied biasing. Dispersion is considerably enhanced in these waveguides compared to passive waveguides. Investigation of interdependency of various distinctive properties including perturbation in real RI, mode loss, group velocity dispersion, and bending loss in depletion mode operation are performed. Other than TS-ADC, these are essential in numerous applications including electro-optic modulation, optical switching, filtering and slowing light.

4.1 Introduction

One of the key enablers of the powered active Si waveguide devices is the distinct concentrations of carriers in the Si waveguide that can be achieved either by carrier accumulation, injection or a depletion process which causes perturbation in optical absorption and effective RIs. In carrier accumulation, applied voltage-induced charges build up near gate dielectric of the capacitor. This accumulation of charges modifies the RI of the waveguide and eventually the phase of light passing through it. As the MOS capacitor is operated in accumulation bias, carrier recombination in Si does not limit device bandwidth. In carrier injection, free carriers are injected into the intrinsic part of the diode which recombines when the bias voltage changes to zero and limits the operational speed. So the time response of injection operation is limited by the minority carrier’s lifetime (ns to µs) due to carrier recombination in the intrinsic region. It also suffers from thermal heating induced by a large forward current. In a carrier depletion operation, a reverse-biased diode increases the electric field in the intrinsic regions which sweeps the carriers out and widens the space charge region.
This in turn alters the RI profile and is more advantageous than carrier injection. Depletion operation under reverse bias is expected to have much faster response times (ps) due to carrier sweep out and also a smaller heating effect for low power dissipation.

Of various active waveguide applications, Si-based electro-optic modulators have been extensively researched. Carrier concentration variation obtained by depletion operation intrinsically provides high speed and is attained in reverse-biased PN or PIN diodes for modulation operations. Several approaches of the depletion-based lateral and vertical diode Mach-Zehnder interferometer (MZI) modulator have reportedly achieved 3 dB bandwidth up to 30 GHz [208, 209, 300]. Designs of a PN diode along a ring resonator to tune the effective index for modulation applications are demonstrated in [301, 302]. Other than optical modulation, the active Si waveguide has also been widely researched to achieve optical switching. Electro-optic (EO) switches based on MZIs benefit from low wavelength as well as temperature dependencies, but require high operation voltage and large dimensions. These have been minimized by utilizing rib or slot waveguide structures [303, 304]. Control and tuning delays to achieve slow light have been researched by utilizing the free carrier plasma dispersion and thermo-optic effects produced by forward-biased pin diode incorporating a PhC waveguide is discussed in [305]. However, as thermos-optic is a slow effect and PhC waveguide-based slowing light suffers from high loss, electronically tunable delay lines combining anodized grating and free-carrier plasma effect is presented in [306]. Another application of the active Si waveguide is electro-optical filtering where the resonant wavelength can be adjusted by applying voltage, which leads to changes in optical properties and shifts output wavelength of the electro-optical filter [307, 308].

The unique impacts on optical modes due to changes in carrier concentrations are explained in [309]. An earlier work showed the effect of heavy doping (up to 3*10\(^{21}\) /cm\(^3\)), for both n and p types, on the critical points of Si including optical properties and band structure [310]. The effect of n and p doping positions to manipulate the density of free carriers in Si waveguide are presented with three different structures in [311]. Similar work analysing the effects of free carrier injection but for a micro-ring resonator is assessed by changing the position of doping regions in [312]. A comprehensive study on design considerations and propagation characteristics of a channel PhC surface plasmon waveguide (PCSPW) with different active metals, such as Au, Ag and Al, is discussed in [313]. The measurement of effective carrier lifetime in a lateral pin diode by different experimental techniques such as static, reverse recovery and transient optical absorption is presented in [314]. Free carrier absorption loss in a pin Si waveguide for various doping concentrations and broadband variable chromatic dispersion in a photonic-band electro-optic waveguide are discussed separately in [315] and [316].
The perturbations in absorption and RI eventually dictate the characteristics of any active waveguide including mode loss (ML), and group velocity dispersion (GVD), for which a careful selection and control of the distinctive parameters involving the changes of the concentrations of carriers are extremely important. Another important aspect of any optical waveguide is the dependence of optical properties on physical dimensions, which can be varied to manipulate most of the characteristic features as desired [69, 71]. However, as the physical dimensions of the waveguide are mostly in the range of 10s to 100s of nm, they are sensitive to small deviations in geometry, for which precise control of manufacturing specifications and tolerances is essential, similar to the changes of the concentrations of carriers, mentioned earlier. Keeping the TS-ADC as target application, here active Si waveguides with planar and 1D PhC are considered for a complete characterization of various distinctive guiding parameters including real RI, change in RI, ML, GVD, and bending loss by incorporating changes in physical dimensions, carrier concentrations, and bias voltages that can be instrumental in developing optimal design specifications for various application centric active Si waveguides.

4.2 Formulation

The change in the RI in Si can be achieved either by applying an electric field or by changing the charge carrier concentration. Electroabsorption, explained by the Franz-Keldysh Effect, is applied to an electric field-induced tunnelling between valence and conduction band state. This alters the linear absorption coefficient \( \alpha \) and is related to the optical extinction coefficient \( k \) according to Equ.4.1 [317].

\[
k = \frac{\alpha \lambda}{4\pi}
\]

where \( \lambda \) is the optical wavelength. Again the relationship between the real part of RI (n) and k is established by the well known Kramers-kronig dispersion relations [318]. Absorption of light in Si by an externally applied electric field is measured experimentally in [319] and is utilized to estimate electro-refraction using Equ.4.2 [204].

\[
\Delta n(V) = 6.3 \times 10^{-6} \text{ cm.V} \int_0^V \Delta \alpha(V') dV' / (V'^2 - V^2)
\]

where, \( \Delta \alpha(V') \) is the change in electro-absorption and \( \Delta n(V) \) is change in the RI resulting from the applied electric field (E). Results show that \( \Delta n \) decreases with increasing wavelength within 1.5 to 1.6 µm, which is approximately \( 2 \times 10^{-6} \) at 1.3 µm wavelength when \( E = 10^5 \ V/cm \) [204]. Another electric field-induced influence known as the Kerr Effect is explained by an
anharmonic oscillator model according to which electro-refraction can be approximated by Equ.4.3 [320].

\[
\Delta n = -3e^2(n^2-1)E^2/2\pi M^2\omega_0^4x^2
\]

where, \(e\) is the electronic charge, \(n\) is an unperturbed RI, \(M\) is the effective mass, \(\omega_0\) is the oscillator resonance frequency, and \(x\) is the average oscillator displacement. Results show that \(\Delta n\) increases with increasing the applied electric field at 1.3 µm wavelength and is about \(10^{-4}\) with \(E = 10^6\) V/cm. However, in both cases the electric field-induced changes in the RI are quite low and are not suitable enough for different applications.

On the other hand, the optical properties of Si are strongly affected by changing charge carrier absorption, whether by carrier accumulation, injection or depletion. Carrier-induced changes in the RI are usually governed by three key mechanisms: bandfilling, bandgap shrinkage and free carrier concentration [321]. Bandfilling has been explained by the Burstein-Moss Effect [322], where electrons from the valence band require more energy than the nominal bandgap to be optically excited due to pre-filled lower energy states of conduction band in n-type semiconductors and cause a decrease in the absorption coefficient. This effect is more pronounced in semiconductors with smaller effective mass and lower energy bandgaps. Bandgap shrinkage is caused when the concentration is large: this lowers the energy in the conduction band and an increment in the valence band due to the overlap and correlation effects [323-325]. Wave functions of the electrons occupied at the bottom of the conduction band overlap, repel one another and form a gas of interacting particles. This results in decreasing the energy of the conduction band edge. Conversely, a similar correlation effect for holes occupied in the valence band increases the energy and the overall effect results in band-gap shrinkage. This effect can be determined by free-carrier density, and is nearly independent of impurity concentration.

However, optical properties are strongly affected and are demonstrated for carrier refraction achieved by variation of free carrier absorption known as the plasma effect [326]. Unperturbed RI and the related changes, due to the change in carrier concentrations, can be calculated by utilizing the well-known Plasma-Drude model [327], as expressed in Equ.4.4.

\[
n + ik = \sqrt{\frac{\epsilon_0 \frac{e^2}{\omega} \frac{n}{m^*_{e} \omega + i\frac{p}{\mu_{e}}} + \frac{p}{m^*_{h} \omega + i\frac{p}{\mu_{h}}}}{\epsilon_0}}
\]  

where \(n\) and \(p\) are the respective densities of free electron and hole carriers, \(\epsilon_0\), \(\epsilon_m\) are the respective permittivities of free space and medium, \(m^*_{e}\) and \(m^*_{h}\) are effective masses of
electrons and holes, $\mu_e$ and $\mu_h$ are the respective mobility of electrons and holes. For large values of $\mu_e$ and $\mu_h$, Equ.4.4 reduces to the following Equ.4.5.

$$n + ik = \sqrt{\frac{\varepsilon m_e e^2 \frac{n^2 + p}{m_e + m_h}}{\varepsilon_0}}$$ 4.5

This can be extended to calculate the changes in RI, $\Delta n$ and absorption coefficients, $\Delta \alpha$, with the assumption that complex RIs can also be calculated from the change of carrier density at any particular wavelength $\lambda$, as expressed in Equ.4.6.

$$\Delta n = -\left(\frac{e^2 \lambda^2}{8\pi^2 c^2 \varepsilon_0 n}\right) \left[\frac{\Delta N_e}{m_e \mu_e} + \frac{\Delta N_h}{m_h \mu_h}\right]$$

$$\Delta \alpha = -\left(\frac{e^2 \lambda^3}{4\pi^2 c^3 \varepsilon_0 n}\right) \left[\frac{\Delta N_e}{m_e \mu_e} + \frac{\Delta N_h}{m_h \mu_h}\right]$$ 4.6

where $e$ is the charge of electron, $n$ is the RI without perturbation, $\varepsilon_0$ is the permittivity of free space, $\mu_e$ and $\mu_h$ are the respective mobility of electrons and holes, $\Delta N_e$ and $\Delta N_h$ are the changes in electron and hole concentrations respectively, and $c$ is the velocity of light. For a Si waveguide, and a light of the 1550 nm band, the wavelengths that are central to most activities of current long-haul telecommunications, Equ.4.6 can be simplified as follows [212] in Equ.4.7 and Equ.4.8.

$$\Delta n = \Delta N_e + \Delta N_h$$

$$\Delta n = -(8.8 \times 10^{-22} (\Delta N_e) + 8.5 \times 10^{-18} (\Delta N_h)^{0.8})$$ 4.7

$$\Delta \alpha = \Delta \alpha_e + \Delta \alpha_h$$

$$\Delta \alpha = 8.5 \times 10^{-18} (\Delta N_e) + 6 \times 10^{-18} (\Delta N_h)$$ 4.8

where $\Delta n_e$ and $\Delta n_h$ are changes in RI, and $\Delta \alpha_e$ and $\Delta \alpha_h$ are changes in absorption resulting from changes in free n and p carrier concentrations respectively. The allowable doping concentration, which largely defines the changes in RI, is bound by the amount of accommodative absorption loss. The amount of loss which will increase sharply with higher carrier concentrations due to elevated free carrier absorption can be calculated from an imaginary part of the effective RI ($n_i$). However, Equ.4.7 indicates that the contribution of the concentration of holes in changing RI is higher than that of the concentration of electrons, which is just the opposite in the case of absorption.
4.3 Modelling and Characterization

To model an active Si waveguide, a 390 nm Si layer is grown on a SiO$_2$ layer with respective width and thickness of 3 µm and 1 µm, as shown in Fig. 4.1(a). The waveguide is chosen to be 500 nm wide. The remaining Si is etched back to 300 nm to leave a waveguide with dimensions 300 nm thick and 500 nm wide that sits on a Si pad of 90 nm. At the edges, metal (Al) contacts with respective widths and thicknesses of 750 nm and 100 nm are grown to enable electrical biasing. The top surface of the waveguide is passivated with a thick layer of oxide.

![Diagram of active Si waveguide](image)

**Fig. 4.1:** (a): Primary geometry of the active Si waveguide under investigation; (b): Layout with specified doping regions.

The PN junction is defined by using analytic profiles of diffusion doping objects which mimics the behaviour of ion implants. These diffusion profiles are 3D objects where doping profiles are defined according to Gaussian or erfc analytic distribution. Dopants are supplied at the “mask-opening surface”, whereas doping concentration goes to a reference concentration at each of the other surfaces. Reference concentration is considered as 1 cm$^{-3}$ which is effectively zero concentration. At a distance of junction width which defines the spacing from the surfaces
where the analytic function is applied, dopant concentration reaches its peak value from any surface except the source. Dopants are applied to the upper z surface with a junction width of 200 nm.

To enable space-charge regions, the inclusion of dopants into Si is modelled by considering a background doping concentration of $1 \times 10^{15} \text{cm}^{-3}$ for a p-type Si epitaxial layer that encompasses the entire geometry. To improve electrical contact between the metal and semiconductor, heavily doped n- and p-wells are used which ensures that the contacts are ohmic. These contact wells are also defined by using the diffusion objects similar to the implants. Source n-well and drain p-well doping concentrations are set at $10^{19} \text{cm}^{-3}$ n and p type respectively, whereas concentrations in n and p waveguides are changed according to the characterization requirements discussed in different sections. Layout with the doping regions specified is shown in Fig. 4.2(b). Finally, to deplete the carriers across the p-n junction, a negative bias of 0 to -4 volt was applied to characterize the distinctive features.

Among different simulation platforms to model the waveguide, this investigation relied on the commercially available Lumerical Solutions: the structure is designed and simulated in a “Lumerical Device” to obtain electrical characteristics and then is run in “Mode Solution” to get the effective RI and mode profiles of various waveguide modes.

A steady state solver mode is selected to perform the dc analysis with 2D y-normal solver geometry. This simultaneously solves Poisson’s equations for the electrostatic potential and drift-diffusion equations for charge where the solutions must be self-consistent. Gummel’s method is used to solve this system of equations which decouples the charge problem from the electrostatic potential problem at each step. First, the electrostatic potential is solved holding the charge fixed. That solution is then used as a fixed input to the charge equations, and those are updated. This process continues until the solution is self-consistent. Convergence control limits the number of iterations of both Poisson and drift-diffusion solvers that may be run. Absolute tolerance of $1 \times 10^{-06}$ volts is considered which determines the maximum absolute change between iterations that can exist for a calculation to be considered as converged. For the Poisson solver, the step converges when:

$$\|V^{k+1} - V^k\|_\infty < \delta$$

where $\delta$ is the tolerance and $V$ is the electrostatic potential. For the drift-diffusion solver, both the electron and hole quasi-Fermi levels must converge:

$$\|E_{Fn}^{k+1} - E_{Fn}^k\|_\infty < \delta$$

$$\|E_{Fp}^{k+1} - E_{Fp}^k\|_\infty < \delta$$

4.10
Fig. 4.2(a) shows the $E_x$ component of TE mode field distribution and Fig. 4.2(b) presents the electric field (E) with unit V/m, where V is the electrostatic potential. Carrier distribution (n-type) as a function of applied bias is shown in Fig. 4.3(a)–(c), where the x-axes denote the width, and z-axes the height of the waveguide and the scale bar presents the number of carriers but in logarithmic scale. It shows, as expected, that the space charge region pushes the free carrier out of the waveguide and becomes wider at higher but negative drain contact voltages.

![Fig. 4.2: Functionality of the waveguide: (a): mode field distribution ($E_x$); (b): electrostatics at -4 volt bias voltage.](image)

![Fig. 4.3: Carrier distribution (n-type) as a function of applied bias (a) at zero bias voltage; (b) at $V=-2v$; (c) at $V=-4v$.](image)

A detailed characterization of various responses of depleting carriers with respect to the changes in bias voltage, doping concentration, physical dimension, and operating wavelength is undertaken as follows. All the simulations are performed for TE polarization, but a response with TM mode is also investigated in a separate section.
4.3.1 Uniform Doping Concentration

Fig. 4.4: Changes of waveguide parameters with respect to the changes in bias voltage and uniform doping concentration: (a): real RI vs. bias voltage; (b): ML vs. bias voltage, and (c): Δn vs. doping concentration.

Fig. 4.4(a)-(c) respectively shows the changes in effective RIs of the fundamental mode, ML, and Δn of the waveguide at the concentrations of electron (n) and hole (p) of 1x10^{17} cm^{-3} to 1x10^{18} cm^{-3} with a reverse bias voltage of 0 to -4 volts. They show that both carrier concentration and bias voltage strongly influence the RI profiles as well as ML, and Δn of the waveguide. With a gradual increase of carrier concentrations from 1x10^{17} cm^{-3} to 1x10^{18} cm^{-3}, the real RI decreases from 2.95468 to 2.95378. Similarly, a gradual increase of reverse bias voltage from 0 to -4 volts increases the real RI. Shown in Fig. 4.4(b), ML has increased from almost nil to 23 dB/cm with the stipulated increase in doping concentrations, which is not, however, so pronounced for the increase of bias voltages. Decreasing loss with increasing bias voltage is attributed to the fact that less number of carriers will be interacting with the propagating mode due to depletion of carriers. The dependency of Δn on doping concentrations is also quite significant although, as for ML, the effects of the change in bias voltage are not that pronounced, as can be seen from Fig. 4.4(c).
4.3.2 Non-uniform Doping Concentration

Fig. 4.5: Changes of waveguide parameters with respect to the changes in bias voltage and non-uniform doping concentration: (a): real RI vs. bias voltage; (b): ML vs. bias voltage, and (c): Δn vs. doping concentration.

To utilize the benefits of higher p concentrations compared to n in terms of a higher change in RI with lower absorption, the waveguide is characterized by varying concentrations of p from 5x10¹⁷ cm⁻³ to 3x10¹⁸ cm⁻³, keeping the concentration of n fixed to 1x10¹⁷ cm⁻³. The corresponding responses are shown in Fig. 4.5(a)-(c). Similar to the characteristics of the waveguide with uniform doping shown in Fig. 4.4(a)-(c), the characteristics with non-uniform doping are almost identical, except that ML is relatively smaller, and Δn is relatively larger, as expected. For example, in Section 4.3.1, with a uniform carrier concentration of 1x10¹⁸ cm⁻³ and bias voltage of -4 volts, the change in real RI is 1.01x10⁻³ with a calculated loss of 20 dB/cm. Whereas for non-uniform doping concentrations of 1x10¹⁷ cm⁻³ and 3x10¹⁸ cm⁻³ for n and p respectively and bias voltage of -4 volts, the change in real RI is 1.66x10⁻³ with a calculated loss of 23.5 dB/cm. These differences can be further explained by the mathematical relationships shown in Equ.4.7 and Equ.4.8.

4.3.3 Influence of pad height H_p

For any active waveguide, physical dimensions also play a significant role in determining responses of the waveguide, along with the applied bias voltage and carrier concentration. Fig. 4.6(a)-(c) shows the influence of different pad heights H_p on real RI, ML, and Δn respectively,
where n and p concentrations of the waveguide are fixed at \(1 \times 10^{17} \text{cm}^{-3}\) and \(3 \times 10^{18} \text{cm}^{-3}\) respectively for Fig. 4.6(a)-(b). For Fig. 4.6(c), the p concentrations are varied from \(5 \times 10^{17} \text{cm}^{-3}\) to \(3 \times 10^{18} \text{cm}^{-3}\) to quantify the effects of changing \(\Delta n\). Keeping \(H_w\) fixed at 300 nm, with an increased pad height \(H_p\) from 50 nm to 120 nm, the real RI increases significantly from 2.95 to 3.03. This can be attributed to the fact that, as the mode is entering to the pad area, this will now also be contributing to RI, and so with increasing \(H_p\), RI is also increasing.

Fig. 4.6: Changes of waveguide parameters with respect to the changes in bias voltage and \(H_p\): (a): real (RI) vs. bias voltage; (b): ML vs. bias voltage, and (c): \(\Delta n\) vs. doping concentration.

Fig. 4.7: Mode Field Distribution for different \(H_p\): (a): \(H_p = 50 \text{ nm}\); (b): \(H_p = 120 \text{ nm}\).
Higher $H_p$ also increases ML, which is caused mostly by the portion of light passing through the pad area. For further clarity, mode profile for $H_p$ 50 nm and 120 nm are shown in Fig. 4.7(a)-(b). Shown in Fig. 4.6(c), the thickness of $H_p$ has hardly any influence on $\Delta n$, although the RI and ML are influenced to a greater extent.

4.3.4 Influence of the gap $W_d$ between a metal contact and waveguide

![Graphs showing changes in waveguide parameters with respect to bias voltage and $W_d$.](image1)

Fig. 4.8: Changes of waveguide parameters with respect to the changes in bias voltage and $W_d$: (a): real (RI) vs. bias voltage; (b): ML vs. bias voltage, and (c): $\Delta n$ vs. doping concentration.

![Graphs showing E-field intensity for different $W_d$.](image2)

Fig. 4.9: E-field intensity (in log scale) of the confined mode for different $W_d$: (a): $W_d=300$ nm; (b): $W_d=700$ nm.
Similar to the pad height \( H_p \), the gap between a metal contact and the waveguide, \( W_d \) has also a great influence on the overall performance of the waveguide. Fig. 4.8(a)-(c) shows the changes in real RI, ML, and \( \Delta n \) respectively of the waveguide with \( W_d \) at 700, 500, 400 and 300 nm, where \( n \) and \( p \) concentrations of the waveguide are fixed at \( 1 \times 10^{17} \text{cm}^{-3} \) and \( 3 \times 10^{18} \text{cm}^{-3} \) respectively for Fig. 4.8(a)-(b) and is varied in Fig. 4.8(c). They show that ML change significantly with the changes of \( W_d \). This change in \( W_d \) however has negligible influence on the real RI and \( \Delta n \), which can be attributed to the negligible effect of \( W_d \) on changing carrier concentrations in the waveguide core.

For further clarity about optimum \( W_d \), E-field intensity of the confined mode is plotted for two values of \( W_d \) at 300 and 700 nm, as shown in Fig. 4.9(a)-(b) respectively. Fig. 4.9(a) shows that the confined mode struggles to be contained within the gap between the source and the drain, whereas in Fig. 4.9(b), it is contained properly. Therefore, the inadequacy of \( W_d \) that spreads the mode over metal contacts needs to be avoided to enable smaller ML, which was also indicated by Fig. 4.8(c). However, a larger \( W_d \) will result in lower operational speed.

### 4.3.5 Influence of core width \( W_w \)

![Graphs showing changes in waveguide parameters](image)

Fig. 4.10: Changes of waveguide parameters with respect to the changes in bias voltage and \( W_w \): (a) real RI vs. bias voltage; (b) ML vs. bias voltage, and (c) \( \Delta n \) vs. doping concentration.
Fig. 4.10(a)-(b) shows the changes in performance of the waveguide in real RI and ML at $W_w$ of 500, 700, 800 and 1000 nm with waveguide height fixed at 400 nm, n and p concentrations fixed respectively at $1\times10^{17}$ cm$^{-3}$ and $3\times10^{18}$ cm$^{-3}$, and bias voltage varied from 0 to -4 volts. Fig. 4.10(c), however, shows the change in $\Delta n$ with p concentrations varied from $1\times10^{17}$ cm$^{-3}$ to $3\times10^{18}$ cm$^{-3}$ by keeping other parameters unchanged. Similar to the responses of the changes to pad heights, increasing $W_w$ from 500 to 1000 nm significantly changes the real RIs. As shown in Fig. 4.10(b), the higher $W_w$ also increases ML which can be attributed to higher absorption caused by increased carriers accommodated in the higher $W_w$, which is also the reason for the increase in $\Delta n$ shown in Fig. 4.10(c). With non-uniform doping concentrations of $1\times10^{17}$ cm$^{-3}$ and $3\times10^{18}$ cm$^{-3}$ for n and p respectively, $W_w$ of 1000 nm, and bias voltage of -4 volts, the change in real RI is $2.02\times10^{-3}$ with a calculated loss of 29.5 dB/cm.

4.3.6 Characterizations with TM polarization

All the characterizations so far were with TE polarization. However, the effect of changing carrier concentration and bias voltage on TM polarization are now investigated. Similar to Section 4.3.2, the waveguide is characterized by varying concentrations of p from $5\times10^{17}$ cm$^{-3}$ to $3\times10^{18}$ cm$^{-3}$, keeping the concentration of n fixed to $1\times10^{17}$ cm$^{-3}$. Field distribution for the TM mode is shown in Fig. 4.11: the TM mode has a large overlap with top and bottom interfaces, whereas the TE mode had larger overlaps with sidewalls. The corresponding responses are shown in Fig. 4.12(a)-(c). The TM mode has a relatively lower effective RI compared to the TE mode. However, similar to the characteristics of the waveguide with TE polarization as shown in Fig. 4.5 (a)-(c), the characteristics with TM polarization are almost identical. This shows that the performance of the active waveguide under investigation is consistent for both TE and TM polarizations.

![Fig. 4.11: Mode field distribution ($E_x$) of TM polarized light.](image)
Fig. 4.12: Changes of waveguide parameters for TM polarization with respect to the changes in bias voltage and non-uniform doping concentration: (a): real RI vs. bias voltage; (b): ML vs. bias voltage, and (c): Δn vs. doping concentration.

4.3.7 Bending loss analysis

Fig. 4.13: Field profile of the confined mode with (a) no bend; (b) bending in right direction with 10µm bend radius.

Bending effects of active Si waveguides are particularly important for high data rates and highly dense photonic circuits. The effects of ‘narrow bends’ in the waveguides are characterized by solving the modes of the form expressed in Equ.3.4. In order to characterize the effects of bending on ML and RI, the waveguide is incorporated with narrow bending, and the respective plots are shown in Fig. 4.13(a)-(b) and in Fig. 4.14(a)-(b) at bias voltage of -4V. For characterization, the bend orientation angle is set as 90° which corresponds to a waveguide bend.
in right direction. Fig. 4.13 shows the field profile of the confined mode with: (a) no bend; (b) bending right with 10µm bend radius.

Fig. 4.14: Changes of waveguide parameters with respect to the changes in doping concentrations at -4V bias voltage: (a): loss vs. doping concentration for right bending; (b): Δn vs. doping concentration for bending.

Fig. 4.14(a) shows that for a nominal p doping, for example 5x10^{17} cm^{-3}, although the change in ML is quite negligible, it increases gradually at higher doping concentrations that must be considered while designing. Also, loss increases with sharper bends. Fig. 4.14(b) shows that at -4V bias voltage bending has a significant impact on the change in RI. Finally, Fig. 4.15 shows the radiative bending loss without the absorption loss. This result suggests that the maximum portion of total loss comes from absorption due to doping.

Fig. 4.15: Contribution of radiative bending loss to total loss for various bending radius.

4.3.8 Dispersion analysis

In this section, we investigate the achievable dispersion in active Si waveguides. The biasing and doping concentration attain changes in optical properties and provide greater control in
tailoring dispersion. Hence, small change in RI leads to significant change in dispersion. We first simulate the dispersion profiles of the designed waveguide in passive mode for better comparison. Then biasing and doping are applied to evaluate the effects on dispersion. Corresponding results are shown in Fig. 4.16(a)-(f). Fig. 4.16(a) shows the changes in dispersion for fixed core width of 500 nm, but varied core heights of 100, 200, 300 and 400 nm across 1.2 to 1.6 μm wavelength ranges. The trends of the results are similar to Section 3.3.1, though the values are different due to different waveguide dimensions.

Fig. 4.16: Changes of dispersion in active waveguide: (a): dispersion vs. wavelength for varying height at fixed 500 nm width; (b): dispersion vs. biased voltage for different heights; (c): dispersion vs. wavelength for varying width at fixed 300 nm height; (d): dispersion vs. biased voltage for different widths; (e) dispersion vs. wavelength for different bends with fixed height and width of 100 nm and 500 nm respectively, and (f) dispersion vs. biased voltage for different bends.
The effects of depleting carriers with bias voltages of 0 to -4V at 1550 nm wavelength are shown in Fig. 4.16(b). Due to high loss with high doping concentrations, we choose concentrations of 1x10^{17} cm^{-3} and 1x10^{18} cm^{-3} for n and p respectively in all dispersion characterizations. Anomalous dispersion with 400 nm height is varied from 2530 ps/(nm.km) to 1680 ps/(nm.km) for entire changes in bias voltage. Whereas, normal dispersion with 100 nm height is varied from -1330 ps/(nm.km) to -3250 ps/(nm.km). Similarly, Fig. 4.16(c)-(d) shows the dispersion for varying core widths of 400, 500, 700 and 1000 nm at fixed core height of 300 nm in both passive and active domain. Characterizations with passive waveguides in chapter 3 showed higher dispersion in waveguide bends. Here, bending effects on active waveguides are evaluated and corresponding results are shown in Fig. 4.16(e)-(f). Fig. 4.16(f) shows that dispersion as high as -9100 ps/(nm.km) is achievable at 1550 nm wavelength with -4V bias voltage with core height and width of 100 nm and 500 nm respectively.

### 4.4 Modelling and Characterization with PhC core

So far, a plain core active Si waveguide is investigated. This is now modified to a 1D PhC structure. To construct the active Si PhC waveguide, as shown in Fig. 4.17, a 450nm Si layer is grown on 1µm thick SiO₂ layer. The waveguide is defined as a 4.7µm wide region, and the remaining Si is etched back 300nm to leave a waveguide 300nm thick and 4.7µm wide, which sits on a 90nm thick Si pad and serves as the host medium for PhC. The PhC consists of dimensions of W_w=400nm, H_p=90nm, H_w=300nm and W_d=1µm. Metal (aluminium) contacts are defined with a distance of 1µm to the edge of the waveguide which are 100 nm thick. The top surface is passivated with a thick oxide layer. Careful selections of pad height (H_p) and doped region to waveguide distance (W_d) are important as because higher H_p and shorter W_d will suffer from higher ML due to entering of the mode into pad and its overlapping with high doped region respectively. H_p should be thin enough to avoid more ML but thick enough for fabrication feasibility. Again, W_d should be large enough to avoid such overlap but, short enough for high operational speed.
Inclusion of dopants into Si to enable space-charge regions, p-n junction, and electrical contacts are defined and modelled, similar to previous active waveguide without PhC. A negative bias of 0 to -4 volt is applied to deplete the carriers across the p-n junction and to characterize the distinctive features. Fig. 4.18(a)-(b) shows the mode field distribution of confined TE mode and the electrostatic with -4v bias voltage. After modelling the structure with p-type and n-type dopants, negative bias voltage is applied to deplete the carriers. Electron distribution as a function of applied bias is illustrated in Fig. 4.19(a)-(c) in log scale. Depletion layer gets widen by pushing free charge out of the waveguide with increasing negative drain contact voltage. Various responses of depleting carriers are described below for variations in bias voltage, doping concentrations, dimensions and operating wavelengths.
4.4.1 Uniform Doping Concentration

Firstly, the waveguide is analysed by uniformly changing n and p doping concentrations and the corresponding responses are plotted. Fig. 4.20(a)-(c) shows the respective changes in effective RI (real), ML and Δn for varying the n and p concentrations from $1 \times 10^{17}$ cm$^{-3}$ to $1 \times 10^{18}$ cm$^{-3}$ and applied reverse bias voltages from 0 to -4V. Shown in Fig. 4.20(a), real RI changes from 3.06621 to 3.065178 for the entire changes in n and p concentrations. With the increase in bias voltage real RI tends to increase. As shown in Fig. 4.20(b), ML changes significantly with
increasing doping concentrations and reaches up to 26.18 dB/cm at doping concentration of 1x10^{18} cm^{-3}. Dependence of \( \Delta n \) on doping concentration and bias voltage is also clearly visible in Fig. 4.20(c), as expected. With \(-4\)V bias voltage, a possible change in real RI is 1.03x10^{-3} for 1x10^{17} cm^{-3} doping concentration. This can be extended up to 1.16x10^{-3} for doping concentration of 1x10^{18} cm^{-3}.

4.4.2 Non-uniform Doping Concentration

To utilize the benefits of higher p concentrations compared to the n concentrations in terms of higher change in RI with lower absorption, the waveguide is characterized by varying concentration of p from 5x10^{17} cm^{-3} to 3x10^{18} cm^{-3} and the concentration of n fixed at 1x10^{17} cm^{-3}. The corresponding responses are plotted in Fig. 4.21(a)-(c). Fig. 4.21(a) shows that the real RIs change from 3.06588 to 3.06441 for the entire changes of p concentrations. With the increase in bias voltage, real RI tends to increase. As shown in Fig. 4.21(b), loss changes significantly with increasing doping concentrations and reaches to 29.34 dB/cm. Compared to Fig. 4.20(b), here similar amount of loss is expected but at a higher p concentration which gives rise to larger \( \Delta n \). For example in Section 4.4.1, with a uniform carrier concentration of 1x10^{18} cm^{-3} and bias voltage of -4 volts, change in real RI is 1.16x10^{-3} with calculated loss of
22.8 dB/cm. Whereas in case of non-uniform doping concentrations of 1x10^{17}\text{cm}^{-3} and 3x10^{18}\text{cm}^{-3} for n and p respectively and bias voltage of -4 volts, change in real RI is 1.941x10^{-3} with calculated loss of 27.7 dB/cm. This non-uniform carrier concentration provides flexibility of higher change in RI with little increase in ML.

4.4.3 Varying waveguide width ($W_w$)

Fig. 4.22: Changes of optical parameters with respect to bias voltage and changes in $W_w$: (a): real (RI) vs. bias voltage; (b): ML vs. bias voltage, and (c): $\Delta n$ vs. doping concentration.

Fig. 4.22(a)-(b) shows the changes in performance of the waveguide in real RI and ML at $W_w$ of 500, 660, 800 and 1000 nm with waveguide height fixed at 400 nm, n and p concentrations fixed respectively at 1x10^{17}\text{cm}^{-3} and 3x10^{19}\text{cm}^{-3}, and bias voltages varied from 0 to -4 volts. Fig. 4.22(c) shows the change in $\Delta n$ with p concentrations varied from 1x10^{17}\text{cm}^{-3} to 3x10^{18}\text{cm}^{-3} by keeping other parameters unchanged. Similar to section 4.3.5, increasing $W_w$ from 500 to 1000 nm significantly changes real RIs. As shown in Fig. 4.22(b), higher $W_w$ also increases ML which can be attributed to higher absorption caused by increased carriers accommodated in the higher $W_w$, which is also the reason for the increase in $\Delta n$ as shown in Fig. 4.22(c). With non-uniform doping concentrations of 1x10^{17}\text{cm}^{-3} and 3x10^{19}\text{cm}^{-3} for n and p respectively, $W_w$ of 1000 nm, and bias voltage of -4 volts, change in real RI is 2.097x10^{-3} with an increased loss of 4.43 dB/cm compared to $W_w$ of 500 nm.
4.4.4 Influence of pad height $H_p$

Fig. 4.23: Changes of waveguide parameters with respect to the changes in bias voltage and $H_p$: (a): real (RI) vs. bias voltage, (b): ML vs. bias voltage, and (c): $\Delta n$ vs. doping concentration.

Fig. 4.24: Mode field distribution for different $H_p$: (a): $H_p = 50$ nm, (b): $H_p = 120$ nm

Like Section 4.3.3, Fig. 4.23(a)-(c) shows the influence of different pad heights $H_p$ on real RIs, ML, and $\Delta n$ respectively. The n and p concentrations of the waveguide are fixed at $1 \times 10^{17} \text{cm}^{-3}$ and $3 \times 10^{18} \text{cm}^{-3}$ respectively for Fig. 4.23(a)-(b). However, for Fig. 4.23(c), the p concentrations are varied from $5 \times 10^{17} \text{cm}^{-3}$ to $3 \times 10^{18} \text{cm}^{-3}$ to quantify the effects of changing $\Delta n$. With an increased pad height $H_p$ from 50 nm to 120 nm, the real RI increases significantly from 3.027 to
3.106. This can be attributed to the fact that, as the mode is entering to the pad area, this will now also be contributing to RI, and so with increasing $H_p$, RI is also increasing. Higher $H_p$ also increases ML, which is caused mostly by the portion of light passing through the pad area. For further clarity, mode field distribution for $H_p$ 50 nm and 120 nm are shown in Fig. 4.24(a)-(b). Shown in Fig. 4.23(c), the thickness of $H_p$ has hardly any influence on $\Delta n$, although the RI and ML are influenced greatly.

### 4.4.5 Characterizations with TM polarization

Similar to Section 4.3.6, the effects of changing carrier concentrations and bias voltage on TM polarization are investigated. Field distribution for the TM mode is shown in Fig. 4.25 and the corresponding responses are shown in Fig. 4.26(a)-(c). TM mode has a relatively lower effective RI compared to TE mode. However, similar to the characteristics of the waveguide with TE polarization shown, the characteristics with TM polarization are almost identical. This shows that the performance of the active waveguide under investigation is consistent for both types of polarizations.

![Mode Field Distribution (E_x) of TM polarized light.](image-url)
4.4.6 Bending analysis

Similar to Section 4.3.7, to characterize the effects of bending on ML and RI, the waveguide is incorporated with narrow bending, and the respective plots are shown in Fig. 4.27(a)-(b) and in Fig. 4.28(a)-(b) at bias voltage of -4V. For characterization, the bend orientation angle is set as 90° which corresponds to a waveguide bend right direction. Fig. 4.27 shows the field profile of the confined mode with (a) no bend; (b) bending right with 10µm bend radius. Similar to Fig. 4.14(a)-(b), Fig. 4.28(a)-(b) shows the variation in loss for varying doping concentrations.
Finally, Fig. 4.29 shows the radiative bending loss without the absorption loss. This result suggests that the maximum portion of the total loss comes from the absorption due to doping.

Fig. 4.28: Changes of waveguide parameters with respect to the changes in doping concentrations at -4V bias voltage:
(a): loss vs. doping concentration for right bending; (b): Δn vs. doping concentration for varying bend.

Fig. 4.29: Contribution of radiative bending loss to total loss for various bending radius.

4.4.7 Dispersion analysis

Similar to section 4.3.8, here we investigate the achievable dispersion in 1D PhC active Si waveguides. Corresponding results are shown in Fig. 4.30(a)-(f). Fig. 4.30(a) shows the changes in dispersion for fixed core width of 400 nm, but varied core heights of 150, 200, 300 and 400 nm across 1.2 to 1.6 μm wavelength ranges. The trends of the results are similar to Section 3.3.3, though the values are different due to different waveguide dimensions. The effects of depleting carriers for bias voltages of 0 to -4V at 1550 nm wavelength are shown in Fig. 4.30(b). Similar to section 4.3.8, we choose doping concentrations of $1 \times 10^{17}$ cm$^{-3}$ and $1 \times 10^{18}$ cm$^{-3}$ for n and p respectively to avoid high losses.
Fig. 4.30: Changes of dispersion in active 1D PhC waveguide: (a) dispersion vs. wavelength for varying height at fixed 500 nm width; (b) dispersion vs. biased voltage for different heights; (c) dispersion vs. wavelength for varying width at fixed 300 nm height; (d) dispersion vs. biased voltage for different widths; (e) dispersion vs. wavelength for different bends with fixed height and width of 200 nm and 400 nm respectively, and (f) dispersion vs. biased voltage for different bends.

Compared to planar structure, dispersion varies largely in PhC structure. For example, normal dispersion with 100 nm height is varied from -1330 ps/(nm.km) to -3250 ps/(nm.km) in Fig.
4.16(b) for planar structure, whereas it varies from -1.11*10^4 ps/(nm.km) to -4.68*10^4 ps/(nm.km) with 200 nm height for PhC structure in Fig. 4.30(b). Fig. 4.30(c)-(d) shows the dispersion for varying core widths of 400, 500, 700 and 1000 nm at fixed core height of 200 nm in both passive and active domain. Bending effects on this waveguide is also evaluated with height and width of 200 nm and 400 nm respectively and corresponding results are shown in Fig. 4.30(e)-(f). Considerable change in dispersion from -0.192*10^5 ps/(nm.km) to -1.02*10^5 ps/(nm.km) for a change in bias voltage from 0 to -4V is found with 3μm bend radius at 1550 nm wavelength and is shown in Fig. 4.30(f).

4.5 Evaluation of active waveguides for TS-ADC

In Section 4.3.8 and Section 4.4.7, we have evaluated the dispersive nature of planar and 1D PhC active Si waveguides. Results from Section 4.3.8 suggest that at 1550 nm wavelength the maximum achievable normal dispersion in Si planar waveguide is about 9100 ps/(nm.km) with 3 μm bend radius at -4V bias voltage. Considerably higher dispersion is achieved with PhC structures. Results from Section 4.4.7 show normal dispersion as high as 1.02*10^5 ps/(nm.km) in waveguide bends with -4V bias voltage at 1550 nm wavelength.

As is explained in Section 3.4, realization of the proposed TS-ADC technique to digitize 100GHz RF signal requires normal dispersion amount of 3*10^5 ps/(nm.km) in the first Si waveguide, whereas 10 times more for the second waveguide. Although, dispersion is considerably enhanced in active waveguides compared to passive waveguides, it is still not suitably enough to replace the fibers. Three of the 1D PhC waveguides can be cascaded to replace the first fiber; however large number of waveguides to replace the second fiber is not realistic considering the design footprint as well as loss. Still, some design considerations can be made to use these active waveguides in the proposed TS-ADC design as follows.

- Dispersion in a waveguide will have greater impact on pulses with shorter width. In the design, we have considered a 100 fs pump pulse which is passed through the first dispersive waveguide to generate the chirped pulse. Instead, if we utilize a 50 fs pulse source, this will have nearly double dispersion effect and thus the requirement of dispersion in the waveguides will be half.
- A 100 GHz RF signal is expected to convert into 10 GHz signal after modulation and stretching. Alternatively, if the signal is targeted to convert into 20 GHz, the requirement of dispersion in the waveguides will be another half.
- In the dispersion analysis of active waveguides, doping concentrations of 1x10^17 cm^-3 and 1x10^18 cm^-3 for n and p respectively have been considered. A higher doping
concentration will lead to higher changes in guiding parameters and corresponding dispersion. However, this will be at the cost of relatively higher loss.

- A reduced waveguide height provides higher amount of dispersion. For example: Fig. 4.30(a) shows dispersion of -1.382*10^4 ps/(nm.km) for 150 nm height, which is reduced to -1.112*10^4 ps/(nm.km) for 200 nm height. Still we considered 200 nm height to evaluate the dispersion in bend waveguide in Fig. 4.30(b) which was to minimize the effect of loss. So, with proper optical amplification, structures with shorter height can be utilized to gain higher dispersion.

In chapter 3 and 4, we have systematically evaluated commonly used passive and active Si waveguides. The findings motivate us to research more complex waveguide structures to achieve higher dispersion amount for implementing high speed TS-ADC. These are explained as future research directions in chapter 8.

### 4.6 Summary

In this chapter, the responses of carrier refraction by depletion and waveguide geometry on various distinctive guiding parameters of active Si waveguides with planar and 1D PhC structure have been investigated. Trends of the characteristic parameters in both cases are similar except that the PhC structure exhibit relatively higher ML and also provides large Δn compared to planar structures. A non-uniform carrier concentration with higher p density allows greater changes in RI compared to the uniform doping density, but similar MLs. It is also shown that ML increases with higher doping concentrations and decrease with applied bias voltage in all cases. These need to be carefully controlled for specific applications.

Waveguide geometry and choosing the right placement of source and drain have a significant impact on the responses, especially on ML. Higher H_p increases ML considerably, which is caused mostly by the proportion of light passing through the pad area. Therefore H_p should be thin enough to decrease the ML but large enough to ensure fabrication feasibility. ML is also higher with shorter W_d because of overlapping of the mode with highly doped regions near metal contacts. However, H_p and W_d have only an insignificant effect on Δn: this can be attributed to the negligible influence of these parameters on changing carrier concentrations in the waveguide core.

Dispersion and bending properties were also analysed: these are particularly important for high data rates and dense circuits. Dispersion is considerably enhanced in active waveguides compared to passive waveguides. Higher dispersion is achievable with 1D PhC active waveguide bends which can be considered in our proposed TS-ADC design with some design considerations made in Section 4.5.
Chapter 5

Geometry Dependence and Performance Optimization of Photodiode

This chapter presents systematic numerical evaluation of geometry dependence and performance optimization of CMOS-compatible Ge on Si vertical photodetector including a lateral spot size converter for PICs. Performance enhanced distributed Bragg reflectors are introduced in vertical PD to reflect back the residual un-absorbed light, which effectively increases absorption length without adding any device capacitance. Transient behaviour and bandwidth dependence on geometry and bias voltage are analysed which are instrumental in developing optimal design solutions for specific application. Further investigations with a unitravelling carrier (UTC) PD comprised of InP/InGaAs III-V materials on a SOI layer show favourable dark current and higher bandwidth due to single carrier transition. Increase in transit time limited bandwidth with a graded doping profile instead of constant doping is proposed and evaluated. We show that our proposed designs of PDs can achieve low loss, high responsivity and high bandwidth and they can be well-suited for on chip integration of proposed TS-ADC application.

5.1 Introduction

In an integrated Si photonic platform, PDs have made unprecedented progress with extensive research on perusing high responsivity, low dark and leakage current, high bandwidth, low cost, low noise and fast response [328]. A PD operation in photo transistors, pn junctions, pin diodes, and avalanche diodes is performed in depletion mode because of their low operational voltages, high-speed properties, and high sensitivity [329]. Fig. 5.1 shows a typical schematic of a p-i-n photodiode and corresponding band diagram. When the intrinsic layer is illuminated by a photon with higher energy than the bandgap of the intrinsic layer material, it excites electrons from valance to the conduction band and results in mobile carriers. These carriers are separated by reverse bias voltage to create electrical current flowing from n side to the p side; this current is known as photo current. However, due to the poor responsivity of Si around short and long haul telecommunications, Germanium (Ge) is utilized as the active material which has 4.2% lattice mismatch with Si and places challenging obstacles towards monolithic integration [330]. Different state-of-the-art methods demonstrated to reduce such dislocations are discussed in Section 2.5.3.3.
Coupling schemes for PDs can be classified as surface normal and waveguide coupled as shown in Fig. 5.2. In the case of a surface-normal structure, light enters the absorbing region perpendicular to the substrate. On the other hand, in a waveguide-coupled structure, light enters parallel to the substrate. Commonly, surface normal PD has better efficiency and power handling capabilities than waveguide PDs. This is mainly because it is easier to attain uniform illumination for a surface-normal PD and also the thermal impedance tends to be lower [269]. However, a waveguide-coupled PD has larger bandwidth compared to a surface-normal PD [332].
Performance of the PD is evaluated based on responsivity, response time, leakage and dark current minimization, higher bandwidth, and so on. State-of-the-art demonstrations of various approaches to realize PD were discussed in Section 2.5.3 along with the fabrication approaches to minimize defects. This chapter brings a Ge on Si vertical n-i-p PD and CMOS-compatible UTC PD for a complete characterization of various distinctive characteristics parameters including dark current, photocurrent, responsivity, transient, and frequency response by incorporating changes in physical dimensions and bias voltages. Proposals of improved design solutions and doping profiles are also evaluated which show further enhancement in performance.

5.2 Theory, Modelling and Characterization

A vertical PD (VPD) is comprised of a vertical n-i-p junction where the thickness of the intrinsic region is determined by the thickness of Ge grown and also the thickness of the n region. The speed of the PDs can be optimized by manipulating the Ge dimension. Light passed through the Si waveguide will incident on the Ge layer and will be absorbed. The amount of light absorbed at a specific point in space can be calculated from the real part of the divergence of poynting vector \((\vec{P})\) as Equ. 5.1.

\[
P_{abs} = -0.5 \text{real}(\nabla \cdot \vec{P})
\]  

However, as absorption calculation from the divergence of the poynting vector tends to be sensitive to numerical problems, an equivalent but more numerically stable solution based on electric field intensity \((E)\) can be utilized as Equ. 5.2.

\[
P_{abs} = 0.5 \text{real}(i\omega \vec{E} \cdot \vec{D})
\]  
\[
= -0.5 \omega |E|^2 \text{imag}(\varepsilon)
\]  

According to this, to calculate the absorption as a function of space and frequency, only electric field intensity and imaginary part of permittivity \((\varepsilon)\) are required to be known. These can be measured in a FDTD simulation [333]. Absorbed photons per unit volume can further be calculated by simply dividing with energy per photon as Equ. 5.3.

\[
g = \frac{P_{abs}}{\hbar \omega} = \frac{-0.5|E|^2 \text{imag}(\varepsilon)}{\hbar}
\]  

5.3
\( \hbar \) is the reduced Planck constant, where \( \hbar = h/2\pi \) and \( h \) is the Planck constant. Absorbed photons will generate electron hole pairs which are swept from the depletion region by a generated electric field with reverse biasing and will produce the photo current. Quantum efficiency (\( \eta \)) and responsivity (\( R \)) are two important parameters which characterize the effectiveness of the photodetector. \( \eta \) is the probability of an incident photon to create carriers which will take part in the current generation and is affected by the material properties as well as waveguide geometry. On the other hand, \( R \) is the measure of output signal strength to incident optical power and is related to \( \eta \) as Equ. 5.4.

\[
R \left( \frac{A}{W} \right) = \frac{I_p}{P_{opt}} = \frac{\eta e}{h \nu} = \frac{\eta \lambda (\mu m)}{1.24} \tag{5.4}
\]

where, \( I_p \) is the photo current, \( P_{opt} \) is the input optical power, \( e \) is the electron charge, \( h \) is the plank constant, \( \nu \) is the frequency and \( \lambda \) is the wavelength. Under no illumination, unwanted current known as dark current is produced which is caused by several different processes [334].

At the depletion region boundary, electron on p and hole on n side tend to diffuse into the depletion region and get drifted by the reverse voltage which is known as saturation current and is a source of dark current. Carriers are also generated by thermal excitation in the depletion region which can also be swept away by drift and contribute to the dark current. This is known as Generation-Recombination (G-R) current. With enough reverse bias voltage, conduction band energy can fall below the valence band which will allow tunneling of carriers and will result in dark current. Tunneling can also occur due to sweeping of trapped carriers from thermal excitation. The surface of the device can also cause dark current known as surface leakage current due to the high density of the surface charge and interface state. Under sufficient reverse voltage, electrons can escape from their localized state in the conduction band and can contribute to dark current known as the Frankel-poole current. While drifting, carriers can hit and dislodge valance band electrons under enough reverse voltage which is known as impact ionization and will allow more dark current. Table 5-1 summarizes different contributing processes to dark current and corresponding dependence where \( E_g \) is the bandgap energy, \( k \) is the Boltzmann constant, \( T \) is the temperature, \( c \) is the velocity of light, and \( V \) is the applied bias voltage.
Table 5-1: Dark current dependence on various processes, where a, a’, b, and c are constants [334].

<table>
<thead>
<tr>
<th>Process</th>
<th>Dependence</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diffusion</td>
<td>( \propto \exp\left(-\frac{E_g}{kT}\right) )</td>
</tr>
<tr>
<td>G-R</td>
<td>( \propto \sqrt{V} \exp\left(-\frac{E_g}{2kT}\right) )</td>
</tr>
<tr>
<td>Band-to-band tunneling</td>
<td>( \propto V^2 \exp\left(-\frac{a}{V}\right) )</td>
</tr>
<tr>
<td>Trap-assisted tunneling</td>
<td>( \propto \exp\left(\frac{a'}{V}\right)^2 )</td>
</tr>
<tr>
<td>Surface Leakage</td>
<td>( \propto \exp\left(-\frac{E_g}{2kT}\right) )</td>
</tr>
<tr>
<td>Frankel-Proole</td>
<td>( \propto V \exp\left(-\frac{b}{T}\right) )</td>
</tr>
<tr>
<td>Impact Ionization</td>
<td>( \propto V \exp\left(-\frac{c}{T}\right) )</td>
</tr>
</tbody>
</table>

Bandwidth, which is an important feature of PD, depends on the applied reverse bias and degrades at lower voltages [335]. 3-dB bandwidth of the frequency response can be calculated from the Fourier transform of the impulse response. To model the vertical n-i-p photodiode as shown in Fig. 5.3, a 500 nm thick Ge layer is grown on top of 220 nm Si. A thick SiO\(_2\) layer under Si with respective width and thickness of 20 \( \mu \)m and 10 \( \mu \)m acts as the under cladding. 500 nm Si waveguide is converted to 5 \( \mu \)m through a lateral spot size converter, whereas the Ge layer is 10 \( \mu \)m long and 8\( \mu \)m wide. Two metal (Al) contacts 0.8 \( \mu \)m apart from the Ge layer act as an anode, whereas the other metal (Al) contact on top of Ge acts as the cathode. The top surface of the waveguide is passivated with a thick layer of oxide. To enable space-charge regions, inclusion of dopants into Ge is modelled by considering a background doping concentration of \( 1 \times 10^{10} \text{ cm}^{-3} \) for a p-type Ge epitaxial layer. The n-i-p junction was defined by using the analytic profiles of doping objects by diffusion that mimics the behaviour of an ion implant where the n and p concentrations are \( 5 \times 10^{18} \text{ cm}^{-3} \) and \( 2 \times 10^{18} \text{ cm}^{-3} \) respectively. Finally, to deplete the carriers generated from photons across the junction, a negative bias of 0 to -4 volt is applied and corresponding distinctive features including dark current, photocurrent, responsivity and bandwidth are characterized.
Among different simulation platforms to model the waveguide, this investigation relied on the commercially available Lumerical Solutions where the structure is designed and simulated in “Lumerical FDTD Solutions”. A 1-mW mode source with a telecommunication wavelength of...
1550 nm is used as the optical input. The injected mode propagates down the device and the number of absorbed photons in Ge is measured. This generation rate profile is then exported in a “Lumerical Device” to investigate electrical and transient characteristics. PML boundaries are used with sufficient layers to absorb outgoing waves from the interior of the computational region and also to restrict strongly any reflection from the boundaries. Fig. 5.4(a)-(b) shows the field coupling from Si to Ge layer in z-x and z-y plane respectively.

A 500*220 nm² Si waveguide is laterally tapered up to 5*0.22 μm² to increase coupling of light from the Si to the Ge layers. Lumerical Mode Solutions, which is fully vectorial bi-directional Maxwell's equations solver, is utilized to find the optimized taper length. To better resolve the geometry, the tapered Si waveguide is divided into sub-sells and a mesh override region is also added. A Continuously Varying Cross-sectional Sub-cell (CVCS) method is utilized to minimize the staircasing effect which is caused by discrete changes in cross-section between nearby cells [336]. Fig. 5.5 shows the mode conversion efficiency over different tapering lengths. To include the insertion loss, taper length is set to have a conversion efficiency of 90%. This is at an optimized taper length of approximately 10 μm.

![Graph showing conversion efficiency over tapering length](image)

Fig. 5.5: Changes in spot size conversion efficiency over tapering length.

A detail characterization of various responses of the designed PD such as dark current, photocurrent, responsivity and bandwidth with respect to the changes in bias voltage and physical dimension is undertaken as follows.

### 5.2.1 Influence of varying Ge height

Fig. 5.6(a)-(d) respectively shows the changes in dark current with respect to temperature and bias voltage, normalized photocurrent and responsivity for varying Ge heights of 250, 500, 750, and 900 nm with a reverse bias voltage of 0 to -4 volts. The photocurrent is normalized by its saturation photocurrent, which is taken to be the photocurrent at a bias voltage of −4 V. Like the increment of dark current with temperature and bias voltage, it increases with increasing the Ge height as is evident in Fig. 5.6(a)-(b). Shown in Fig. 5.6(c)-(d), normalized photocurrent and
responsivity of the PD also increase with increasing Ge height due to enhancement of photon absorption. However, this higher responsivity comes at the expense of operational speed and bandwidth, which is addressed later.

![Graphs showing changes in dark current, normalized photocurrent, and responsivity with varying Si heights.](image)

Fig. 5.6: Changes of characteristics parameters with respect to changes in bias voltage and Ge height: (a): DC vs. T; (b): DC vs. bias voltage; (c): normalized photo current vs. bias voltage, and (d): responsivity vs. bias voltage.

### 5.2.2 Influence of varying Si height

Fig. 5.7(a)-(d) respectively shows the changes for varying Si heights of 100, 150, 220, and 500 nm with a reverse bias voltage of 0 to -4 volts. As was the case previously, dark current increases with increasing temperature, bias voltage, but decreases with increasing Si height, as is evident in Fig. 5.7(a)-(b). Again, as shown in Fig. 5.7(c)-(d), normalized photocurrent and responsivity of the PD also decreases with increasing Si height. These can be attributed to the fact that a thicker Si layer will restrict the light from being absorbed by the Ge absorption layer effectively which also will affect the operational speed and bandwidth efficiency of the PD.
Fig. 5.7: Changes of characteristics parameters with respect to changes in bias voltage and Si height: (a): DC vs. T, (b): DC vs. bias voltage, (c): normalized photo current vs. bias voltage, and (d): responsivity vs. bias voltage.

5.2.3 Enhancing Responsivity by Bragg reflector

A longer length of Ge layer to increase responsivity will effectively increase device capacitance and can be avoided by replacing it with distributed Bragg reflectors (DBR) [337]. DBR at the end of the Ge layer will reflect the residual un-absorbed light which can be absorbed a second time. This will effectively increase absorption length without adding any device capacitance. The structure of the designed PD by including the DBR is shown in Fig. 5.8. The duty cycle, grating depth and pitch length of the designed DBR are 50%, 150 nm, and 0.3 μm respectively.
Fig. 5.9 shows the changes in responsivity for a varying DBR length with a reverse bias voltage of 0 to -4 volts. Inclusion of the DBR with only 2 μm shows that the responsivity increases from 0.74 to 0.89. A longer DBR achieves better responsivity but it does not increase much after 5 μm as most of the light has already been absorbed. Keeping the grating length, duty cycle, grating depth, and pitch length of the DBR to 10 μm, 50%, 150 nm, and 0.3 μm respectively, the wavelength response of the DBR is now analysed. Fig. 5.10 shows a maximum reflection of 68% at around 1550nm wavelength of the designed DBR. However, this efficiency is dependent of the dimension of the structure and can be varied by tailoring different parameters to fit a specific application. A maximum efficiency of 68% around 1550nm wavelength means that the most of the unabsorbed light coming towards the DBR will be reflected back.

![Graph showing changes in responsivity with bias voltage and DBR length](image1)

**Fig. 5.9:** Changes of responsivity with respect to changes in bias voltage and DBR length

![Graph showing wavelength dependence of DBR](image2)

**Fig. 5.10:** Wavelength dependence of the DBR.
5.2.4 Transient behaviour and frequency response

![Graph showing changes in frequency response for various bias voltages.](image)

Fig. 5.11: Changes in frequency response for various bias voltages.

Now, the transient behaviour and corresponding frequency responses of the PD are analysed. To perform this, contact voltage is modified as a function of time, where the anode is adjusted to be time dependent and cathode voltage is kept at 0 volts. For fixed voltage contacts, the solver applies same constant voltage at every time step. In anode, first and second time points are set as 0 ps and 1 μs respectively with -0.5 volts initially. The actual shutter effect of the optical generation box is applied through the transient tab of the solver region object to perform the step response. Thus, the step response and its derivative, the impulse response are attained, whereas, a normalized frequency response is achieved by carrying out FFT on impulse response. This response degrades significantly at low bias voltages as shown in Fig. 5.11, which shows the normalized frequency response of the PD for various bias voltages of 0, -0.5, -1, and -4 V. At -0.5 V bias voltage, 3-dB bandwidth is calculated as 17 GHz which can be increased to 24 GHz for a bias voltage of -4 V. However, this can be further optimized by manipulating PD dimensions and by including the DBR. The effects of Ge and Si heights on the bandwidth are characterized next at 0 bias voltage.

Fig. 5.12(a)-(b) shows the transient and frequency responses for varying Ge heights of 250, 500, 750, and 900 nm. As in Fig. 5.12(a) both impulse and step responses become slower with an increasing Ge height. Although the responsivity increases with increasing height as in Fig. 5.6(d), it requires a longer transit time and hence, low detection speed. Fig. 5.12(b) shows the normalized frequency response derived from the impulse response where the higher values of Ge height results in a lower 3-dB bandwidth and vice versa.
For varying Ge height (a): Normalized impulse and step response vs. time; (b): Normalized frequency response in dB.

Similar to Fig. 5.12(a)-(b), Fig. 5.13(a)-(b) shows the transient and frequency responses but for varying Si heights of 100, 150, 220, and 500 nm. As before, both impulse and step responses were faster at lower Si heights and are shown in Fig. 5.13(a). The light is evanescently coupled to the Ge layer from Si layer. When the Si layer thickness is increasing, light is more strongly confined in this layer. As a result, it gradually becomes more reluctant to evanescently couple to the Ge layer and tries to remain in Si layer. Thus, a thicker Si layer restricts light from being absorbed by the Ge layer effectively. Eventually the generation of carriers decreases. Also, a thicker Si layer requires longer transit time. This, in turn, decreases the bandwidth. The 3-dB bandwidth changes from 1 GHz to 4 GHz for changing Si height from 500 nm to 100 nm at 0 bias voltage as shown in Fig. 5.13(b).

For varying Si height (a): Normalized impulse and step response vs. time; (b): Normalized frequency response in dB.

5.3 Uni Travelling Carrier (UTC) PDs

In Si/Ge p-i-n PDs, the Ge layer thickness directly controls the quantum efficiency as well as diode capacitance, transit time limited bandwidth, and output current. With the increment of Ge thickness, capacitance decreases, which in turn increases the RC limited BW. However, it also increases the transit time of the carriers and results in reduced transit time limited BW. BW of
standard vertical n-i-p PD suffers from transit time and RC constant time limitations. Photon absorption takes place in the depletion region where both electron and hole take part in transit time and also the lumped nature of vertically-illuminated PDs rise RC time constant which limits the BW of operation. However, in the case of UTC PDs, photon generation takes place in a p-doped layer and only electrons act as the active carriers in the depletion region. This eventually offers lower transit time and achieves higher bandwidth with minimized space charge effect. Some demonstrations of UTC-PD utilizing InGaAs/InP III-V materials as well as Si/Ge structures were previously discussed in Section 2.3.4.4. Here, we introduce a InP/InGaAs based UTC structure heterogeneously integrated on Si photonic integrated circuit and further characterize the effect of the collection layer thickness and PD area on photo current, responsivity, transient response and bandwidth.

### 5.3.1 UTC PD: Design and Characterization

![Schematic of the simulated UTC PD](image)

Fig. 5.14: Schematic of the simulated UTC PD based on [338].

The UTC PD comprised of III-V materials on the SOI layer is shown in Fig. 5.14, based on [338]. 250 nm thick p doped InGaAs acts as the absorber layer. At higher frequencies, this highly doped undepleted absorber layer significantly reduces the voltage-dependent capacitance [339]. The collection layer comprises of a 700 nm intrinsic InP drift layer. A thin InP layer below the absorber facilitates wafer bonding onto Si and reduces defects propagation in the active region.
5.3.2 Influence of InP collection layer thickness

Fig. 5.15(a)-(c) respectively shows the changes in dark current with respect to bias voltage, normalized photocurrent, and responsivity for varying InP thickness of 250, 500, 700, and 900 nm, keeping the InGaAs absorber layer fixed at 250 nm with a reverse bias voltage of 0 to -4 volts. Fig. 5.15(a) shows that the dark current reduces with the increasing collection layer thickness. As shown in Fig. 5.15(b)-(c), normalized (by saturation photocurrent) photocurrent and responsivity of the PD decrease with an increasing InP thickness. However, higher responsivity with lower InP comes at the expense of lower operational speed, which is addressed later.

![Graphs showing changes in dark current, normalized photocurrent, and responsivity with respect to bias voltage and InP thickness.](image)

Fig. 5.15: Changes of characteristics parameters with respect to changes in bias voltage and InP thickness: (a): DC vs. bias voltage; (b): normalized photo current vs. bias voltage, and (c): responsivity vs. bias voltage.

5.3.3 Influence of PD length

Fig. 5.16(a)-(b) respectively shows the changes in normalized photocurrent and responsivity with respect to bias voltage of 0 to -4 volts for varying PD lengths of 25, 50, and 100 μm keeping the InP collection layer and InGaAs absorber layer fixed at 700 nm and 250 nm respectively. Photocurrent and responsivity both increase with a longer PD length due to higher coupling of photons. Although responsivity with 50 μm increases considerably compared to 25 μm, for 100 μm it does not vary much as most of the photons are absorbed within 50 μm PD lengths. However this higher responsivity with longer PD comes at the expense of lower operational speeds due to increased capacitance effect. This is also addressed in the next section.
5.3.4 RC limited BW dependence

The operational speed of the PD is influenced and restricted by RC values and transit time requirements. Maximum capacitance will build up across the collection layer. However, considering a conductive substrate, parasitic capacitance will form between the absorption layer and the substrate. Moreover, metal anode and cathode contacts will contribute to some contact capacitances. Different formations of capacitances in the structure are depicted and can be calculated as Eqn. 5.5:

$$C = (C_d + C_{sub})A + C_cL \tag{5.5}$$

Here, C is the total capacitance formed, whereas $C_d$, $C_c$, and $C_{sub}$ are capacitances formed across the collection layer, contact, and absorber layer. A and L are the area and length of the PD respectively. RC BW can be calculated utilizing the resistance model which includes load resistance ($R_L$) and resistivity of contact interfaces ($\rho_c$) as Eqn. 5.6 [340].

$$R = R_L + \frac{\rho_c}{A} \tag{5.6}$$

Where, $R_L = 50\Omega$ and $\rho_c = 10k\Omega.\mu m^2$. Fig. 5.17(a)-(b) show the changes in RC bandwidth with respect to bias voltage of 0 to -4 volts for varying PD length and width respectively, keeping the InP collection layer and InGaAs absorber layer at a fixed thickness. There is a decrement in BW by increasing both length and width and eventually the area of the PD and is clearly evident from the responses. This limits the increment of PD length to achieve high responsivity and requires a trade-off between both.
Fig. 5.17: Changes of BW over PD area: (a): BW vs. PD length with PD width fixed at 10 μm; (b): BW vs. PD width with PD length fixed at 50 μm.

5.3.5 BW dependence on InP collection layer

Fig. 5.18: Current travelling in the InP collection layer at different thickness point.

The InP collection layer has an important role in realizing the BW of the PD. Increasing the thickness will result in decreasing capacitance and will increase the corresponding RC limited BW; however, the transit limit BW will decrease due to an increment in transit time. Transit times of the carriers are calculated evaluating current density monitors at different thickness points of the InP layer for 500fs input pulse at 1550 nm wavelength and the corresponding result is shown in Fig. 5.18 at 0.25, 0.5, and 0.7 μm where PD length and width are fixed at 50μm and 10μm respectively. Broadening of the pulses due to dispersion is also visible from the response. Transit times ($\tau_0$) at 0.25, 0.5, and 0.7 μm thick InP are measured as 4.3, 8.5, and 12.5 ps respectively which can be utilized to measure the transit time limited BW according to Equ. 5.7.

$$f_{0, tr} = \frac{0.445}{\tau_{tr}} \quad 5.7$$
However, an overall BW of the PD will be a combination of both transit time and RC limited BW and can be calculated using Equ. 5.8 [341]:

\[ f_0 = \left( \frac{1}{f_{0,RC}} + \frac{1}{f_{0,tt}} \right)^{-\frac{1}{2}} \]  

5.8

Fig. 5.19 shows the changes in RC limited and transit time limited BW and also the overall BW for varying InP thickness from 400nm to 1μm keeping length and width of the PD fixed at 50 and 10 μm respectively. It shows that the RC limited BW increases with increasing InP thickness whilst the contrary happens for a transit time limited BW. As a result, the overall BW of the PD initially increases with increasing InP thickness and then at one point it starts to decrease where the transit limit BW becomes dominant. Therefore, the optimized performance requires careful selection and investigation of these design parameters.

Fig. 5.19: Changes of RC limited, transit time limited and overall BW for varying InP thickness.

5.3.6 Enhanced bandwidth with graded doping

So far we have used constant doping in p-InGaAs absorber layer and now investigate the effects of graded doping from $10^{17}$ cm$^{-3}$ at the top to $10^{19}$ cm$^{-3}$ at the bottom. This will further enhance the electron transport towards intrinsic InP collection layer and will decrease the transit time slightly. This can be attributed to the fact that the graded doping will induce a quasi-electric field which will drift the electrons faster. Fig. 5.20 shows the differences in BW comparing constant and graded doping profile and shows the higher BW achieved with graded doping in p-InGaAs.
5.4 Summary

The responses of vertical n-i-p Ge photodetector for various distinctive characteristics parameters including dark current, photocurrent, responsivity and bandwidth by incorporating changes in physical dimensions and bias voltages including a lateral spot size converter are investigated. In all cases, dark current increases with increasing temperature and applied bias voltage. A normalized photo current and responsivity increase with increasing Ge height due to enhancement in photon absorption, whereas there is a decrease when increasing Si height. This higher responsivity comes at the cost of structural compatibility and operational speed. DBR at the end of the Ge layer is proposed to reflect back the residual un-absorbed light, which is shown to effectively increase absorption length without adding any device capacitance. Influences of grating length, duty cycle, grating depth and pitch length are characterized and optimized. Finally, geometry dependence of transient and frequency responses of the designed PD is also investigated. These responses degrade significantly at low bias voltages. 3-dB bandwidth increases when decreasing Ge and Si height due to a fast transient response but at the expense of lower responsivity.

Next, we analyse the UTC PD where absorption and collection layers are separated which improves the dark current, photo current, responsivity, and BW efficiency. Dependence of these characteristics parameters on PD length, width, collection layer thickness is investigated. A longer PD increases the responsivity due to higher absorption but suffers from smaller BW resulting from higher capacitance. Again, a thicker InP collection layer achieves higher RC limited BW due to lower capacitance but suffers from lower transit time limited BW resulting from a longer transition time. Graded doping profile is proposed instead of constant doping which enhances the electron transport towards intrinsic collection layer and decreases the transit time. Eventually enhanced transit time limited bandwidth is achieved.

Bandwidth requirement of PD in the TS-ADC design decreases with stretching the modulated signal in time. However, here the Ge on Si PD shows a 3 dB bandwidth of 24 GHz for bias
voltage of -4V with high responsivity. UTC PD, which is preferable for low dark current, also shows a 3 dB bandwidth of 36 GHz for bias voltage of -4V with responsivity close to unity. With the proposed design options, we show that the resulting PDs with high responsivity, high bandwidth and low dark current properties making them highly suitable for on-chip integration of proposed TS-ADC.
A performance-enhanced butt coupling structure incorporating a vertically and laterally tapered SiON polymer core on Si to tunnel and widen propagating optical modes of adiabatic taper is proposed and suitable design options are evaluated. This structure can effectively overcome the strong back reflections caused at the interface between the fiber and Si nanowire to enable higher coupling efficiency. The placement of the SiON polymer core is chosen to restrict the passage of light through the bottom cladding to avoid unnecessary leakage. The performance of the structure is characterized by distinct features including tapering length, coupling efficiency and coupling bandwidth, and is also compared with the state-of-the-art grating coupler. It is found that, with the right set of design specifications, proposed butt coupler can outperform grating coupler in both coupling efficiency and bandwidth, although grating couplers are considered ‘friendlier’ for wafer-level testing.

6.1 Introduction

Si wire waveguides enable increased integration density by the virtue of its strong light confinement capability in the core. Added to that, with the advancement of cost effective CMOS processes, wide range of applications are expected to be performed in Si PICs. However, to accomplish specific applications, the wire waveguide requires to be connected to external optical devices, e.g., optical fibers, semiconductor lasers, and photodetectors. This creates considerable challenges to enable efficient coupling, which is caused mainly due to the mode-field differences, and the relative misalignments. To overcome these, various coupling mechanisms are proposed which are explained in details in Section 2.4.2. Out of these, coupling with a spot size converter (SSC) consisting of a Si inverse taper and a low index second core offers large misalignment tolerances and a low loss polarization independent operation [106-108]. However, in this chapter, we systematically evaluate the limitations of such butt coupling structure and provide new structural design to overcome these. To the best of our knowledge, we propose for the first time, a new structure by replacing the SiON rectangular polymer core with a laterally-and vertically-tapered core that reduces waste of light remarkably. The placement of the polymer core is also chosen in such a way that it restricts the passage of light.
through the bottom cladding to avoid unnecessary further wastage. The proposed design is also characterized for various coupling efficiencies with respect to tapering lengths and operating wavelengths to draw the performance bounds.

This chapter has taken a bottom-up approach to examine the performance of the tapers, with optimum design features and performances. Utilization of a low index second core to tunnel and widen the mode from an Si adiabatic taper is characterized in Section 6.2.1. Systematic evaluations of limitations of such SSC structures are presented in Section 6.2.1.1. Proposals of new structural designs to mitigate these limitations are provided in Section 6.2.1.2. Considerable improvements in coupling efficiencies are achieved with these proposed modifications. Section 6.3 evaluates the proposed design to couple light from and to a single mode fiber with corresponding coupling efficiency and bandwidth. In Section 6.4, proposed butt coupler is compared with state-of-the-art grating based couplers in terms of coupling length, efficiency and bandwidth. Some state-of-the-art fabrication solutions for lateral and vertical tapering are discussed in Section 6.5.

### 6.2 Modelling and characterization

The design and the characterizations relied on commercially available Lumerical Solution software and utilized the EME [Eigen Mode Expansion] method, which is a fully vectorial bi-directional Maxwell's equations solver. The EME method has advantages over FDTD based methods in simulation time and simulation numbers required for different taper lengths. Using this method, power transmitted in the Si waveguide is characterized after lateral and vertical tapering. The tapered Si waveguide is divided into sub-cells and a mesh override region is also added to better resolve the geometry. A continuously varying cross-sectional sub-cell (CVCS) method is utilized to minimize the staircasing effect, which is caused by discrete changes in the cross-section of nearby sub-cells [336].

![Fig. 6.1: Lateral SSC under investigation.](image)
For EME simulations, the number of cells used in tapered region, resolution of transverse mesh, and the number of modes will affect convergence. After a certain limit, increasing any of these properties will have a negligible impact on converter results. Fig. 6.2(a)-(c) shows the results for different numbers of cells, modes and resolution of transverse mesh with the structure in Fig. 6.1. With numbers of cells used in tapered region and mesh step size of the transverse mesh as
19 and 10nm respectively, Fig. 6.2(a) shows that 10 modes are sufficient. With longer tapering, the higher order modes become less important as the adiabatic limit is approached. Again with the numbers of modes used in each cell and mesh step sizes of the transverse mesh as 10 and 10nm respectively, Fig. 6.2(b) shows that 19 cells used in the tapered region are sufficient. Finally, with the number of modes used in each cell and the number of cells in tapered region as 10 and 19 respectively, Fig. 6.2(c) shows that 10nm of mesh step size of the transverse mesh is sufficient. So for the rest of the simulations, the number of cells used in the tapered region, the resolution of transverse mesh and the number of modes are used as 19, 10nm and 10 respectively.

6.2.1 SSC with a polymer second core

Coupling between waveguides with different cross-sectional areas are usually dictated by tapered waveguides that transform optical modes from one size to another. Traditional tapering approaches that employ a gradually narrowed or widened waveguide are affected by various issues including lower spot size expansion. To overcome such issues, a polymer core with a fiber-like cross-sectional area is first butt coupled to fiber and then placed onto a Si waveguide that is tapered to a width narrow enough to allow any propagating mode. The tapered Si waveguide, which is gradually widened adiabatically to the dimensions of Si nanowire, couples the light from the polymer core to the tapered Si waveguide and progressively confines light to the nanowire. A similar approach in the reverse direction can be applied to couple the propagating mode from the nanowire to the fiber. The mode needs to be fully released and expanded around the tapered Si tip, and correspondingly requires a tip width of less than 100 nm for efficient coupling. Again, a gradual increment of RI along the taper minimizes back reflection, thus offering a low loss coupling feature.

![Fig. 6.3: Initial dimension of SSC with a polymer (SiON) second core under investigation.](image-url)
Fig. 6.3 shows the initial dimensions of the SSC structure. To tunnel the light from Si wire to the polymer core, a 400*200 nm$^2$ Si wire is laterally tapered down to 80*200 nm$^2$. Typically, the taper is 200 μm long and the tip is less than 100 nm and are investigated in subsequent sections. Fig. 6.4(a)-(b) shows the field profiles of the propagating mode in x-y and x-z planes while transferring from the adiabatic taper to the polymer core. The 400*200 nm$^2$ nano wire is tapered down to 80*200 nm$^2$ and the mode is converted to the larger (4*4 μm$^2$) low index waveguide.

![Field profile](image)

Fig. 6.4: Field profile: (a) xy plane showing lateral conversion; (b) xz plane showing vertical conversion.

### 6.2.1.1 Performance Characterization

![Comparison of transmission over tapering length](image)

Fig. 6.5: Comparison of transmission over tapering length for SiO2 and SiON polymer core.
Firstly, the SSC is compared with SiO$_2$ (RI=1.44) and SiON (RI=1.5) as the low index core and the corresponding results are shown in Fig. 6.5. It shows that SiON outperforms SiO$_2$. The SiON polymer has advantages of less absorption and a lower index contrast with Si core compared to SiO$_2$ and also preserves higher humidity resistance. For the remaining investigations SiON will be used as the second core.

Secondly, the SSC is analysed for different SiON dimensions of 4*4, 6*6, and 8*8 $\mu$m$^2$. Waveguides with larger dimensions will have lower conversion efficiency and this is evident from the corresponding responses plotted in Fig. 6.6(a). With a tapering length of 250 $\mu$m, possible conversion for 4*4 $\mu$m$^2$ waveguide is 94% and reduces to only 52% for 8*8 $\mu$m$^2$. Thirdly, the SSC is analysed for various tip widths of 80, 120, and 160 nm and the corresponding responses are plotted in Fig. 6.6(b). The tip width of the taper is an important measurement and it is problematic to achieve an ultra narrow tip due to fabrication difficulties. It is evident that a sharper tip will perform better and will couple more light into the second core. It is observed in Fig. 6.6(b), with a 250 $\mu$m taper length, conversion efficiency with 80, 120, and 160 nm tip widths are 95%, 92.5%, and 70% respectively.

![Fig. 6.6: Changes of transmission over tapering length with down and up SSC for (a): different second core dimensions; (b): different tip widths.](image)

### 6.2.1.2 Performance Enhancement

Converting the mode to 8*8 $\mu$m$^2$ second core dimension shows an efficiency of only 52% and needs to be further enhanced. As shown in the inset of Fig. 6.4(b), a portion of light is wasted as it passes through the bottom cladding. Also, light inside the large rectangular polymer core is spread out all over the places. This restricts perfect evanescent coupling to/from the tapered Si waveguide. Moreover, as the second core tends to confine some portions of light, its cross section needs to be minimized, which in turn limits the required conversion of the guided mode [107].

Here, the proposed design provides two possible improvements in the SSC structure to increase the overall performance of butt coupling. First, by laterally and vertically tapering the second core to confirm more effective conversion of the guided mode. This tapering will itself
contribute to mode conversion and will also allow the mode to couple properly. At the same time, it can tolerate larger misalignments for butt coupling. This enlarged mode diameter would also offer easier assembling of photonic node chips in devices with highly multichannel interfaces. Second, placement of the second core from beneath the Si taper to capture the light passing through bottom cladding. Fig. 6.7 shows the proposed structure. Fig. 6.7 shows that the SiON polymer core is laterally and vertically tapered up from a cross-section of 1*1 μm² to the required cross-section of 8*8 μm² for effective coupling with SMF. A smooth and gradual transition in the tapered polymer core allows the mode to be converted suitably at a higher dimension for coupling. It also shows that the tapered core grows from 1 μm beneath the Si taper to capture the light that otherwise passes through the cladding.

Fig. 6.7: Initial dimension of SSC with a laterally and vertically tapered polymer (SiON) second core under investigation.

Fig. 6.8: Changes of conversion efficiency over tapering length for different tapered second core dimensions.
The SSC is analysed for different SiON dimensions of 4*4, 6*6, and 8*8 μm² which are laterally and vertically converted from 1*1 μm². Similar to Fig. 6.6, waveguides with larger dimensions show lower efficiencies and this evident from the corresponding responses plotted in Fig. 6.8. With a tapering length of 250 μm; possible conversion for 4*4 μm² waveguide is 97% which reduces to 78% for 8*8 μm². However, in comparison with Fig. 6.6(a), where 8*8 μm² waveguide showed efficiency of 52% after 250 μm tapering length, by utilizing a laterally and vertically tapered SiON core, Fig. 6.8 shows efficiency of 78%.

Fig. 6.9: (a): Changes of conversion efficiency over tapering length for different tapered second core dimensions; (b) conversion efficiencies for different placement depths of the SiON second core beneath the tapered Si core; (c) Comparison of conversion efficiency with and without improvements.
This improvement can be further increased to 83% with correct placement of the tapered SiON core, as shown in Fig. 6.9. In comparison with Fig. 6.8, where 8*8 µm² waveguide showed efficiency of 78% after 250 µm tapering length, modifying the structure by preventing light from passing to the cladding shows efficiency of 83%. Shown in Fig. 6.9(b), the changes in conversion efficiency for different placement depths of the tapered SiON core gradually increase, however becomes insignificant after 1 µm. Fig. 6.9(c) summarizes the SSC efficiency from a 400*200 nm² nanowire to 8*8 µm² with and without the proposed improvements and clearly shows the enhancement in performance. Typical SSC without any improvements shows 52% efficiency, whereas it improves to 77% with only tapering and to 83% with proper placement + tapering.

Fig. 6.10: (a): Electric field profile of the 400*200 nm² nanowire; (b): Electric field profile of the 8*8 µm² second core; (c): Frequency response of the SSC with and without proposed improvements.

Fig. 6.10(a)-(b) shows the electric field profile of the confined mode in 400*200 nm² nanowire and in 8*8 µm² second core. The measured modal area of 0.11 µm² in the nanowire is converted to 32.98 µm²: this provides a high spot size expansion factor of 300. Frequency response is an important measure when designing waveguide couplers where butt coupling performs better compared to grating based couplers. Here, the frequency responses of the SSC with and without
proposed improvements are measured over 1 to 3 µm wavelength bands and the corresponding responses are plotted in Fig. 6.10(c). It shows the maximum efficiency around 1500 nm wavelength and gradually decreases after that.

6.3 Coupling from and to single mode fiber

To have a complete characterization of the overall network, it is important to couple the light from and to fiber. Fig. 6.11 is a schematic diagram of a tapered SSC based butt coupler to couple light from SMF to nanowire and nanowire to SMF. Light from a SMF with a 9 µm core diameter is butt coupled to 8*8 µm² SiON polymer core which is tapered down to 400*200 nm² Si nano wire: the opposite happens when coupling light from the nanowire to SMF. Coupling to a SiON polymer core rather than to a Si core is much more efficient due to lower index contrast. This is measured with FDTD solutions as 96% at 1550 nm wavelength. Fig. 6.12 shows the overall efficiency of the complete network with and without the proposed improvements. Coupling efficiency of a conventional coupler is enhanced from 25% to 64% with the proposed modifications.

Fiber to nanowire coupling efficiency reaches up to 80% which corresponds to a total loss of only 0.96 dB, whereas overall coupling efficiency is 64% for the cascaded system depicted in Fig. 6.11. The performance of tapered butt couplers is primarily measured in terms of conversion efficiency, loss and required tapering length. Expansion of the guided mode from micro or nano waveguides to nearly fiber cross section is also important for efficient coupling; however this comes at the expense of a longer tapering length. Most of the previous tapered butt couplers convert the size only around 3*3 µm² [102, 106, 108-111], whereas the proposed
design converts the size from nanowire of $400 \times 200 \text{ nm}^2$ to $8 \times 8 \text{ \mu m}^2$ within a comparable tapering length of $250 \text{ \mu m}$. As a result the spot size is converted from $0.11 \text{ \mu m}^2$ to $32.98 \text{ \mu m}^2$; this corresponds to a very high spot size expansion factor of 300. Again, previous demonstrations with lower tapering lengths than ours exhibit higher losses and, most importantly, lower spot size expansion ratios [102, 106, 109-112]. By implementing the proposed modifications, both loss performance and coupling efficiency are greatly improved.

![Graph showing coupling efficiency with and without proposed improvements.](image)

**Fig. 6.12:** Overall coupling efficiency with and without proposed improvements.

### 6.4 Grating based couplers

Grating couplers, which mostly perform out of the plane coupling between fiber and waveguide, are found to be quite attractive as light can be coupled in and out everywhere on the chip, opening the way for wafer-scale testing. Grating couplers which favour dense integration and are capable of achieving reasonable efficiency within a short coupling length, have been the subject of extensive research for years. However, as the designed grating structure is wavelength-dependent, these couplers show a coupling bandwidth below 80 nm despite utilizing different optimization techniques [342]. Although the requirement for alignment accuracy in such couplers is relaxed, the precious control of incident angles of light on grating creates considerable challenges while packaging. However, perfectly vertical grating couplers to reduce packaging cost and complexity are demonstrated [90, 343, 344]
Here, the overall coupling efficiency with a grating based coupler is investigated and compared with the proposed design. The structural dimensions of the grating are shown in Fig. 6.13. The efficiency of a grating coupler is determined by the directionality of propagation of light where incident light from SMF to the top surface of the grating coupler propagates in three main directions. The first part of light diffracts towards the waveguide. The second part of light diffracts in the opposite direction of the waveguide, which can be redirected towards the waveguide by placing a second order grating. However, this portion of light is quite small compared to the first part and introduces additional complexity in the fabrication process, so can be ignored for simplicity. The third part of light, comprising about 30% of incident light, transmits through the BOX layer and adjacent Si substrate and contributes significantly to loss. The portion of light propagation in different directions can be visualized from the full field
profile shown in Fig. 6.14. The portion of light passing through the bottom cladding can be redirected by using Si Bragg reflectors [92, 345, 346].

Incident angle of light, grating pitch, duty cycle, pitch length and grating length are all important factors in controlling the coupling and should be optimized. A parameter sweep is used to simulate the coupled power as a function of incident angle. A single frequency mode at 1550nm is set to obtain these characteristics, shown in Fig. 6.15. It shows maximum coupling efficiency of 53% at around 13 degrees. A longer grating benefits by redirecting more light going in the opposite direction to the waveguide. A coupling efficiency at 1550 nm wavelength is calculated for a range of values, such as grating length from 5 to 20 µm, pitch length from 600 to 700 nm, duty cycle from 30 to 80% and etch depth of the grating from 50 to 150 nm. The corresponding responses are plotted in Fig. 6.16(a)-(d). In Fig. 6.16(a), coupling efficiency reaches its maximum after 15 µm of grating length, whereas Fig. 6.16(c)-(d) shows that coupling efficiency decreases above and below a particular value for pitch length, duty cycle, and etch depth and therefore needs to be carefully designed.

Next, the coupling efficiency is calculated over 1.5 to 1.6 µm wavelengths to couple light from fiber to the waveguide by considering optimized values of incident angle of light, etch depth, duty cycle, pitch length, and grating length as 13°, 100 nm, 0.66, 660 nm, and 15 µm respectively. Coupling efficiency at 1550 nm is found to be 53% without Bragg reflectors. This is extended up to 65% by placing three Bragg reflectors below the grating and the corresponding responses are plotted in Fig. 6.17. The dimensions of the Bragg reflectors are given in Fig. 6.13. However, overall coupling efficiency is found to be 41%, which is much less than the proposed design. Fig. 6.18(a)-(b) compares the coupling efficiency as well as bandwidth responses of both types of couplers.
Fig. 6.16: Coupling efficiency for various distinguishable parameters; (a): coupling efficiency vs grating length; (b): coupling efficiency vs pitch length; (c): coupling efficiency vs duty cycle; (d): coupling efficiency vs etch depth.

Fig. 6.17: Comparison of coupling efficiency over wavelength from fiber to the Si waveguide with and without reflectors.

In Fig. 6.18(a), the maximum possible efficiency with grating coupler is 41% whereas with proposed design improvements in a tapered SSC butt coupler it reaches 64%. However, it requires longer tapering to confirm smooth tunneling of light to the polymer core whereas grating couplers benefit from shorter coupling length. A grating coupler is also beneficial as light can be coupled into and out of everywhere on the chip. But again, it suffers from having a shorter bandwidth as the grating is designed for a specific operating wavelength as is clear from Fig. 6.18(b). Conversely, butt coupling benefits from efficient wideband coupling.
6.5 Fabrication overview

In the proposed SSC design, Si is tapered laterally, whereas the SiON polymer core is tapered both laterally and vertically. However, it is easier to fabricate lateral tapers where only waveguide widths need to be varied and can be accomplished by designing a mask with lateral tapers. A lateral ultra-narrow inverse taper structure by the double-patterning method which utilize photolithography as shown in Fig. 6.19 is demonstrated in [111]. A waveguide structure formed after photoresist and subsequent dry etching steps is attached with a parallelogram structure. Again, in Fig. 6.19(b) coated photoresist is patterned to remove another parallelogram area followed by an etching process to remove the bare Si area. A controlled etching achieving vertical sidewall allows an ultra-narrow structure with a high aspect ratio near the tip. Fabrication tolerance to achieve narrow tip width will allow the confined mode to transfer to second core more effectively and will reduce the required tapering length to a great extent.

One-way tapering is easily achievable, whereas vertical tapering is challenging as it requires special growth and etching techniques to achieve precise control over thickness variation. However, despite all challenges, vertical tapering has been demonstrated in several different ways in the last three decades. Etching techniques to realize vertical tapering can primarily be classified as wet and dry etching [347]. Different wet etching techniques include dip-etch [348], dynamic etch mask [349], stepped etching [350] and diffusion limited etching [351]. In contrast, dry etching techniques include oxide or direct shadow etching [352] and shadow masked reactive ion etching [353]. On the other hand, special growth techniques involve a temperature gradient during molecular beam epitaxy [354], liquid phase epitaxy growth on a ridge [355], selective area growth [356] and shadow mask growth by chemical beam epitaxy [357]. Although most of the early demonstrations are focused to realize tapering in III-V semiconductor materials, those techniques can be modified for tapering silica waveguides. Some such demonstrations include flame hydrolysis deposition with a special modulation of
raw materials [358], shadow mask sputtering [359, 360], a modified local oxidation (LOCOS) process [361] and a controlled resist reflow technique [362].

Using the dynamic etch mask technique, the layer to be tapered will first need to be covered by a dynamic mask which has a significantly higher etch rate. Additionally, a photoresist is deposited which is kept open near the dynamic mask and where the deeply etched end is to be created. As a dynamic mask has a high etching rate, more and more material is exposed to the chemical etchant. However, the length of the taper structures achieved by using this process is limited to around 50 μm [349]. Tapering from 0 to 6 μm thickness over a 2-mm tapering length is documented by the shadow mask sputtering method [359]. There a spacer made of Si chip is first put on a Si substrate and then a metal shadow mask is placed on the spacer covering half part of that substrate. Finally when a thin film is deposited on the substrate by RF sputtering, a vertically tapered portion is formed under the edge of the shadow mask. Using another approach, a vertically tapered photoresist pattern is designed using standard lithography and a sliding-mask technique [363, 364]. The mask contains a raster which has fixed spacing but a gradually increased opening. Regions with larger openings along the taper are more exposed than smaller opening areas, and this creates a gradient in the exposure time as shown in Fig. 6.20. Experimental validation of the resist reflow profile and subsequent transfer of tapering into Si and SiO₂ is presented in [362]. There one lithography step is used to define photoresist and a mask is designed with a composed array of trenches whose density depends on the amount of the photoresist that needs to be removed. Photolithographically defining the pattern followed by a reflow of photoresist to planarize strip of material transforms the original flat surface into a tapered shape. Tapering in the photoresist layer can be subsequently transferred to Si or silica by using a plasma-etching technique. The slope angle of the taper can be controlled by controlling...
resist/oxide or resist/Si etch rate ratio. In summary, although achieving vertical tapering is challenging and requires extra processing steps, it can be achieved by utilizing any favourable processes as explained.

An imperfect resist pattern causes roughness on the sidewalls. ECR plasma etching with SF$_6$–CF$_4$ gas mixture performed at low gas pressure and low-energy ions irradiate a wafer confirms little damage with hardly re-deposition of any reaction products while etching [365]. It is also important to select proper plasma conditions as well as proper material to use as the etching mask. A SiON second core can be deposited by PECVD. A mixture of O$_2$, N$_2$, and SiH$_4$ gases to deposit the SiON film gives the control to manage its RI over a wide range. This was used as 1.5 in the simulations. Fig. 6.21(a)-(c) show SEM images of a 400 nm Si waveguide, a 80 nm wide taper tip after etching, and a 3*3 μm$^2$ SiON with vertical and smooth sidewalls achieved in [366]. To ensure low propagation loss, it is important to achieve smoother sidewalls by controlling the fabrication process. Oxidation removes sidewall roughness and this eventually reduces propagation loss [366].
6.6 Summary

A new structure for butt coupling by incorporating both laterally and vertically tapered SiON polymer second core is proposed in this chapter: this reduces leakage of light remarkably. The placement of the second core is also chosen in such a way that it restricts the passage of light through the bottom cladding to avoid unnecessary wastage. The proposed design overcomes the limitations of conventional approaches and increases coupling efficiency by 31% at a tapering length of 250 µm with a spot size expansion of 300. Further, the proposed design can be fabricated by using state-of-the-art fabrication approaches although vertical tapering may require some additional post-processing steps. The performance of the design is compared with the performance of grating couplers in terms of tapering length, coupling efficiency and coupling bandwidth. Although grating couplers are advantageous for wafer-level testing, results show that the proposed butt coupler can outperform grating couplers in both coupling efficiency and bandwidth.
Chapter 7

Efficient Polarization Rotation in Si nanowire

To integrate many discrete functional blocks into a larger PIC suitable for applications such as TS-ADC, controlling polarisation within the PIC becomes a challenge. In this chapter, the design and operation of a CMOS compatible polarization rotator based on asymmetrical Si waveguide is presented. New structural designs are proposed by introducing 1D PhC structure. This structure achieves strict confinement of modes in the asymmetric structure which provides a large difference in the effective RI of two fundamental modes and substantially reduces the rotation length. A novel approach of lateral tapering is introduced in the rotator device which further reduces the device length. Addition to these, a CMOS compatible SiN/SiO$_2$ structure is proposed. Numerical evaluation of the proposed design shows rotator length less than 4 μm with high operational bandwidth of >700nm which covers the entire short and long haul telecommunication bands.

7.1 Introduction

Strong polarization dependence of SOI functional devices due to high index contrast of the SOI materials, limit PICs in the SOI platform from large-scale commercialization [146]. Therefore, building compact and highly efficient PICs including components, modules, and systems to realize the on-chip optical interconnect with high density and low power consumption require polarization management. Polarization-diversity approach is a suitable solution to manage the polarization, where the key elements are polarization beam splitters (PBS) and polarization rotators (PRs) [131]. A PBS separates the input light into two orthogonally polarized beams, while a PR rotates the polarization state of one beam into its orthogonal counterpart (TE to TM, or vice versa) [153]. Compared with Group III–V waveguides of similar dimensions, SOI waveguides provide stronger optical confinement and also can be fabricated at relatively low cost. Various configurations have been explored to demonstrate PR on SOI platform, including angled walls [367], cut-corner structure [368], subwavelength trenches [122], twisted waveguides [150], over layer of different materials [142]. However, these devices either suffer from a large device footprint or multiple additional fabrication steps [153]. Recently, PRs based on plasmonic waveguide [147] and waveguide bends [150] are presented to minimize device
footprint. Also polarization splitter rotators (PSRs) are used to control PRs [117]; however these structures have large device length of few hundred μm. Device length of PR is a critical parameter. Although longer length provides higher efficiency, from the viewpoint of integration, it needs to be as short as possible. Achieving simultaneously high PR efficiency, low loss, high bandwidth and high tolerance to fabrication imperfections is desired for such devices to achieve large scale Si photonics integration.

Different approaches to achieve these are discussed in Section 2.3.4. Although, some of the demonstrations achieve considerable operational bandwidth, the device length is too high for compact PICs [130, 143, 144, 148, 149]. On the other hand, most of the demonstrations which achieve preferable device length are failed to offer high operational bandwidth [129, 141, 142, 146, 147, 151, 153]. Hence, finding an ultrashort device length with low loss and especially very high operational bandwidth is still a challenge. This chapter provides suitable solutions to these challenges and achieve a high performance, ultra-compact PR with very high operational bandwidth. Section 7.2.1 presents a typical PR based on asymmetrical waveguide structure and evaluates its performances. New structural design by introducing 1D PhC in the rotator device is presented in Section 7.2.2. Section 7.2.3 describes a novel approach of lateral tapering in the rotator device to further reduce the device length. This is further modified with SiN/SiO2 waveguide presented in Section 7.2.4. The influences of waveguide dimensions and higher order modes on overall performance are also characterized.

7.2 Modelling and Characterization

Two modes in a waveguide with different effective RIs (n₁ and n₂) will accumulate different phases after propagating certain distances. If the propagation length is sufficient to provide a π phase difference, then the conversion length (L) can be written as Equ. 7.1.

\[
\text{Phase difference, } \pi = \frac{2\pi L}{\lambda/n_1} = \frac{2\pi L}{\lambda/n_2} \implies L = \frac{\lambda}{2(n_1-n_2)}
\]  

Equation 7.1

Utilizing this principle, here, a PR based on Si waveguides with asymmetrical cross sections is designed. Modes are hybridized by the geometric asymmetry and become transverse electric (TE) and transverse magnetic (TM). In general, modes are weakly hybridized in multiple-section PRs, while single section devices provide fully hybridized, nearly equal TE and TM components. Polarizations of the modes in the PR device need to be rotated by 45 degrees with respect to incoming TE or TM mode. The modes of waveguide B should be around 50% TE and
50% TM which are non-degenerate with different RIs. TE and TM fractions of the confined mode are defined according to the equations below.

$$\text{TE fraction} = 1 - \frac{\int |E_{\perp}|^2 \, dx \, dy}{\int (|E|^2) \, dx \, dy}$$

$$\text{TM fraction} = 1 - \frac{\int |H_{\perp}|^2 \, dx \, dy}{\int (|H|^2) \, dx \, dy}$$

7.2

Where, $E_{\perp}$ and $H_{\perp}$ refer to the field components in the direction of propagation perpendicular to the mode cross section. A full 3D EME simulation of Mode Solutions is utilized to characterize the PR efficiency.

7.2.1 PR with asymmetrical Si waveguide:

Fig. 7.1: (a) Waveguide A structure; (b) Waveguide B structure.

Fig. 7.1(a) shows waveguide A, in which the fundamental mode is 100% TE. The values of W and H in Fig. 7.1(a) are 1μm and 900nm respectively. Waveguide B in Fig. 7.1(b) is designed to support quasi-TE and TM modes (approximately 50% each) which will convert the TE mode of waveguide A into TM mode. Values of $W_a$, $W_T$, $H_a$, and $H_b$ in Fig. 7.1(b) are 750nm, 1.5μm,
750nm and 750nm respectively. To form the PR device, waveguide B is coupled with waveguide A as shown in Fig. 7.2. The inset in Fig. 7.2 shows the meshing, EME port and simulation region set up. Initially, the simulation is performed with first two modes of the waveguides, which avoids the influence of higher order modes on performance. Later, the higher order modes are also included to evaluate the interference.

Fig. 7.2: Combined structure of waveguides A and B to perform the PR.

Fig. 7.3: E-field intensity of (a) TE mode in waveguide A; (b) Quasi-TE mode in waveguide B; (c) Quasi-TM mode in waveguide B; (d) TM mode in waveguide B.
Fig. 7.3 shows the mode field distributions of waveguides A and B. Shown in Fig. 7.3(b)-(c), the first two quasi-modes of waveguide B as have 45% TE and 55% TM with effective RIs of $n_1=3.281598$ and $n_2=3.276398$ at 1550nm wavelength. Using Equ. 7.1, L is calculated as 149μm and the rotator device is simulated to evaluate the mode conversion efficiency with rotator length. Shown in Fig. 7.4, the calculated L is well matched with simulation results. It shows that the TE mode of waveguide A is fully converted to TM mode at around 150μm rotator length with approximately 62% efficiency. However, this simple asymmetric structure is showing poor PR efficiency as well as very high rotation length and needs to be modified for high performance and compact integration.

So far, only the first two modes of waveguide B were chosen. However, as waveguide B supports higher order modes, so the TE mode of waveguide A will also be expanded into those modes. This interference with higher order modes will cause some beats in the output which affect the stability of the modes. Different number of modes such as 2, 4 and 8 are chosen for waveguide B to see the influence of higher order modes on rotator performance and the results are shown in Fig. 7.5(a)-(c). This shows how the higher order modes are affecting the rotator performance.
7.2.2 Compact design with 1D PhC Si nanowire

As shown in Fig. 7.4, the rotation efficiency of the initial design is only around 60% and the rotation length is as high as 150μm. This is improved by making more compact dimensions and by introducing a 1D PhC structure. This provides flexibility to engineer the effective RI of the structure to enhance guiding capabilities. Strict confinement of modes in the 1D PhC asymmetric structures will achieve a large difference in the effective RI of two fundamental modes and substantially will reduce the rotation length.

Fig. 7.6(a) shows waveguide A with fundamental mode of 100% TE. The values of W and H in Fig. 7.6(a) are changed to 800nm and 700nm respectively. Waveguide B in Fig. 7.6(b) is designed to support quasi-TE and TM modes (about 50% each) which will convert the TE mode of waveguide A into TM mode. Values of \( W_a, W_T, H_a, \) and \( H_b \) in Fig. 7.6(b) are 600nm,
1000nm, 400nm, and 400nm respectively. To form the PR device, waveguide B is coupled with waveguide A as shown in Fig. 7.7.

Fig. 7.6: Compact structures (a) Waveguide A; (b) Waveguide B.

Fig. 7.7: Combined structure of waveguide A and B to perform the PR.
Fig. 7.8 shows the mode field distributions of waveguides A and B for the new structural design. The first two quasi-modes of waveguide B have 49% TE and 51% TM with effective RIs of $n_1=2.935914$ and $n_2=2.862$ at 1550nm wavelength. Using Equ. 7.1, L is calculated as 10.48 μm and the rotator device is simulated to evaluate the mode conversion efficiency with rotator length. Shown in Fig. 7.9, the calculated L is well matched with the simulation results. With the proposed structure, the TE mode of waveguide A is fully converted to TM mode within 10.5 μm rotator length with more than 90% efficiency. Compared to Fig. 7.4, PR efficiency as well as rotational length is considerably improved.

![Fig. 7.8: E-field intensity of (a) TE mode in waveguide A; (b) Quasi-TE mode in waveguide B; (c) Quasi-TM mode in waveguide B; (d) TM mode in waveguide B.](image)

![Fig. 7.9: Conversion from TE mode to TM of waveguide A.](image)
As we can see, the dimensions of waveguide B influence the overall performance of the rotator device considerably. In this section, we vary the value of $W_b$ and evaluate its impact on PR performance. Fig. 7.10(a) shows the response for varying $W_a$ from 400nm to 700nm and keeping $W_T$, $H_a$, and $H_b$ in Fig. 7.6(b) fixed at 1000nm, 400nm, and 400nm respectively. With $W_a=500nm$, the length required for the rotation has been further reduced to only 7.5μm, but at the expense of efficiency which is now about 81%. Fig. 7.10(b)-(c) shows the impact of varying $W_a$ on rotation efficiency and required length respectively. Although the device’s length decreases with a lessening $W_a$, PR efficiency peaks at around 600nm.

![Fig. 7.10: Impact of varying $W_b$ values: (a) Conversion from TE mode to TM mode at $W_a=500nm$; (b) PR efficiency Vs $W_a$; (c) rotation length Vs $W_a$.](image)

Frequency response is an important measure to analyse the overall performance of such a PR. So far, the characterizations have been performed with a 1550nm wavelength which has been extended from 1μm to 2μm in this section. Fig. 7.11 shows the PR efficiency and required length with respect to wavelength which covers the short and long haul telecommunication bands. In Fig. 7.11(a), the designed PR shows a large bandwidth of more than 800nm with ensuring more than 90% efficiency. The compact 1D PhC structure facilitates to achieve such high operational bandwidth. This is optimized for 1550 nm wavelength and the maximum conversion efficiency reduces for higher or lower wavelength than that. This is because of the deviation of the quasi modes from 50% TE and 50% TM. In Fig. 7.11(b), the required length for
the rotation decreases for higher wavelengths. With the increase in wavelength, effective RI of the confined modes decreases. However, difference in the RIs of first two modes \((n_1-n_2)\) increases, which in turn reduces the rotation length.

![Fig. 7.11: Wavelength response of the designed rotator, (a) PR efficiency Vs wavelength; (b) Rotation length Vs wavelength.](image)

### 7.2.3 Lateral tapering in rotator device

In this section, we propose a new PR structure with lateral tapering in the rotator device. If the values of \(W_a\) and \(W_T\) in Fig. 7.6(b) are changed to 450nm and 850nm respectively, the first two quasi modes supported in waveguide B becomes 24% TE and 76% TM instead of 50% each. Keeping the dimension of waveguide A unchanged, simulation of the PR with new waveguide B dimensions is shown in Fig. 7.12. Although, it results in low efficiency, the PR length has been reduced compared to Fig. 7.9. However, as the quasi modes are not about 50% each, the modes cannot convert fully and therefore, we cannot utilize such dimensions.

![Fig. 7.12: Conversion from TE mode to TM for waveguide B dimensions of \(W_a=450\text{nm}\) and \(W_T=850\text{nm}\).](image)
Fig. 7.13: Compact structures (a) Waveguide A; (b) Tapered Waveguide B.

Fig. 7.14: Combined structure of waveguide A and laterally tapered waveguide B to perform the PR.
To combine the reduced rotator length with higher conversion efficiency, we propose a new design structure of lateral tapering in the rotator device as shown in Fig. 7.13(b). Here, the initial dimensions of the waveguide B are set as $W_b=450\,\text{nm}$ and $W_b=850\,\text{nm}$, which are laterally tapered to final dimensions of $W_a=600\,\text{nm}$ and $W_f=1000\,\text{nm}$. Values of $H_a$ and $H_b$ remain the same as 400 nm each. To form the complete PR device, tapered waveguide B is coupled with waveguide A as shown in Fig. 7.14. With the proposed structure, the TE mode of waveguide A is fully converted to TM mode within 10.5 $\mu\text{m}$ rotator length with more than 95% efficiency. Compared to Fig. 7.9, PR efficiency as well as rotational length is considerably improved.

Similar to Fig. 7.10, $W_a$ is varied to see its impact on overall performance with lateral tapering. Value of $W_b$ is kept fixed at 450 nm. Results are shown in Fig. 7.16 for varying $W_a$ from 400nm to 700nm. With $W_a=500\,\text{nm}$, the length required for the rotation has been further reduced to only 6 $\mu\text{m}$, but at the expense of efficiency which is now about 88%. Fig. 7.16(b)-(c) shows the impact of varying $W_a$ on efficiency and required length respectively. Although the device length is decreasing with decreasing $W_a$, the efficiency peaks at around 550nm. Fig. 7.17(a)-(b) shows the PR efficiency and required length with respect to wavelength from 1.1 $\mu\text{m}$ to 1.8 $\mu\text{m}$. In Fig. 7.17(a), the designed PR shows a large bandwidth of more than 700nm with more than 90% efficiency. In Fig. 7.17(b), the required length for the rotation decreases for higher wavelengths, similar to Fig. 7.11(b). This is for the same reason explained in Section 7.2.2.
Fig. 7.16: Impact of varying $W_b$ values: (a) Conversion from TE mode to TM at $W_b=500$nm; (b) PR efficiency Vs $W_b$; (c) rotation length Vs $W_b$.

![Graph](image)

Fig. 7.17: Wavelength response of the designed rotator, (a) PR efficiency Vs wavelength; (b) Rotation length Vs wavelength.

![Graph](image)

Finally, the impact of higher order modes on the proposed design is investigated as was done in Fig. 7.5. Different number of modes such as 2, 4 and 8 are chosen for waveguide B to see the influence of higher order modes and the results are shown in Fig. 7.18(a)-(c). Compared to Fig. 7.5, in the proposed design with 1D PhC structure and lateral tapering in PR device, the impact of higher order modes on overall performance is quite negligible.
Fig. 7.18: Beats due to interference with higher order modes (a) with 2 modes; (b) with 4 modes; (c) with 8 modes.

7.2.4 Replacing Si core by SiN

Si Nitride (SiN) is a good candidate for thin film optical devices due to its chemical stability, high RI and low optical loss. Compared to Si waveguides, SiN presents suitable compromise between low surface roughness control and index contrast [369]. SiN films deposited by plasma-enhanced chemical vapour deposition (PECVD) for fabrications of optical devices at low temperatures have become attractive [370]. By adjusting deposition parameters, this provides the control of structural and optical properties of the deposited films. The effects of SiH₄/N₂ flow ratio, rf power and post-annealing on RI, deposition rate and surface morphology of SiN films grown by PECVD for low loss operations are studied in [369]. SiN/SiO₂ waveguide fabricated by PECVD with dual frequency reactors shows significant reduction in stress [371]. Also, SiN layers grown by low-pressure chemical vapour deposition (LPCVD) employing a thermal cycling process achieve very low propagation loss [372].
In this section, keeping the dimensions same, the Si core is replaced with SiN (RI=2.36), which gives a higher difference in $n_1$ and $n_2$. Corresponding performance is evaluated in Fig. 7.19. Compared to Fig. 7.15, the device length is further reduced to only 4 μm. Effect of $W_a$ on efficiency and rotator length is also performed. Similar to Fig. 7.16, device length decreases with decreasing $W_a$ with little reduction in efficiency. Fig. 7.20 shows that the TE mode of waveguide A is fully converted to TM mode within the rotator length of only 3.8μm at $W_a=500\text{nm}$.

![Graph](image1.png)

Fig. 7.19: Conversion from TE mode to TM mode with lateral tapering and SiN core material.

![Graph](image2.png)

Fig. 7.20: Conversion from TE mode to TM mode with $W_a=500\text{nm}$. 
7.3 Summary

The design and operation of a PR based on an asymmetrical 1D PhC Si waveguide has been investigated in this chapter. An initial design without the 1D PhC structure shows that the required length for rotation is around 150 μm with 62% efficiency. The proposed PhC structure helps to achieve strong confinement of modes in the asymmetric structure which provide a large difference in effective RIs of two fundamental modes and greatly reduces the device length. The proposed design shows that the required length for rotation has reduced to 10.5 μm with 91% efficiency. Again, a new structure of lateral tapering in rotator device is proposed which achieves fast conversion of the modes and reduces the rotation length to 7μm.

Addition to these, a CMOS compatible SiN/SiO₂ structure is proposed. This makes the rotator length <4μm. Geometric dependence of the asymmetric waveguide on rotator performance is investigated. High operational bandwidth of >700nm with more than 90% PR efficiency is achieved which covers the entire short and long haul telecommunication bands. According to our knowledge, this is the best to date performance of PRs which makes it suitable for polarization control in compact PICs.
Chapter 8

Conclusions and Future Research Directions

8.1 Key Conclusions

The main motivations of this research were primarily related to the proposal, theoretical analysis and numerical evaluations of various Si based waveguides to realize single chip solution of the TS-ADC target application. Fulfilling the target requires thorough investigations of various passive and active Si waveguides to meet required design specifications and is presented in chapter 3 and 4. Improvements of different design components in the targeted PIC such as PD, coupler, polarization controller are also important, which are presented in chapter 5, 6 and 7 respectively.

In chapter 3, a typical TS-ADC technique is modified with proposals of replacing long fibers by dispersive Si waveguides for single chip integrations. The most popular forms of passive Si wire, rib and PhC waveguides are systematically evaluated with and without bends to meet required dispersion profiles for the target application over 1.2 to 1.6 μm short haul and long haul telecommunication bands. However, none of the waveguides are dispersive enough to be used in the proposed TS-ADC design. While cascade of waveguides explored in this section could potentially be used to achieve the dispersion levels required, this option will require significantly larger photonic integrated circuits making it practically infeasible from the cost as well as the loss perspectives. This led us to investigate active Si waveguides, where with geometry, the control of biasing and doping concentrations will provide greater control to tailor dispersion.

Systematic evaluation of active reverse biased PIN structures with and without PhC with changes in waveguide dimensions, doping concentrations and applied biasing are presented in chapter 4. Compared to passive waveguides, dispersion is greatly enhanced in active waveguides, especially in 1D PhC structure with bends. Although, dispersion achieved in active waveguides under consideration is not suitably enough for the proposed high speed TS-ADC, some design considerations mentioned in Section 4.5 allow successful implementation.

Chapter 5 presents systematic numerical evaluation of geometry dependence and performance optimization of CMOS-compatible Ge on Si vertical photodetector for PICs. Performance enhanced distributed Bragg reflectors are introduced in vertical PD to reflect back the residual un-absorbed light, which effectively increases absorption length without adding any device capacitance. Also increase in transit time limited bandwidth with a graded doping profile instead of constant doping is proposed and evaluated. Our proposed designs of PDs can achieve low
loss, high responsivity and high bandwidth and they can be well-suited for on chip integration of proposed TS-ADC application.

One of the key challenges with submicronic waveguide devices is to enable efficient coupling with fiber, which is caused mainly due to the mode-field differences between fiber and waveguide, and the relative misalignments. Chapter 6 proposes a performance-enhanced butt coupling structure incorporating a vertically and laterally tapered SiON polymer core on Si to tunnel and widen propagating optical modes of adiabatic taper. The placement of the SiON polymer core is chosen to restrict the passage of light through the bottom cladding to avoid unnecessary leakage: this further enhances the performance. Evaluation of the proposed design to couple light from and to a single mode fiber and comparing with grating based couplers in terms of coupling length and bandwidth is also presented.

As we integrate many discrete functional blocks into a larger PIC suitable for applications such as TS-ADC, controlling polarisation within the PIC becomes a challenge. In chapter 7, new structural designs are proposed by introducing 1D PhC structure and replacing the core by SiN. This shows considerable reduction in rotator length with very high operational bandwidth. Additional to these modifications, a novel approach of lateral tapering is introduced in the rotator device which further reduces the device length.

### 8.2 Future research directions

Keeping the on chip TS-ADC as primarily targeted application, this work presented new and innovative design proposals, theoretical analysis and numerical evaluations of various Si based waveguides including modifications of various PIC components. As Si photonic integrated circuits is rapidly expanding, the study presented here provides more impetus for further research into pushing the limits of what is currently possible to be manufactured and seek to introduce modifications to manufacturing and design of such key functional blocks. In the course of this research, we identify number of key research challenges or issues of future relevance, which would require further research. We outline those challenges briefly to provide some inspiration to those who seek to advance these further:

- The real-time capture and processing of ultrafast electrical signals in wideband communications, image processing, THz detection etc. requires ADCs with a sampling rate of 100 GS/s or more. The proposed on chip integrations of the TS-ADC to perform such operations requires highly dispersive Si waveguides. We have evaluated dispersion properties in common forms of passive and active Si waveguides, which can perform the TS-ADC operation with some design considerations. However, for ultra-high speed
operations, dispersion in some other complex form of waveguides can be investigated. For example: A further investigation of passive and active 2D PhC structures as stand-alone configurations or embedded within ring resonators configurations to create recirculating dispersive elements is needed to evaluate compact but scalable dispersive elements within the photonic integrated circuit functional blocks. With proper design, strong dispersion can be achieved at the band edge near a PhC bandgap. Active control also allows adjusting the position of the band by modifying effective RI through plasma dispersion effect. With switchable ring resonator configurations, one should be able to realise arbitrarily large dispersive values. These all will provide greater control in tailoring dispersion in Si waveguides.

- Investigation of interdependent phenomena of different optical properties in most popular forms of passive and active Si waveguides is performed. These are mostly the linear optical properties which have numerous applications including our primary target application. However, non-linear effects need to be carefully handled especially at high input power. Complete characterization and geometry dependence of non-linear optical parameters can be performed which have potential to fit in specific applications like optical soliton, wavelength conversion, supercontinuum generation, self-phase and cross-phase modulation, and so on.

- In chapter 6, It is found that, with the right set of design specifications, butt couplers can outperform grating couplers in both coupling efficiency and bandwidth, although grating couplers are considered ‘friendlier’ for wafer-level testing. Grating couplers also favour dense integration and are capable of achieving reasonable efficiency within a short coupling length. Therefore, it could be useful to enhance the efficiency and coupling bandwidth of grating couplers by incorporating special grating structure designs to realize ultra compact solutions.

- The state-of-the-art polarization rotators are mostly based on passive Si waveguides. Passive and active tuning of the stress-induced birefringence for achieving polarization independence in a variety of photonic components is described in [373]. Strain-optic modification of the RI for active phase control on a photonic chip is also presented recently [374]. Active control of polarization rotation in Si waveguides are however limited and can be researched further to achieve highly efficient more compact design solutions. The use of such devices to engineer the state polarization at ingress and egress of functional modules would also warrant further investigation.
Development of the whole photonic ADCs on a CMOS-compatible chip so that both the electronic and optical processing can be co-developed monolithically on a single Si-substrate requires integrating the laser as well. However, laser is the most challenging and is yet to perfectly develop for successful integration. For successful EPIC implementation, the integrated laser needs to be efficient in emission at the designed wavelength, compatible with CMOS processing, and electrically pumped. Although, there have been several approaches towards these goals as explained in Section 2.6, it requires further research.

Several new structural designs have been proposed in this work and have been numerically evaluated. The designed and characterized devices can be fabricated for further validation. Improvement in fabrication process is important for performance enhancement. Though the fabrication processes for most of the structures used in the investigations are already well demonstrated but still will open up new challenges and opportunities for further optimization in terms of structural design and fabrication tolerances.
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