

An integrated circuit towards improved management of epilepsy and other neurological conditions

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Abstract

Epilepsy is the second-most common neurological disorder, with an estimated prevalence of 1% worldwide. Antiepileptic drugs (AEDs) are the frontline treatment but, despite more than 25 agents available, there can be significant difficulties in finding a treatment plan that controls seizures without unacceptable side effects. Furthermore, approximately 30% of patients do not obtain full control of seizures with the available AEDs. Therefore, there exists a need for novel therapies.

Therapeutic electrical stimulation of the brain and peripheral nervous system has shown great promise in treating those with refractory epilepsy, but still little is known about the mechanisms underlying this. Recent work looking at prolonged recordings of the brain has revealed a deep rhythmicity to seizures that may provide a method of developing patient-specific prediction algorithms that could be used to titrate electrical stimulation therapies. What is missing in research and in clinical practise is an implantable device which provides enough flexibility to explore new paradigms and adapt to suit the needs of the patient. Safety considerations of implantable devices necessarily precedes large-scale clinical evaluation, and this has prevented exploration of speculative higher density arrays, which come at a cost to power, complexity and mechanical reliability with no guarantee of improvement to efficacy.

Rather than redesign the system from scratch, this PhD thesis asks, “how can existing implantable technology be leveraged to create flexible high-density brain recording and stimulation systems?” In response to this question, an integrated circuit called XPAND was designed to enable seamless expansions of electrode count for a wide variety of commercial stimulators. Comprising a 6 x 64 element high voltage crosspoint switch powered and configured entirely using biphasic stimulation pulses, XPAND was designed with clinical safety in mind. Fabricated in Austria Microsystems H35 high voltage CMOS process, key modules within the chip were characterised, and the crosspoint switch shown to simultaneously route high voltage stimulation and ECG signals.

Declaration

This is to certify that

- a) the thesis comprises only my original work towards the PhD except where indicated in the preface;
- b) due acknowledgement has been made in the text to all other material used; and
- c) the thesis is fewer than 100,000 words in length, exclusive of tables, maps, bibliographies and appendices.

A handwritten signature in black ink, appearing to read 'Kyle Slater', with a large, stylized initial 'K'.

Kyle Damon Slater, October 2020

Acknowledgements

I started my PhD looking at ways to improve music experience for hearing impaired people using the sense of touch and 10 years later I have fabricated a chip towards improving the management of epilepsy! In 2015 I cofounded a company called nura dedicated to improving music experience and now in 2020 I find myself helping to build a second company called Seer revolutionising epilepsy diagnostics. There are threads in life that only ever make sense on reflection. I'm very grateful for the opportunities I've had to explore and learn, and I can't wait to return the favour when the time comes.

One of the silver linings of a *slightly* protracted thesis was the opportunity to work with so many incredible people. I could write pages and pages of thanks – but I will try to keep it punchy.

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Preface: Impacts of Covid-19

Best efforts were made in the experimental validation of the integrated circuit presented in this thesis. With restrictions in place in Melbourne – limited access to laboratory equipment and software presented some interesting challenges! This did not substantially impact the ability to acquire data and test the integrated circuit that was fabricated but it did make things much more difficult. A number of test circuits and scripts were needed to conduct testing in an ad-hoc home-based lab setup.

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1 Introduction

The human brain can be observed and measured in many ways through advanced imaging technology, such as functional magnetic resonance imaging (fMRI) that infers brain activity through increased blood flow, or technologies like electroencephalography (EEG) that measure the electrical fields associated with synchronised neural firing. These important technologies have helped to shed light on the inner workings of our most mysterious organ. However, it is safe to say that our understanding of how the brain controls some of the most basic functions in the body is still not well understood.

Our lack of understanding of the brain has made understanding conditions of the brain, such as epilepsy, difficult but not completely impossible. Epilepsy is not a condition that occurs through the normal functioning of the brain but is rather unstable behaviour of the brain. In these moments of instability, synchronous neuronal firing causes large and measurable changes in the observable electrical fields, which can be reliably detected using EEG or other measurements. The use of high-density EEG recordings over prolonged periods could further aid in our understanding of patient-specific conditions by understanding the origin and spread of neurological instabilities.

This thesis is motivated by looking at new ways to improve the management and treatment of epilepsy. In this chapter, an introduction to epilepsy aetiology, diagnosis and treatment will be provided. This establishes the motivation for some of the nascent technologies utilising functional stimulation that are rapidly finding their place as adjunctive treatments to standard anti-epileptic medication. Offering the promise of seizure freedom without drug treatment, implantable stimulation and recording technologies are gaining momentum. However, several engineering challenges still remain, and to this end, a review of the modern neural interface will be provided.

1.1 What is epilepsy?

Epilepsy is often used synonymously with the word “seizure”, which is commonly referred to as a fit, turn, spell or attack by the public [1], evoking imagery of uncontrollable convulsive shaking. However, not all seizures involve motor function and epilepsy is not always the cause [2].

Broadly speaking, epilepsy is the condition of recurrent and unprovoked seizures, and a seizure is an alteration in neurologic function caused by excessive, hyper-synchronous discharge of neurons in the brain [3]. These changes can alter a person's behaviour, mood, awareness (consciousness), sensation and movement.

1.1.1 Aetiology

The causes (aetiology) of epilepsy have evolved from supernatural theories of ancient times to more sophisticated concepts based on early concepts of cerebral cortical localization developed by Hughlings Jackson in the 1800's, to currently a deeper classification and understanding driven by clinical and molecular biochemistry, neuroimaging, molecular genetics, mechanisms of epilepsy, risk factor analysis and classification [4]. Aetiology can be divided into three broad categories: Genetic, Structural/Metabolic or Unknown [5]. Typically, structural causes include brain insult, infection, stroke and tumours. Approximately one third of patients are said to be idiopathic where the cause is unknown [5].

Due to the broad and often undetermined aetiology of epileptic seizures, patient symptoms and the electroencephalography (EEG) are still used to classify the nature of their condition. More recent classification schemes incorporate imaging abnormalities and other investigational

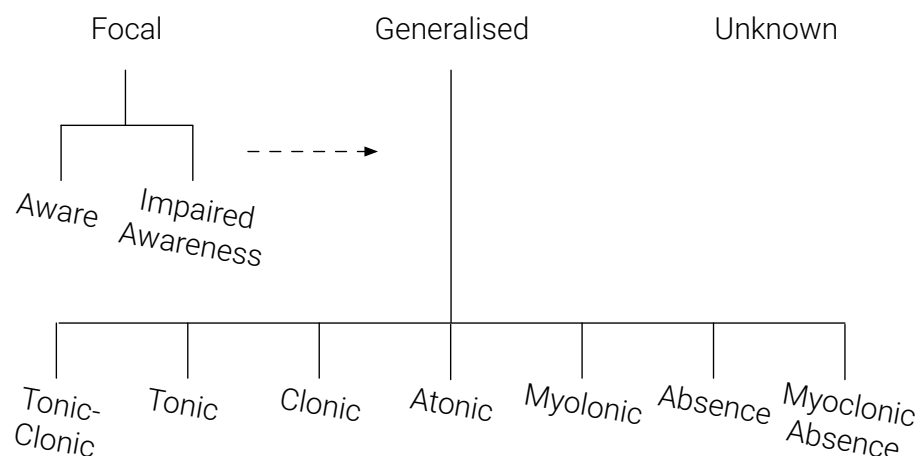


Figure 1-1 Epilepsy classification by seizure type.

results such as genetic abnormalities. Seizure classifications are shown in , with characteristic behaviour, as summarised in Table 1-1. [5]

Table 1-1 Descriptions of the characteristic behaviours for seizure types [6].

Seizure type	Characteristic behaviour
Focal	Seizure originating in specific part of the brain. May or may not spread.
Aware	Patient aware. Butterflies, déjà vu, strange taste.
Impaired Awareness	Confused, dazed often strange repetitive motions.
Generalised	Seizure involving both hemispheres of the brain.
<i>Tonic-Clonic</i>	Body stiffens followed by rhythmic jerking movements.
<i>Tonic</i>	Body stiffens.
<i>Clonic</i>	Repetitive rhythmic jerks.
<i>Atonic</i>	Sudden loss in muscle tone.
<i>Myoclonic</i>	Shock like jerks.
<i>Absence</i>	Brief non-motor seizure that causes lapse in awareness.
<i>Myoclonic Absence</i>	Rhythmic myoclonic jerks with tonic contractions.
Unknown	No determinations made.

What begins as a focal seizure can sometimes spread to both hemispheres of the brain where it is said to generalise [7]. But in any case, a seizure is typically experienced in three phases: a beginning (aura) where the person often has a feeling the seizure is imminent; a middle (ictal) phase where the seizure actually occurs and the characteristic behaviour described above is experienced; finally, a post-ictal phase where the patient recovers.

Seizures can be triggered by certain situations that change physiological state or external stimulations. These can include but are not limited to missed medication, sleep deprivation, stress, infection, hormonal changes, bright lights[8]. While perceptively the person affected may feel this is exclusively happening in response to certain stimulus, brain states primed to seizure occurrence have been shown to build up over hours or even days before the event [9, 10]. Going back nearly 100 years, clinical observations suggested an underlying rhythmicity could be present [11, 12], and recent studies based on chronic brain monitoring confirm this to be the case [13].

1.1.2 Diagnosis

Epilepsy is a very difficult condition to diagnose, largely due to the intermittency of events and overlap with other cardiac or neurological disorders. A large population study looking at

diagnostic accuracy in 1998, found that 49 of 214 patients originally diagnosed with epilepsy were found to have other causes of seizure-like events. These included cardiovascular or cerebrovascular pathology, underlying psychopathology, and single seizure events [14]. Other studies reported 20-30% of those diagnosed epilepsy may have cardiac syncope, which cause seizure-like symptoms due to cerebral hypoxia [15].

Epilepsy diagnostics are generally undertaken after observation or experience of seizure-like behaviour and the neurologist who is tasked with making an assessment needs to discriminate epileptic seizures from a number of mimics, including psychogenic seizures (PNES) and underlying cardiac conditions such as syncope.

There are a number of diagnostic tests a neurologist may perform to better understand the nature of the events. These include:

- Electroencephalography (EEG) to observe the electrical activity of the brain
- Electrocardiography (ECG) to observe the electrical activity of the heart
- Brain imaging using either computed tomography (CT) or magnetic resonance imaging (MRI) to look for structural abnormalities
- functional magnetic resonance imaging (fMRI), Single-photon emission computed tomography (SPECT) or positron emission tomography (PET) to localise the origin

Neurologists will also look at the patients history and seizure logs or diaries, though studies have shown they are not always an accurate representation of the patients events [16]. Week-long inpatient video-EEG was demonstrated in early 2000's to deliver high yield diagnostics by providing an "eye witness" account in the event a seizure occurred [17]. Even in the absence of a seizure, high quality EEG was recorded and reviewed for epileptiform discharges [17].

In recent years, week-long at-home ambulatory video-EEG has been shown to be equally effective as inpatient monitoring but with improved patient experience and reduction in cost[18]. With the addition of ECG also, Neurologists can view the behavioural manifestation and also differentiate between epileptic, cardiac and psychogenic causes.

1.1.3 Treatment

Anti-epileptic drug (AED) therapy is the frontline treatment for epilepsy and, in a large number of patients, proves successful in reducing seizure frequency [19]. However, studies have shown that up to 30% of people prescribed these medications do not receive adequate seizure control despite use of several medications [20]. These people are said to suffer refractory epilepsy. There are now in excess of 28 registered AED drugs [20] that span a diverse group of pharmacological agents, which typically act to suppress neuronal excitability that in turn reduces the susceptibility of triggering a seizure. However, adverse effects, both acute and developed over many years, often result since they are not targeted and they are toxic [21].

A treatment plan is usually a trial and error process between the patient and the neurologist, whereby an acceptable balance between seizure suppression and the overall side effects of the medication is met. If the patient outcome is unacceptable with multiple AEDs, they may be assessed for resective surgery, whereby a portion of the brain is removed. This process is high risk, but has proven remarkably successful [22].

Invasive investigation using ECOG (electrocorticography) grids placed directly on the surface of the brain, has greatly assisted in surgical planning. While non-invasive techniques such as scalp EEG can be used to measure brain activity, these measurements are noisy and lack spatial and temporal resolution. In contrast to this, intracranial electrocorticography (EcOG), where high electrode count grids of millimetre scale disc electrodes are placed subdurally on the surface of the brain, enables relatively high spatiotemporal brain monitoring. In addition to this, direct electrical stimulation of the brain can be carried out through the same electrodes. Electrical stimulation in the context of surgical planning serves a dual purpose. First, by stimulating the electrodes one at a time, the neurologists can attempt to elicit a seizure. The electrode that triggers the patient's habitual seizures is likely in proximity to the seizure focus. Second, adjacent electrodes can be stimulated through a process known as Brain Mapping to better understand the underlying function of the brain near seizure foci. This is particularly important for eloquent regions where speech and movement could be affected if resected. Once assessed, the locations are co-registered with brain imaging to give the neurosurgeon precise information about the resection [23].

Over the past decade there have been substantial advances in the use of implantable devices to treat refractory epilepsy as an alternative to surgical resection. These implants are called neuromodulation devices, and they deliver electrical stimulation to specific locations in the brain and peripheral nervous system. The general idea is that they are able to stabilise brain function in a much more targeted way compared to AEDs and come with fewer side effects as a result [24]. That said, some can only be prescribed as an adjunctive treatment and may only reduce the AEDs the patient is already on. Neuromodulation holds the promise of a drug free and seizure free life with few side effects – but more research is needed [25].

Implantable technology to measure the brain can also play a more indirect role in patient outcome, by helping patients to anticipate seizure occurrence. One of the most difficult aspects of living with epilepsy is not knowing when a seizure will occur. Substantial research spanning decades has been committed to a field known as seizure prediction – which aims to provide an early warning to the patient, well in advance to the ‘aura’ some may feel in the moments immediately prior to an event. Primarily, this allows the patient to prepare themselves and move out of harm’s way [26], but which could also potentially provide a trigger for various therapies, both pharmacological and electrical. However, epilepsy-related mortality is not confined to car accidents and drowning, but also is the result of comorbidities such as depression and anxiety. Providing an alert to help anticipate seizures, reduces anxiety [27].

1.2 Nascent Treatment Technology

Implantable electronic stimulators have proven remarkably successful in delivering meaningful improvement to patient health and wellbeing. From the cardiac pacemaker in 1951 [28] through to the cochlear implant for restoration of hearing dating back to 1957 [29], there is no question about the value therapeutic stimulation can deliver. The use of direct stimulation for the treatment epilepsy also has a long history dating back to the 1950’s [30]. Numerous target locations and stimulation paradigms have since been explored and will be discussed in further detail in Section 1.2.1.

Promising new research aiming to predict or forecast a patient’s seizures has emerged in recent decades – and its practical implementation has become a possibility with advances in implantable technology, cloud infrastructure and artificial neural network technology to

interpret vast repositories of time series data [31]. This research has moved from understanding the brain state and its general excitability, to exploring seizure frequency over much larger durations [32].

This section will review the state of the art in stimulation therapy, seizure prediction and a combination of the two to form a closed loop responsive seizure abatement. Finally, commercially available devices and clinical results will be presented.

1.2.1 Stimulation Therapy

It is somewhat counterintuitive that electrical stimulation of the brain could suppress seizure activity, rather than provoke it. But just as a pendulum would struggle to swing at resonance amidst random external stimulus being applied so too would the recruitment of synchronised neuronal firing in the presence of electrical stimulation. Of course, the brain doesn't function by analogy and these kinds of conceptual thought experiments may have no bearing on the complex mechanisms that are really at play.

The greatest challenge faced in devising an optimal stimulation therapy in terms of what is stimulated, when and how, stems from the fact that the results are vastly overdetermined; that is, it is difficult to know cause and effect. Different brains, different conditions, surgical variation and stimulation variation. It is complex to piece together a clear picture of why it is effective for some, and not for others.

Experimental studies of electrical stimulation of the brain date back to the late 1884, when Cincinnati surgeon Robert Batholow used some form of electrical stimulation on the cortex and observed contralateral movements [33]. The first use of electrical stimulation as a treatment for epilepsy was not until the early 1950s in the field of psychiatry [34]. It wasn't until 1965 that chronic stimulation of the brain as a treatment for epilepsy was first studied [35, 36].

The emergence of new stimulation technology and the success of deep brain stimulation (DBS) in movement disorders renewed interest in the field over the past three decades with a vast array of stimulation targets explored, as illustrated in Figure 1-2. Of these stimulation sites, the

anterior nucleus of the thalamus (ANT) has shown the most promise. This is not unsurprising given the vast connectivity of the thalamus to multiple regions of the brain. Favourable results from a pilot study involving 15 patients in 2012 [37] along with several smaller studies provided the impetus to conduct a large multicentre trial involving 110 patients [25]. This randomized controlled trial of bilateral stimulation of the anterior nucleus of the thalamus for epilepsy (SANTE) proved successful, ultimately leading to the FDA approval of DBS of the ANT for the treatment of refractory partial seizures [25].

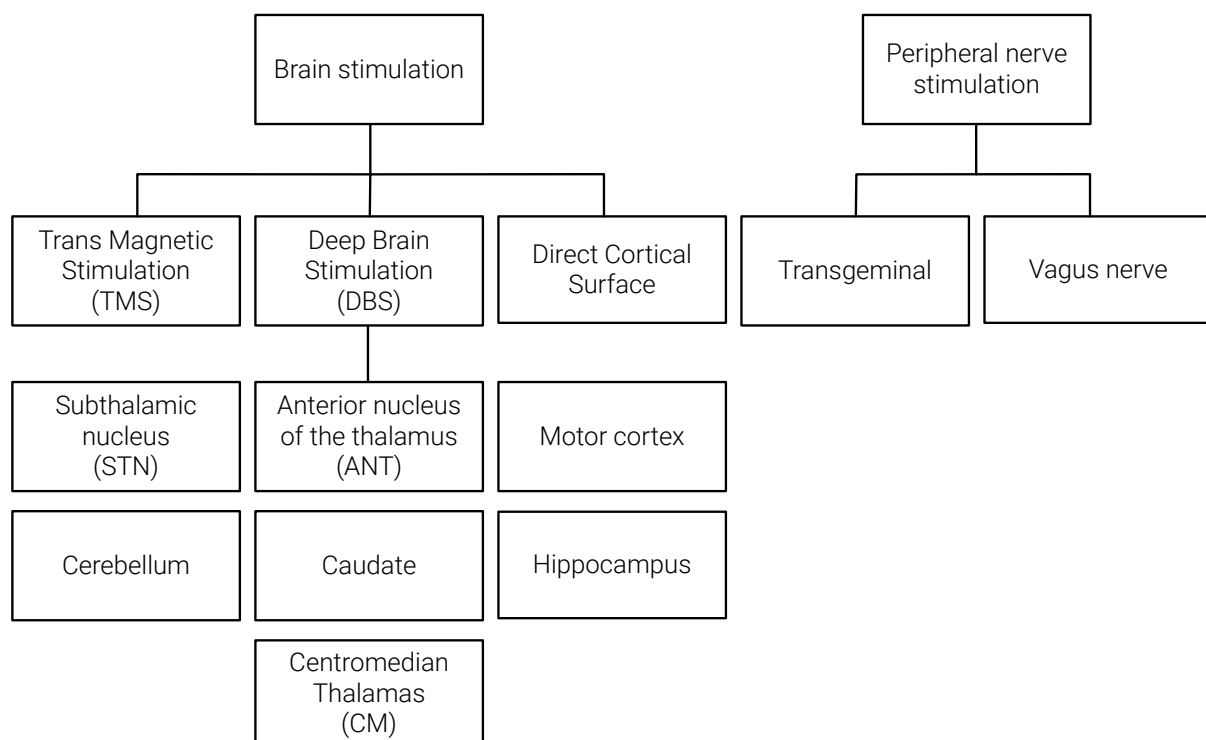


Figure 1-2 Brain and peripheral nerve stimulation sites for the treatment of refractory epilepsy.

More work is required to evaluate strategies to determine patient specific stimulation sites and devise robust stimulation paradigms. Greater targeting on patient-specific bases would benefit from broader access to the brain that would be enabled using devices with higher electrode counts. The brain is understood to be a neural network with such complex and evolving “wiring” that it is difficult to understand where to “plug in” a stimulator to achieve optimal seizure suppression let alone the parameters to stimulate with. The underlying mechanisms of how seizure suppression works via stimulation are not clear and further basic laboratory studies are needed [38]. What works with one patient who suffers one type of epilepsy, may not work with

another – and there are many reasons why. After all, no two brains are equal. There are additional confounding factors that have made assessing stimulation targets and strategies problematic – but mainly, the heterogeneity in the underlying pathology and anatomical location of the abnormalities.

In spite of the complexity of the problem, there are established regions in the brain where stimulation has been shown to have a physiological effect, and well-reasoned arguments to suggest that that artificial periodic activation of these regions could suppress synchronous firing by inhibiting activity thus limiting the ability for a seizure to develop [39]. These are summarised in Table 1-2.

Table 1-2 A comprehensive summary of stimulation site, reasoning for this location and results.

Target	Reasoning	Results	Reference
STN	Popular target for DBS therapy to suppress chemically induced generalised seizures	Studies showed only 50% of patients benefited from this therapy.	[40]
ANT	ANT sits at a key junction point believed to be involved in propagation of seizure	Large scale multi centre study (SANTE) demonstrated 50% improvement in seizure frequency.	[41]
Motor cortex	To eliminate epileptic focus that overlaps the motor cortex.	Refractory motor seizures treated in 6 patients successfully.	[42]
Cerebellum	Outflow inhibitory to most target structures.	No large controlled. Mixed results with for those with generalised seizures .	[43]
Caudate	Basil ganglia argued to have role in inhibition of seizures.	Mixed. Low freq stim (4-8Hz) lowered seizure frequency, higher freq stim (50-100Hz) increased.	[44]
Hippocampus	Structures around hippocampus are very seizure prone.	Numerous studies have shown great promise.	[45]
CM	Influences wide regions of cortex and studies in 1951 showed desynchronisation in response to CM stimulation.	Shown to be beneficial for generalised but not focal.	[46]

Transgeminal	As with vagus nerve this is a large cranial nerve.	Moderate success but with side effects.	[47]
Vagus Nerve	Left vagus nerve connected directly to brain stem.	> 50% reduction of patients with partial or generalised. FDA approved 1997.	[48]
Trans Magnetic Stimulation	Repetitive low frequency pulses could reduce cortical excitability.	Nothing significant and unclear how this would translate to patient therapy.	[49]

1.2.2 Seizure Prediction

Measuring the electrical activity of the brain is performed predominantly using electroencephalography (EEG), a technique first demonstrated on Monkeys in 1875 by British neurophysiologist Richard Caton [50]. In its simplest form, EEG involves placing two electrodes on the scalp and measuring the potential difference between them using a high impedance amplifier with good common mode signal rejection. This method predominantly measures post-synaptic ionic current, which are the result of neural firing, but not the action potential itself. The resultant EEG recording reflects the firing synchronicity of large groups of neurons along with their spatial alignment which form electric fields (voltage gradients) in the brain. To measure any signal at all typically requires 6-10 cm² of synchronous neural firing [51]. However, scalp EEG lacks spatial and temporal resolution due to current dispersion as ion waves move through the dura, skull and scalp to the electrode. In addition to this, artefacts generated by muscle and movement can degrade the signal. Despite its inherent limitations, EEG has proven to be an extremely useful tool for measuring global brain patterns such as epileptiform discharges for diagnostic applications [52].

To achieve high spatiotemporal recordings, electrodes must be placed below the dispersion layers and either sit directly on the cortex or record from electrodes embedded within the brain. In addition to achieving much greater spatial and temporal resolution, embedding electrodes in and around the brain makes both stimulation and recording possible.

As discussed in Section 1.1.2, EEG is a very powerful tool for uncovering the nature of a patient's seizure events. There are also emergent applications that make use of these recordings to help predict a patient's seizures.

Attempts to predict the occurrence of seizures have been underway for well over 30 years now. In 1975, time-series analysis of scalp EEG was used [53] followed by auto-regressive techniques in 1981 [54] with little success. Since then, there has been a shift towards utilising more invasive intracranial EEG techniques for better feature extraction and the use of machine learning to classify them. Recent studies utilising this general framework have shown remarkable detection sensitivity and specificity. A study conducted recently with canine models demonstrated a sensitivity of over 91% [55].

In 2013, Cook et al. [26] published a first-in-human study using a seizure advisor device manufactured by Seattle based company, NeuroVista. In this work, 15 patients were enrolled to undertake a 12-month multicentre trial. The advisory system indicated low, medium and high chance of seizure and was shown to be between 65 to 100% sensitive. A high likelihood indication had to precede a seizure by 5 minutes to be considered a true predictor, whilst the device had to remain in a low state for more than 5 minutes to be classified as a true negative. Ultimately NeuroVista was not successful in commercialising their seizure advisory product, however this pivotal study did demonstrate the huge potential of seizure advisory technology and also provided a large dataset of recording for further work.

Using data captured during these longitudinal studies, Karoly et. al. [13] were able to look deeper into the relationship between interictal spike activity and seizure frequency. In this work, they presented autocorrelation of both spiking and seizure frequency for 15 subjects with delays ranging 0-24 hours and 0-30 days. If, for example, autocorrelation is high at a delay of 1 hour, this would indicate a 1-hour cycle is occurring. In this work, they demonstrated half of the subjects showed an increase in spike rate prior to seizure – and additionally they demonstrated significant autocorrelation for spiking. Since seizure frequency numbers were much lower than spiking, autocorrelation was statistically more difficult to ascertain due to the limited data set. Further to this work, they developed a probabilistic framework for developing and improving patient specific forecasting models [56].

A Bayesian inference that utilises a forecasting model modified by new environmental and brain activity shows great promise in reliably and accurately predicting seizure occurrence. Beyond seizure advisory, this information could be used as a way of titrating stimulation therapy. This brings together the fields of both brain stimulation and seizure prediction to create something akin to the cardiac pacemaker. Attempts towards this approach have been made and will now be discussed.

1.2.3 Responsive Treatment

Open-loop stimulation paradigms have been used in both peripheral nerve stimulation and direct brain stimulation systems with some degree of success as discussed in 1.2.1. However, any electrical stimulation system will elicit broad neuronal activity in the brain and, consequently, modulate normal neural networks in the process of preventing the manifestation of seizures. There are numerous short-term side effects, mostly minor [57], but very little is known about the long term effects of chronic stimulation of the brain. In addition to this, chronic stimulation comes at the cost of increased device power consumption, necessitating either more regular charging or a transcutaneous power supply. As a result, there has been increased interest in closed-loop systems that only deliver stimulation upon detection of seizure onset.

Neuropace has led the way by developing a responsive neurostimulation system (RNS), now approved as an adjunctive therapy for refractory epilepsy [58]. The RNS system continuously monitors electrocorticogram in short 90s windows and delivers brief pulses when abnormal activity is detected. Whilst results indicated on average a near 50% reduction in seizure frequency – it is difficult to ascertain the false positive rate. With the threshold set low it is possible it would be in stimulation mode most of the time in which case it is similar in performance to open loop stimulation [58].

In comparison to recent advances in seizure forecasting and prediction, the algorithm implemented on the RNS system is very limited due to the small 90s window and fixed detection algorithm. A Bayesian predictive model based on fundamental rhythmicity modified by new data from the environment and EEG, could lead the way in developing neural network-based patient-specific algorithms, which hold the promise of delivering exactly the right stimulus exactly when it is needed.

1.2.4 Review of Commercial Devices

Substantial research into the treatment and management of epilepsy either through therapeutic stimulation or brain recording has culminated in the approval of multiple FDA approved implantable devices now on the market.

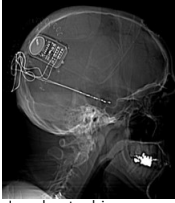
To date, four large randomised trials have been conducted: the first two for Cyberonic's VNS system in 1994 and 1998, the third for Medtronic's DBS stimulator in 2010 and the fourth for the Neuropace (RNS) system in 2011 [59]. It is encouraging to see that benefit is delivered using these systems, but it is also evident that none, either commercially available or in clinical trials, represent optimal solutions. This is indicative of the fact that all three of the devices utilise entirely different stimulation paradigms yet demonstrate similar performance.

Many parallels can be drawn between the current state of epilepsy treatment and diagnosis to that of cardiovascular treatment and diagnosis. First naïve open-loop pacing devices, without monitoring capabilities, were implanted and showed benefit – yet an unacceptable group of individuals were not treated adequately. Sophisticated telemetry was incorporated into the devices to better understand underlying cardiac abnormalities. This led to more effective and patient specific treatment strategies. In fact, these devices were able to uncover intermittent cardiovascular events in people suffering syncope, who had previously been diagnosed with epilepsy [15].

1.3 Neural Interface Architecture

In previous sections of this chapter, the motivation, research and commercialisation of implantable brain recording and stimulation systems has been outlined. This technology has proven its place in the treatment and management of epilepsy. However, as noted previously, the fact that many of the devices all targeting different locations with different stimulation paradigms report similar results, does suggest that an optimised strategy has not been found. This is in part due to the large parameter space, but also due to the architectural limitations of the interface itself. Either through limited electrode count or inability to interface to specific regions, recording duration or stimulation flexibility – many paradigms cannot truly be put to the test without the implantable technology to support it.

Table 1-3 Commercial implants and their clinical trial outcomes.

Manufacturer	Stimulation/ Recording Unit	Placement	Stimulation/ Recording Target	Clinical Trial Outcomes			
				No. of Patients	Seizure Frequency Reduction Group		Authors & Year
					Treatment	Sham	
Medtronic		 Subclavicular region with a lead wire tunnelled through the neck to deep brain electrodes.[60]	Stimulation The Anterior nucleus of thalamus	110	40.4%	14.5%	[41] 2010
NeuroPace		 Implanted in false cavity in skull with lead wires running to both deep brain and subdural surface electrodes.[61]	Stimulation Direct-seizure foci Recording Subdural cortical surface array	191	37.9%	17.3%	[62] 2011
Cyberonics		 Subclavicular region with a leadwire tunnelled through to the neck, where cuff electrodes clamp around the vagus nerve.[63]	Stimulation: Left branch of Vagus nerve	114	25%	6%	[64] 1994
				196	28%	15%	[65] 2001

NeuroVista		 The recording unit is implanted in the subclavicular region. A lead wire is tunneled through to a 16 electrode subdural recording strip.[26]	Recording: Subdural cortical surface array	15 person trial showed seizure estimation sensitivity of 65-100%.	[26] 2013
UNEEG		 Implanted through small incision behind the ear. [66]	Recording: Subdural cortical surface array	8 person trial for 490 days. Showed self-reporting seizure counts differed from objective measured and a circadian distributions confirmed.	[66] 2019

It could also be argued that the research and clinical evaluation of existing technology has led progress towards delivering real benefit rather than theory-based design and development where engineering requirements are clearly defined. Unlike a typical interface to an electronic system, the human body varies from person to person in ways that cannot be captured neatly as a design requirement. Providing great flexibility in the underlying architecture of a neural interface facilitates greater exploration and ultimately greater optimisation in a patient specific way but comes at a cost to complexity and power consumption among other things. In this chapter, the various key architectural types of interface will be outlined including the many engineering considerations necessary to develop safe and effective devices.

1.3.1 Requirements

All implantable neural stimulation and recording devices have two components in common: a hermetically sealed main unit and one or more electrode arrays that interface with the tissue. They have evolved enormously over the past four decades with refinement and improvement of the materials used, device form, stimulation safety, and implantable electronics. This has led to high reliability, stable and biocompatible implants that can be implanted for the lifetime of a patient with very low infection risk and high reliability [67-70].

Broadly speaking, there are two general classes of implantable devices: transcutaneous and battery powered. A transcutaneous device such as the cochlear implant has no implanted power source and derives all its power externally through a transcutaneous inductive link. A battery powered implant, like the heart pacemaker, utilises a battery that is located in the hermitically sealed main unit. The benefit of a battery powered device is that the entire system can be implanted. This is very attractive, but it comes at a cost. The battery has a lifetime and, therefore, must be surgically replaced periodically. The advantage of a transcutaneous system, such as the cochlear implant, is that it can last for the patient's life. Significant research has gone into transcutaneous rechargeable implants, a hybrid of the two strategies. However, the batteries used still have a limited lifetime and the device will have to be surgically replaced, albeit less often [71].

The power and physical size constraints of implantable systems compromise device flexibility. There are three key constraints in the context of a chronic brain monitoring and stimulation system:

No direct power and communication

- Brain signals must be digitised and transmitted internally
- Stimulation must be generated internally

Remote power requirement

- An implanted system must be powered remotely or from an implanted battery. This is not a trivial design challenge.

System flexibility

- Once implanted it is not possible to modify stimulation and recording hardware

The points raised above have implications on the quality and flexibility of the core functionality of the interface. For recording, electrode signals need to be sampled and then transmitted with very low power. Power limitations will make high sampling rates very difficult. Stimulation must be generated internally and will be limited in compliance voltage and stimulation current level, due to power constraints.

1.3.2 Electrode Interface

An electrode simply refers to a conductive biocompatible material exposed to neuronal tissue that, when connected to a high impedance amplifier, is used to “sense” the electrical activity of either a single neuron or a large ensemble of neurons. When a conductor like gold or platinum is placed in direct contact with tissue, ions in the tissue are attracted to electrons in the metal – essentially creating a capacitor. When neurons or an ensemble of neurons fire, the currents are coupled through this capacitor to the amplifier.

Electrodes come in many shapes and sizes, but their principle of operation is the same. To understand the role electrode geometry plays in the reception of neuronal activity it is useful to consider the neuron as a simple point source as shown in Figure 1-3. Since the electric field

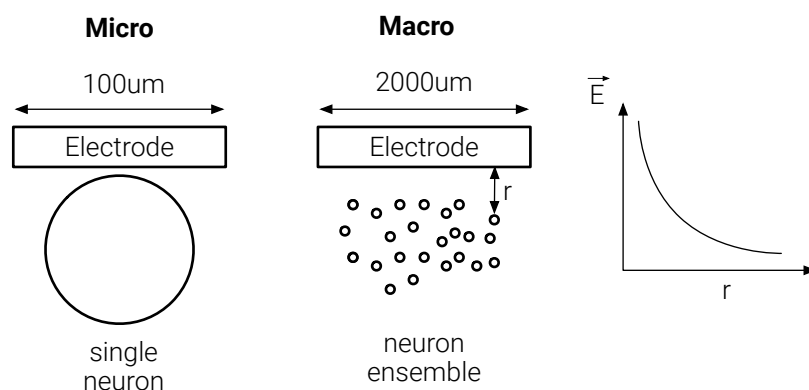
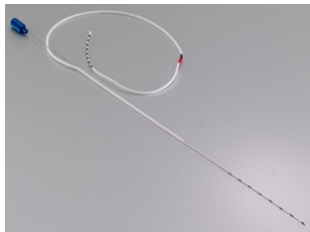
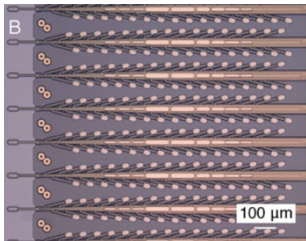
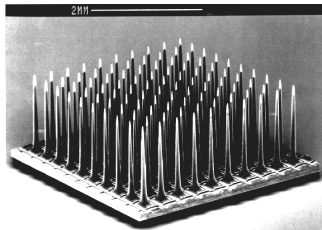
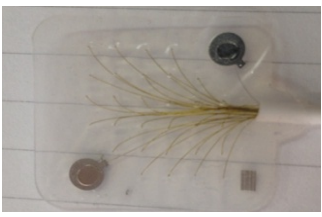


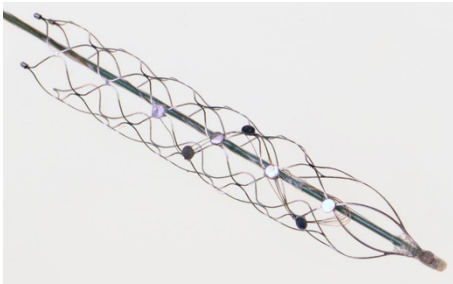
Figure 1-3 Electrode dimension relative to neuronal cell size.

generated by the neuron will reduce inversely proportional to the square of the distance from the electrode – the micro electrode will be overwhelmingly dominated by the closest neurons field and will therefore be sensitive to single neuron firing. In the case of the macro electrode – instead, it will be receptive to many thousands. Recordings of a single neuron is referred to as single cell recording, whilst recording from within the volume of tissue from many thousands of neurons is referred to as the Local Field Potential (LFP). A single electrode sized somewhat between macro and micro is capable of recording both LFP's and spiking potentials simultaneously [72].

In addition to the physical size of the electrodes, there are also several classes of electrode used to access different parts of the brain as shown in Table 1-4. Depth electrodes are tunnelled through the brain to deep underlying structures such as the Hippocampus, Subthalamic Nucleus and the Anterior Nucleus of the Thalamus. Surface electrodes sit under the dura and make direct contact with the surface of the brain. Penetrating electrodes are somewhat of a hybrid between depth and surface electrodes. They typically penetrate millimetres into the surface of the brain. A very novel neurovascular system is actually tunnelled up through veins in the neck in a similar way to the way stents are used in stroke patients.

Table 1-4 Examples of commercially available macro and micro electrodes.

	Macro	Micro
Depth	 [73]	 [74]
Penetrating		 [75]
Surface	 [76]	 [76]

Neurovascular	
---------------	--

[77]

In current practise, clinical applications exclusively use macroelectrodes for their stability and because the goals are often to either achieve broad activation with stimulation or to record LFP's or ECoG from many thousands of neurons. Therapeutic stimulation is, as discussed in Section 1.2.4, an imprecise art that is typically about disturbing a very large number of neurons.

Recent advances in the density of micro electrode interfaces and their integration with electronics have however, made clinical applications of such a devices possible [74]. "Neural dust", a research project based out of University of California, Berkeley, is attempting to make many thousands of untethered stimulation and sensing particles [78]. Elon Musk's formation of Neuralink, which aims to build ultrahigh density brain interfaces, is also an indication that single cell recording is possibly the next frontier [74].

1.3.3 Recording

The characteristic frequency and amplitude of neural signals depends largely on the electrode-tissue interface size and its location. The field potentials that are detected by an electrode can be classified into three distinct signal types as summarised in Table 1-5. Local field potentials (LFP) are relatively large, low frequency signals which can represent the degree of synchronicity of nearby neuronal ensembles. Electrocorticography (ECoG) and LFP recordings are similar in that the origin of the signal is the same - however, ECoG measures surface layer of the cortex confined loosely speaking to two dimensions – whereas the LFP is receptive to all three dimensions and is generally a much larger signal [79]. This makes intuitive sense, if there is a simplistic assumption made that the size of the signal relates to the volume of tissue the electrode is receptive to.

Table 1-5 Signal characteristics of neuronal activity based on location and electrode type [80].

Signal Type	Electrode Type	Placement	Origin	Frequency	Amplitude
Electrocorticography (ECoG)	Macro	Cortical surface	Synchronised postsynaptic potentials	<300Hz	<100uV
Local Field Potential (LFP)	Macro	Brain	Synchronised postsynaptic potentials	<300Hz	<1mV
Single Cell Firing	Micro	Brain	Action potential	0.1-10kHz.	<100uV

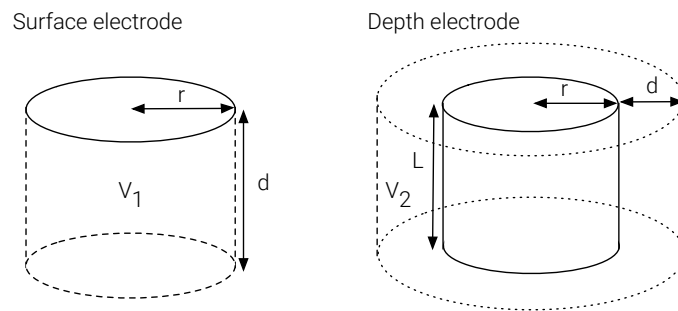


Figure 1-4 Approximate volume of tissue contributing to receptive field.

Consider two electrodes, a surface and a cylindrical depth shown in Figure 1-4, and the volume of tissue they interact with V_1 and V_2 . If the surface area of both a surface electrode and depth electrodes is equal, assuming equal r (for mathematical simplicity), the length of the depth electrode L must be $r/2$. The volumes V_1 and V_2 can then be calculated,

$$\text{Surface electrode:} \quad V_1 = \pi \cdot r^2 \cdot d \quad (1-1)$$

$$\text{Depth electrode:} \quad V_2 = \pi \cdot r^2 \cdot d \cdot \left(1 + \frac{d}{2r}\right) \quad (1-2)$$

So, for the same surface area - V_2 is larger than V_1 and therefore receptive to a larger volume of tissue. Additionally – it is receptive to a wider range of cell orientations creating the ionic wave.

Spiking activity, on the other hand, results in a lower amplitude and higher frequency signal arising from individual action potentials generated in close proximity to the electrode interface. LFP's and ECoG are measured with macro electrodes, whereas spiking activity is measured with micro electrodes – the theory of how this works is outlined in Section 1.3.2.

Clinical implants tend to rely most on macro depth to record LFP for several reasons. First, the electrodes are larger, more stable and less sensitive to migration. Secondly, the LFP is a lower frequency signal that is lower in power to capture and transmit. Finally, synchronous firing activity is often the measurement of interest – and the LFP intrinsically averages activity rather than the need to explicitly compute.

1.3.4 Stimulation

Electrical stimulation of tissue is generally achieved using charge balanced biphasic current pulses, which is shown in Figure 1-5. Since tissue is capacitive in nature, charge imbalance can lead to charge accumulation on the electrodes and hence DC voltages, which have been shown to be unsafe over time. This is discussed further in 1.3.5.

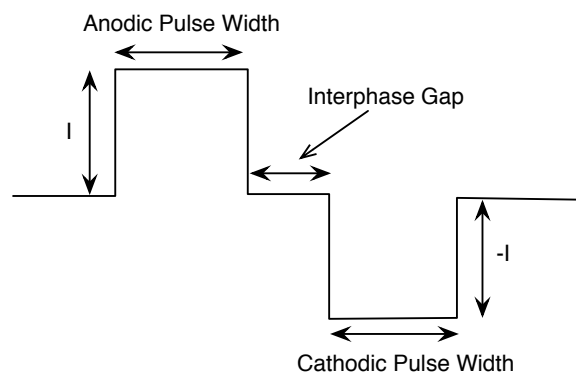


Figure 1-5 A typical biphasic constant current waveform.

There are two general types of stimulation that are of interest,

- I. **Super-threshold stimuli.** Used in a functional brain mapping and therapeutic stimulation.

- II. **Sub-threshold stimuli.** Used to gain insight into neural dynamics, or general tissue properties without eliciting a perceivable response. Examples include electrode impedance measurement and excitability probing [81].

Table 1-6 Typical stimulation parameters for subthreshold and suprathreshold stimulation via macro electrodes [82].

Subthreshold Stimuli	Min	Max
Phase width (us)	10	100
Amplitude (uA)	10	100
Suprathreshold Stimuli		
Phase width (us)	100	2000
Amplitude (uA)	100	10000

The stimulation signal is a current mode signal. That is, current is being controlled and voltage is resultant due to tissue impedance. In normal operation, the stimulator terminal voltage between the source and sink will depend largely on the current delivered and the impedance of the tissue. A convention used to define tissue impedance is to find the peak voltage reached at the end of the first current phase delivery and divide this by the current delivered. Of course, this value completely depends on the phase width and amplitude. However, this convention is still a useful way of describing the peak voltage for which the stimulator needs to withstand. This is referred to as the stimulator's compliance voltage. One possible approach to limit compliance voltage requirements of a stimulator is to reduce the current and extend the pulse width. In this way, the same quantity of charge is delivered but with a lower voltage requirement [83].

1.3.5 Tissue safety

Extensive safety studies into safe electrical stimulation of neural tissue have been conducted over the past several decades. The gold standard of electrical stimulation of tissue utilises charge balanced biphasic constant current pulses and shown in Figure 1-6 [84]. In this paradigm, a fixed quantity of charge is delivered to the tissue activating or exciting neurons in the first phase and the second phase is used to recover this charge such that close to net zero

charge remains on the tissue interface. When an electrical current is delivered to tissue, it induces ionic current flow, and can be approximated as a leaky capacitor [85]. Without charge recovery, a DC voltage will accumulate at the interface due to this capacitive nature. This can cause damage to the underlying tissue over time [84]. Of concern to the delivery of biphasic stimulation pulses, absolute charge and charge density limits must be observed and accumulated DC voltages at the interface must be negligible.

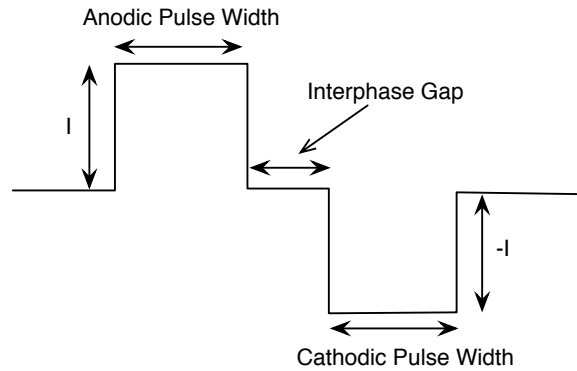


Figure 1-6 A typical biphasic constant current pulse

The Shannon equation was an important contribution to the field, as it unified disparate observations of safe charge density limits into a single equation relating current, pulse duration and electrode surface area [86],

$$I.T = \sqrt{A.10^k}, \quad \text{Eq 1-3}$$

where I is the stimulation current, T is the pulse width, A is the electrode area and k is a constant typically chosen to be 1.85, but can be modified taking into account duration of exposure, duty cycle, stimulation frequency and pulse duration.

Further to this, in-vivo studies conducted by Shepherd et al. demonstrated charge imbalances greater than 100nA to be unsafe for chronic stimulation [84]. It is noted, however, that even though this is an often-cited measure it is actually very specific to the stimulation paradigm of the experiment, measurement apparatus and the electrode location and type. This is not simply because of differences in tissues, but the leakage of the measurement apparatus for different stimulation parameters. Nevertheless, it has proven to be a robust benchmark in which to constrain stimulator design [84]

The actual charge and charge density limits are not absolute and depend largely on the region of stimulation and the type and geometry of the electrodes. To ensure zero net DC flow, capacitive coupling, electrode shorting, and precise balancing of biphasic pulses can be employed. The physical size constraints of implantable devices often limit the use of DC blocking capacitors. Active charge balancing strategies or high precision matching techniques can be used to overcome this.

1.3.6 Power

As previously discussed, power can either be derived internally through a battery or externally via induction through what is often referred to as a transcutaneous link. Cardiac pacemakers typically use a battery, whereas cochlear implants use a transcutaneous link. The fundamental reasoning for this comes down to power.

In the context of brain recording and stimulation, the higher the number of channels – the higher the power consumption. Power consumption will depend on: channel count, stimulation parameters and recording parameters.

Whilst stimulation if titrated well can remain off most of the time, recording will need to happen continuously for the purpose of seizure prediction. Recently, remarkable progress has been made in reducing the power consumption and size of neural recording devices for combined LFP and spike detection [72].

1.4 Conclusions

In this chapter, a broad introduction into epilepsy aetiology, diagnosis and treatment was provided. In spite of all the efforts seen in recent decades, there has been relatively modest progress in treating epilepsy [87]. While AEDs continue to dominate treatment regimens, as many as 30% of people with epilepsy do not receive sufficient seizure reduction and are said to suffer refractory epilepsy [88].

Surgical intervention became a viable option with the use of advanced imaging technologies, most notably MRI, which recently superseded CT scanning. MRI enabled the pathological basis of seizure activity to be understood in most patients [89]. This technology made it possible for Neurologists and Neurosurgeons to localise seizure foci. The use of ECoG and brain stimulation has also been a powerful tool in surgical planning by further homing in on the foci and understanding surrounding tissue function that can and cannot be removed. Finally, radionuclide imaging, such as Positron Emission Tomography (PET) and Single Photon Emission Computed Tomography (SPECT), enhanced localisation efforts.

While the risks of surgical intervention have been greatly reduced with advances in neural imaging and electrical recording technology discussed above, they are not completely mitigated, and the prospect of such a surgery remains daunting for many patients. Concurrently to these efforts, the use of electrical stimulation for modulation of brain activity and therapy has seen renewed interest since its origins in the early 1950's. Though still not well understood, stimulation is aimed at either inhibiting neuronal excitability in targeted regions of the brain or preventing the synchronisation of many neurons, which leads to seizure spread. A variety of targets have been explored, as discussed in Section 1.2.1, with varying results. The first commercially available devices stimulated the Vagus nerve, which innervates deep brain structures, and showed to be of benefit to some patients. Direct stimulation of the brain has demonstrated proven benefit, in particular when delivered to the ANT region.

Practical clinical applications of brain monitoring have recently emerged. That is, if you can predict the occurrence of a seizure minutes or hours before it happens, then you can help a patient to get out of harm's way and reduce the anxiety they often live with. It also helps in easing anxiety associated with uncertainty of seizure occurrence. In recent years, this field has matured to the notion of Seizure forecasting – akin to a weather forecast for the day – aimed at helping the patient better manage their condition. A combination of both approaches is ideal. Chronic brain monitoring also holds the promise of providing more accurate and objective information for neurologists to assess the benefit of various AEDs.

The requirements for optimal recording and stimulation are not clear. Increase the number of electrodes and face serious engineering scalability issues with no guarantee of any

improvement. Stick with the same hardware and there is a chance important information will be lost.

There appears to be somewhat of a bifurcation in the approach to epilepsy seizure management. One based on long term cycles emerging from seizure rhythms or inferred through spiking activity and its possible relationship to seizure activity. The other is ultra-high-density brain interfaces that can understand brain state beyond what has so far been possible. A combination of both approaches, whereby the chronic rhythms form a Bayesian estimate modified by new information, may prove the most powerful prediction method.

To understand the effect of a given treatment strategy on the activity of the brain, we must measure the brain. Most importantly, we must measure the same brain for extended periods of time. Acute measurement is plagued with confounding factors that make drawing meaningful conclusions extremely difficult, if not impossible. Observing one patient over a long period using intracranial EEG would be of enormous significance to the field of epilepsy treatment and diagnosis. To this end, a chronic and highly flexible brain monitoring/stimulation system is needed.

One option that provides flexibility and leverages the proven performance of existing implants is the modification of existing implantable devices. This largely mitigates biocompatibility risks and greatly reduces the regulatory burden so long as the device is not substantially changed. To seamlessly increase electrode count of a commercial stimulator requires the custom design of an integrated circuit.

2 Modification of commercial implants

The motivation for developing a flexible brain interface has been established and some of the basic approaches discussed in the context of epilepsy management. While it is completely feasible to develop an integrated circuit for brain stimulation and recording applications, the purpose of this work is to look at ways of expanding the capability of already approved devices. The regulatory barriers to entry for implantable systems are extensive since issues of biocompatibility and stability necessitate extensive preclinical and clinical trials. These are not just issues of device engineering, but rather how to develop something that can safely be implanted.

Expansion of a commercial stimulator, such as the cochlear implant, to increase the number of electrodes without any changes to the wire feedthrough out of the hermetically sealed package will be explored. By using modulated biphasic stimulation pulses to both power and configure a cross point switch a flexibility to trade-off stimulation rate with access to greater numbers of electrodes can be achieved.

In this chapter, the architecture for such an expansion chip will be explored along with considerations relating to switching, harvesting and communication. This discussion is in preparation for Chapter 3, which will discuss in detail one embodiment of such a system.

2.1 Architecture

The expansion of an existing implant to increase the number of recording and stimulation channels can be achieved in one of two ways, as shown in Figure 2-1. Either the multiplexing chip is placed within the array or it is placed within the Implants hermetically sealed can.

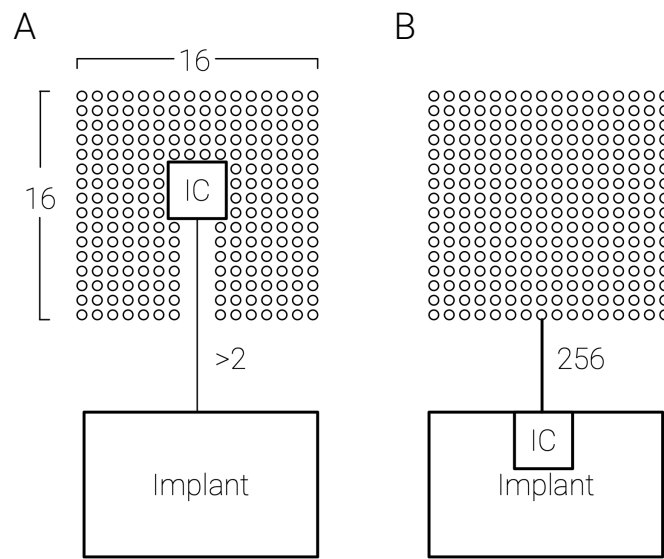


Figure 2-1 The IC location shown in A embedded into the electrode array and in B contained within the implants hermtically sealed can.

Both approaches have merit. Placing the IC within the array will mean that a multitude of such arrays could be scattered throughout the brain. The formation of pseudo macro arrays using the grouping of many smaller micro electrodes is achievable. This would enable macro electrodes and recording for LFP whilst targeted single channel cell recording is still possible as shown in Figure 2-2 [90].

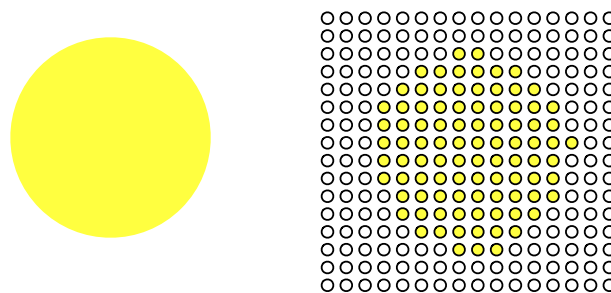


Figure 2-2 An electrode shown in yellow on the left being approximated by 16 x 16 electrode array on the right.

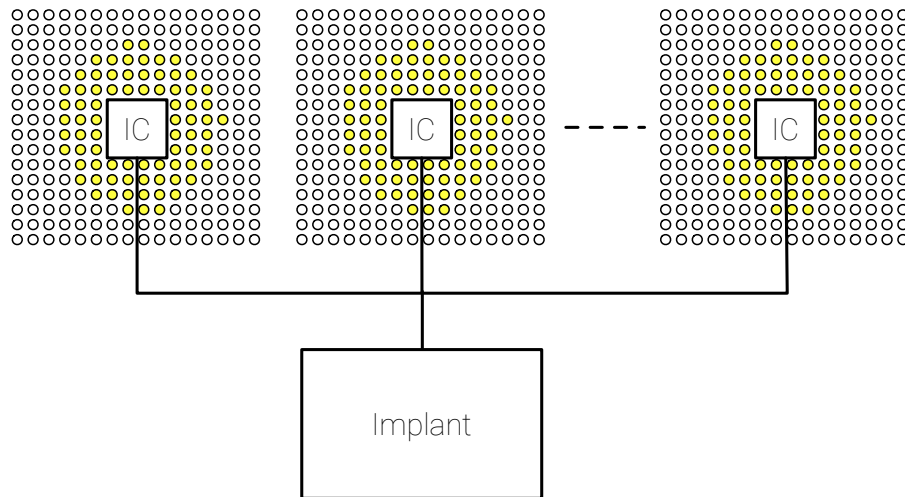


Figure 2-3 Multiple 16x16 arrays configured to synthesize macro electrodes.

Alternatively, placing the IC within the implant will mean no modification is required to proven high density arrays but presents serious challenges in the design of the feedthrough and the density of the wire bundle as will be discussed further in Section 2.2.

Assuming that the chip is instead integrated into a large electrode array with mechanical and encapsulation issues resolved, there remains a serious concern regarding power and communication to such an array in a safe manner so as not to expose tissue to DC voltages [84]. This was discussed in Section 1.3.5. One solution to this challenge is the use of biphasic stimulation lines for power and communication to such an array. That is, using safe subthreshold stimulation pulses that simultaneously power the chip, and via modulation of the stimulation pulses encode information required to set the electrode array. Further to this, if the system could be designed in such a way as to dynamically power up on any two input pins, a high redundancy interface would mitigate risk of wire breakage.

While such an approach complicates the Integrated Circuit (IC) design, it comes with a number of important benefits that are summarised as

1. Safe power and communication to implant array.
2. Redundancy to bypass broken wires.
3. Access to large parts of the brain where the implant stimulation rate can be traded for electrode count.

Considerations will now be outlined for such an approach.

2.2 Expanding electrode count

With a limited number of electrodes in commercially available implants, access to multiple regions of the brain is also limited [70], and they are not able to interface with high density micro electrode arrays used to explore individual neuron firing. Typically, commercial implants include only a few channels. The cochlear implant contains the largest channel count with over 20. Electrode count is, in part, fundamentally limited by the mechanical complexity of feeding each wire from within the hermetically sealed enclosure out to the electrodes that interact with the tissue [91].

Multiplexing has proven to be successful in reducing electronic channel count whilst providing access to the required number of electrodes. This includes work by Viventi et al. [92], who developed flexible and foldable arrays containing electrodes that could be uniquely addressed. By integrating transistors within the array of electrodes, large high-density arrays could be interfaced to implants with far fewer wires. It was a novel breakthrough in both concept and manufacturing process design that made meaningful progress towards high-density recording arrays.

The next question is how to record and stimulate vast arrays. One interesting observation is that simultaneous stimulation and recording from vast regions of the brain concurrently may not be necessary. Instead – optimal stimulation and recording locations could be selected. In the first instance by a clinician, and in subsequently algorithmically by subjective and objective patient response. By extension of this artificial neural networks could one day be used to achieve this learning process automatically over time.

2.2.1 Crosspoint Switch

A cross point switch is an array of switches that enables any set of inputs to connect with any set of outputs, noting that the inputs and outputs are often bidirectional and naming is arbitrary. To increase the number of electrodes of a commercial stimulator without the addition of stimulation channels, a cross point can be used. Such a system can be made arbitrarily large. If M is the number of inputs and N is the number of outputs, the Crosspoint switch will require $M \times N$ individual switch cells. Figure 2-4 illustrates a 6 x 64 Crosspoint switch, which will

necessitate 384 switch cells. Addressing such an array will, in turn, require a minimum of 384 separate control lines within the chip if complete flexibility in configurability is required.

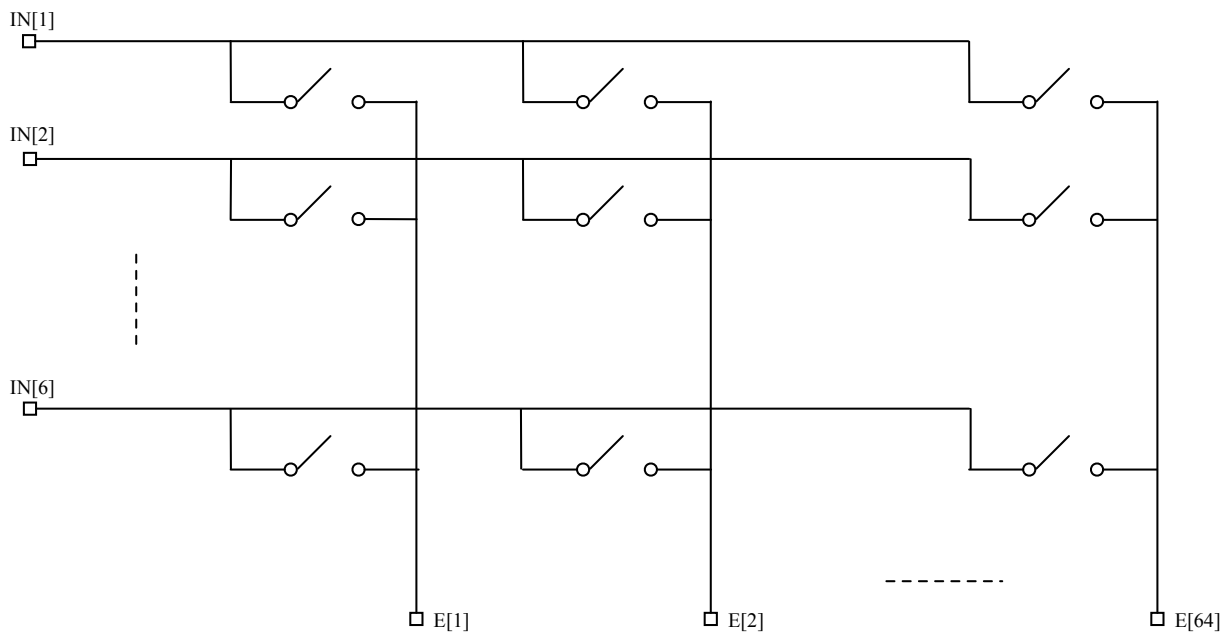


Figure 2-4 Cross point switch comprising an array of addressable switches that enable connection of any input to any output.

It is tempting to think that the number of programming bits and control lines can be reduced by addressing in rows and columns, but as illustrated in Figure 2-5 where desired switches are [1,1] and [3,3], there are unintended connections at [1,3] and [3,1]. So, short of anything more sophisticated happening at each cell to prevent this, each cell must all be addressed uniquely.

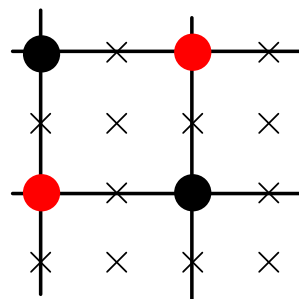


Figure 2-5 Cells (1,1) and (3,3) being addressed by row and columns an causing inadvertent selection of (3,1) and (1,3) shown in red.

2.2.2 Stimulation considerations

Figure 2-6 demonstrates how the 6 x 64 element cross-point switch can be configured to stimulate any two output electrodes from any two inputs. In this example, cells (1,1) and (6,2) are enabled and stimulation between IN[1] and IN[6] is applied to electrodes E[1] and E[2]. Of course, any configuration is possible, making the platform highly flexible to explore the most effective stimulation therapy.

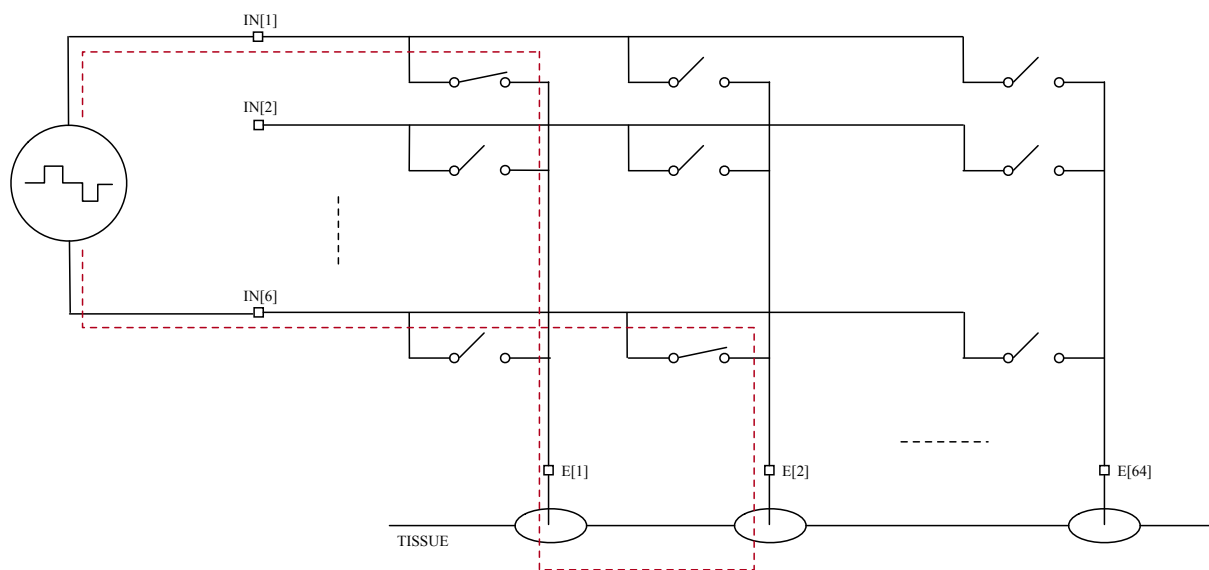


Figure 2-6 Crosspoint switch configured to stimulate through E[1] and E[2] via IN[1] and IN[6].

The switch cells must be able to pass or block the current flow in both directions. Switches of this type are known as bilateral switches [93]. If this were not the case, switches in an off position would still be able to conduct return current. This is often referred to as common ground stimulation, whereby there is a single electrode activate while the rest return [94]. This will result in higher density charge around the stimulating electrode and is useful for stimulation directly beneath the electrode. Alternatively, stimulation between electrodes can be achieved using what is known as bipolar stimulation [94]. It is in this configuration that the active and return electrodes both elicit stimulation to surrounding cells and importantly such a stimulation paradigm relies on bilateral switches.

In addition to this, the switches must tolerate instantaneous phase reversal, which can create negative and above rail voltage transients. To illustrate this mechanism, it is instructive to consider the tissue as if it were a purely capacitive load as shown in Figure 2-7, which shows a circuit comprising a biphasic current stimulator connected through to two electrodes that connect to an artificial tissue model consisting of a single capacitor. The first stimulation pulse will charge the capacitor resulting in a linear ramp since charge is proportional to current and a capacitor simply integrates charge. On the second phase, the charge is still held on the capacitor, but the positive terminal is pushed to 0V relative to the stimulators supply. This assumes the implant makes use of single switched current source rather than a mid-supply current source [70, 95]. Most commercial implantable stimulators to the authors knowledge make use of single supply current source switching to generate efficient high compliance voltage biphasic stimulation pulses.

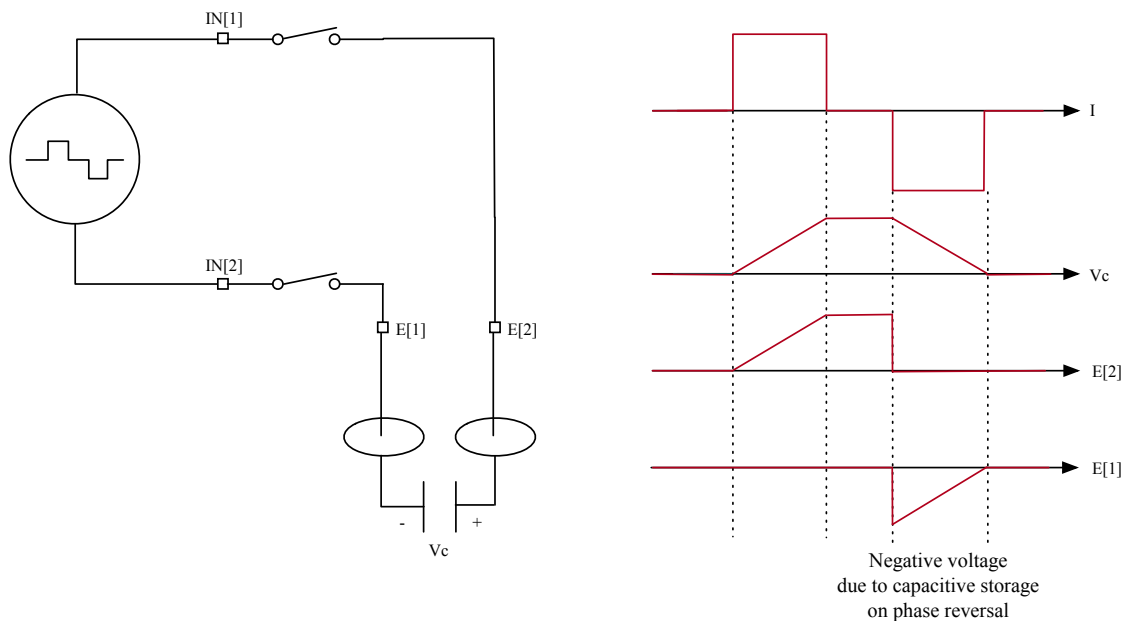


Figure 2-7 Negative terminal voltage due to phase reversal of capacitive load.

As a result, in the first phase, the IN[2] is effectively connected to the system ground of the stimulator, meaning that E[1] will be at 0V during the first phase. In the second phase, E[2] will be connected to 0V. Since the capacitor is charged to +Vc with respect to E[1], the actual voltage of E[1] will be forced to -Vc.

A real tissue load is not simply a capacitor. However, it will have a component of capacitance and hence charge storage that may not fully dissipate in the Interphase Gap.

In summary, it is important to note through the example provided that negative terminal voltages are likely on phase reversal, and the switch cells must be designed to be able to handle this.

2.2.3 Recording considerations

In much the same way as stimulation can be routed to any two electrodes, neural signals can be routed back to the stimulator. Many stimulators, including those that are marketed purely for stimulation therapy, also include neural amplifiers, albeit with limited capability [96].

Figure 2-8 illustrates the switch array configured in such a way to record from electrodes 1 and 2 via the input lines 1 and 2. Since the array is static and close to the recording site – the interference from external signals will be low so long as the electrodes make good low impedance connection with the underlying tissue. If the electrode is floating, noise will be an issue as the electrode will simply act as an antenna to all surrounding electromagnetic interference. Putting external noise contributions aside, there is an intrinsic noise that needs to be considered.

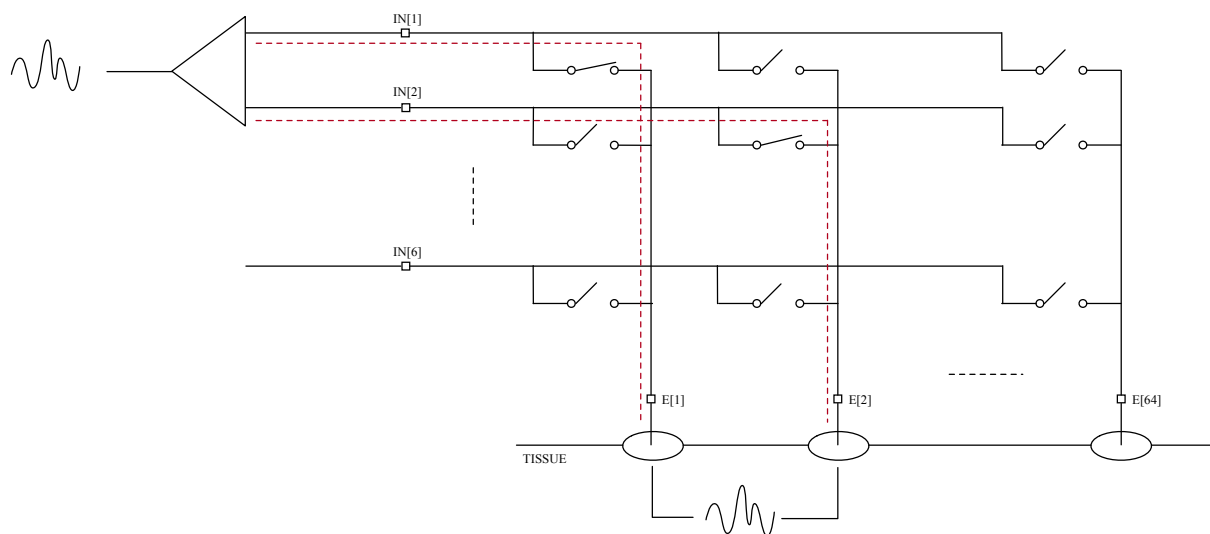


Figure 2-8 Crosspoint switch configured to record through E[1] and E[2] via IN[1] and IN[2].

It can be assumed that the switch cell will be implemented using a Field Effect Transistor (FET), the basic building block of CMOS IC technology. FETs can be used to create low impedance switches, where the on resistance is proportional to the size of the device. Unfortunately, all FETS suffer from an intrinsic noise known as flicker or 1/f noise. This results from charge carriers moving at the interface of the gate oxide and silicon substrate getting trapped and released at some later time [97]. Without discussing this in more detail, it is a well understood phenomenon that is inherent to all FETS.

The noise voltage is given by

$$\text{Noise Voltage} \propto \frac{1}{WL} \cdot \frac{1}{f}, \quad (2-1)$$

where W and L are the width and length of the transistor and f is the frequency. What this equation shows is that flicker noise is far more dominant at lower frequencies and can be reduced by increasing the size of the transistor.

Generally, PMOS devices exhibit less flicker noise than NMOS due to the way they are physically constructed, since the charge carriers transfer in a buried channel some distance from the oxide-silicon interface [97].

One of the most effective methods of mitigation is with the use of a chopper stabiliser circuit commonly used in Op Amps to eliminate offset voltage [98]. This, however, is beyond the scope of this work and it is accepted that some degree of flicker noise will occur but that it can be mitigated with the use of large PMOS devices.

As discussed in Section 1.3.3, the signals of interest are electrocorticography (ECoG), local field potentials (LFP's) and spike waves. Extracellular action potentials have energy focused around 1kHz and are often detected rather than fully quantised and, as such, flicker noise presents less of a problem with adequate filtering. ECoG is smallest in amplitude with meaningful energy in at low frequency. For this reason, it is anticipated that there will be a degradation in the low frequency detection of LFPs. That said, such synchronous activity would have higher frequency

components for which the flicker noise will have less of an effect. In this instance, it is not a case of elimination but rather maximising the device size and using PMOS devices to limit as best as possible the $1/f$ noise contribution.

2.3 Harvesting energy from biphasic current stimulation

As discussed in Section 2.1, it is a practical necessity to power the switch IC using biphasic pulses so as to eliminate the need for DC power lines, which would present an unreasonable risk of tissue damage. In this section, we explore the key principles of how biphasic stimulation pulses can be harvested and stored on chip to create the chips voltage supply.

2.3.1 Full wave rectification

The conversion of alternating current to a DC voltage, be it the 50Hz mains power used in residential power distribution or in this case a biphasic stimulation pulses, is performed using a process called rectification. Rectification utilises diodes to “steer” current in one direction through to a capacitor, which in turn integrates this current and charges. This can be achieved with both current mode and voltage mode signals. Of course, both signals have an associated current and voltage but a current mode signal just refers to one in which the current is being controlled.

The process of rectification in the context of biphasic power harvesting can be understood in three distinct phases as illustrated in Figure 2-9 where the three phases are denoted I, II, and III. Phase I shows the state where no current is being injected. Under these conditions, charge stored on the capacitor cannot flow back through the diodes D2 and D4 since they are both reverse biased. Phase II represents what is typically referred to as the anodic phase whereby the stimulators active electrode is a positive current source. Under these conditions, D2 and D3 will conduct whereas D4 and D1 will remain reverse biased. Phase III represents the cathodic phase whereby the active electrode is instead sinking current. Under these conditions, D4 and D1 become forward biased and conduct whereas D2 and D3 are reverse biased. This cycle repeats at the stimulation rate.

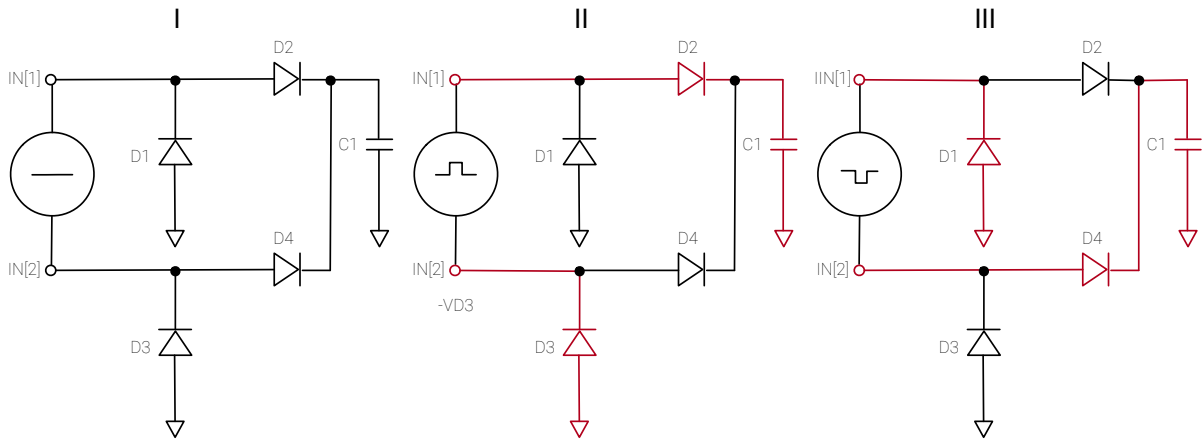


Figure 2-9 Three phases of an ideal full wave rectifier.

There are two key considerations in the context of full wave rectification. The first relates to the forward voltage drop of the diodes and the effect this has on the maximum achievable stored voltage. The second relates to what is known as the droop voltage, which refers to the voltage ripple appearing on the capacitor as it discharges in Phase I. These will now be briefly explored.

The voltage that results from each current pulse can be expressed as

$$\Delta V = \frac{Q}{C} \quad (2-2)$$

$$\Delta V = \frac{PW \cdot i_{amp}}{C}, \quad (2-3)$$

where ΔV is the voltage change on the capacitor, PW is the width of the pulse, i_{amp} is the amplitude of current and C is the capacitance of the storage capacitor. Assuming a storage capacitor of 100nF, pulse width of 100 us, and amplitude of 1 mA, the voltage step would be

$$\Delta V_{cap} = 1 \text{ V}. \quad (2-4)$$

The capacitor will not continue to charge indefinitely. A real biphasic current stimulator has what is called a compliance voltage, which is the maximum voltage at which it can still control current. In addition to this, the diodes need to be forward biased in order to turn on and charge.

All real diodes or diode-like devices will have a non-zero switch on voltage with respect to the input and output lines called the forward bias voltage. So, the maximum capacitor voltage will be

$$V_{C,max}=V_{Comp}-2V_D, \quad (2-5)$$

where $V_{C,max}$ is the maximum voltage the storage capacitor will reach, V_{comp} is the compliance voltage of the stimulator and V_D is the diode forward voltage. A typical diode has a forward voltage of around 0.6 V. Therefore, the maximum voltage will be approximately 1.2 V lower than the compliance voltage of the stimulator if ideal diodes were assumed.

The following consequences need to therefore be considered:

1. If IN[2] is connected to the return of the stimulator and the substrate of the chip is also connected to the Ground, the anodic phase will lead to a terminal voltage of -0.6V.
2. Since the maximum voltage the internal capacitor will charge to $2V_D$ lower than the compliance voltage, the switch array (which will be powered by the cap) will need to be able to withstand voltage beyond $+2V_D$.

Section 3.2.1 will discuss methods that can be used to overcome these issues.

The second key consideration is the droop voltage that occurs in the off time. During the interphase gap and interstimulus interval, denoted in Figure 2-9 by phase I, the circuitry within the IC will need to derive all its power directly from the capacitor. Just as with charging, this will lead to a discharging given by

$$\Delta V_C = \frac{PW_{off} \cdot i_{dis}}{C}, \quad (2-6)$$

where ΔV_C is the voltage change on the capacitor, PW_{off} is the width of the pulse, i_{dis} is the amplitude of current and C is the capacitance of the storage capacitor.

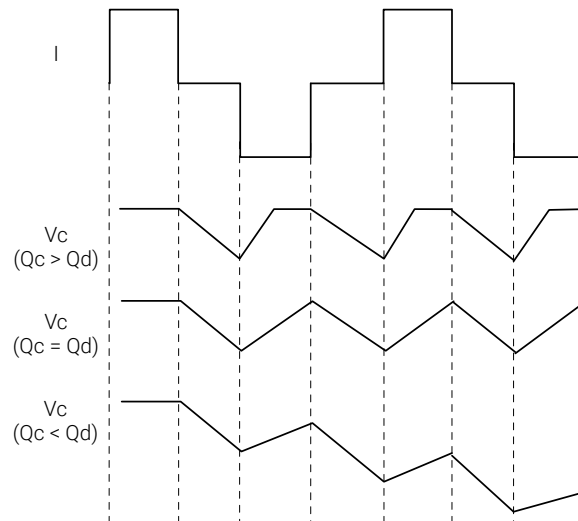


Figure 2-10 Supply droop during stimulation off periods for different quiescent consumption.

The discharge phase will result in fluctuations in supply known as ripple, which can have an impact on sensitive current sources and circuits. This can be smoothed by either increasing the size of the capacitor (though this is limited by the chip area), reducing off time or reducing quiescent current. In a practical sense, ripple can be most meaningfully addressed by reducing the Inter-Stimulus Interval (ISI) and the Inter-Phase Gap (IPG) as it is not a charging problem, but rather a discharging problem.

Finally, a regulator that takes the harvested energy and creates a regulated voltage at a much lower voltage will virtually eliminate this slow ripple so long as there is sufficient head room (difference in supply vs. regulated output voltage) for which it can regulate.

Key considerations in the design of the harvesting include:

- Minimise the ISI and the IPG
- Maximise the on-chip capacitor
- Limit the quiescent power consumption to a minimum
- Keep sensitive circuits on the low voltage regulated supply where possible

2.3.2 Pseudo-ground

As eluded to in Section 2.3.1, the ground of the IC substrate will not be derived from any fixed line but rather determined by the stimulation lines in an alternating fashion. During a charge pulse, the substrate will be V_D below the ground of the stimulator, and during the IPG and the ISI since both diodes D1 and D3 will not be active and the chip will in essence be floating (excluding leakage and parasitic components that will couple the circuit in some way).

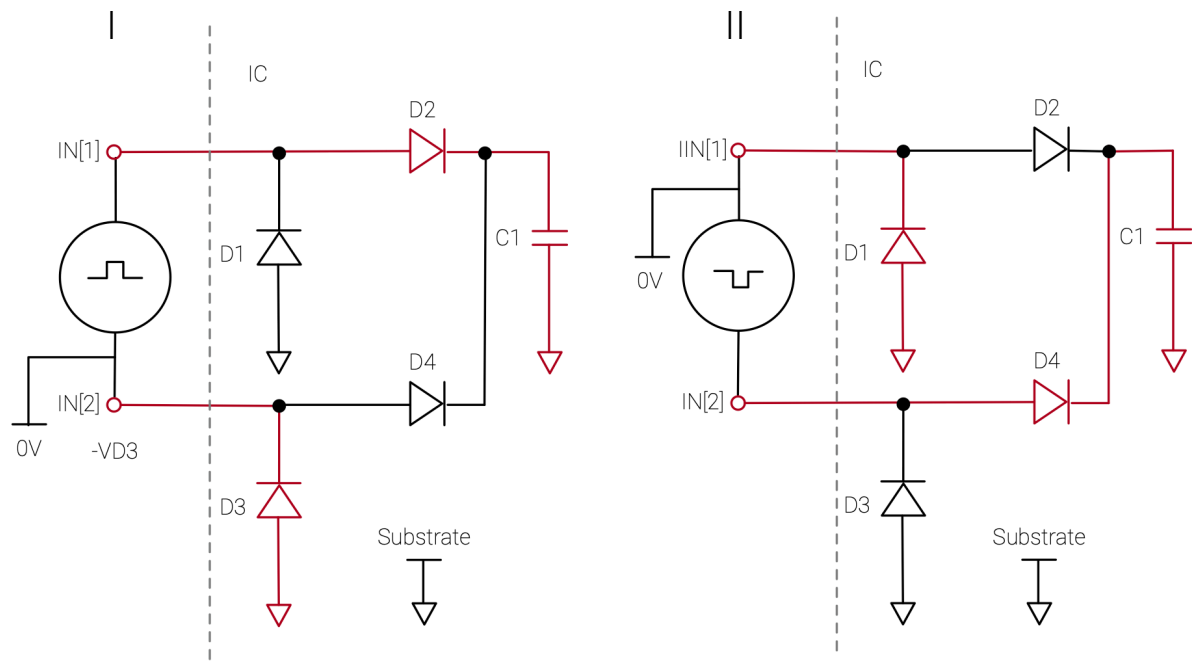


Figure 2-11 The two charging phases I and II and the relationship between stimulator ground and IC ground.

Now, if we assume that the chip is in a fully charged state with no leakage and that the pins used for this are IN[1] and IN[2] and that stimulation is delivered through IN[2] and IN [3] and we consider that the tissue being stimulated is again a capacitor, we arrive the schematic shown in Figure 2-12.

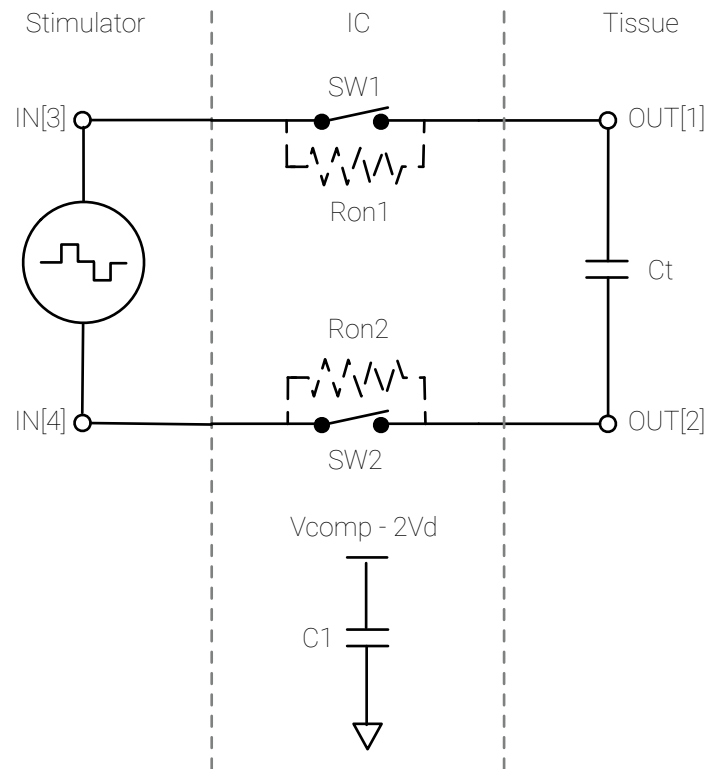


Figure 2-12 Two switch cells turned on with stimulation current looped through both via tissue load modelled by a capacitor.

Now, if we just consider the anodic phase of stimulation, we can see that terminal voltages will not be defined on-chip explicitly. There is only a relationship between the terminals relative to each other since the “switches” are floating. In other words, the actual ground of the capacitor could be something as large as 1000 V below that of the stimulator ground. This is a problem when it comes to controlling the switch state since the gate voltage is relative to the terminals of the transistor.

This is a good place to now introduce the concept of pin casting, where the issue of floating ground will be further explored in the context of the full circuit.

2.3.3 Pin redundancy

In the architectural overview provided in Section 2.1, motivation for pin redundancy was briefly mentioned. Essentially, if any two input pins can be used for power and communication, a wire

breakage can easily be bypassed. To understand how such a system could work, it is useful to view both the IC with both power harvesting and switch array included, as shown in Figure 2-13. Without going into the detail yet of how the switches are configured, it is clear to see from symmetry that each pin would need to have precisely the same configuration and that they would all include a diode connection to the substrate.

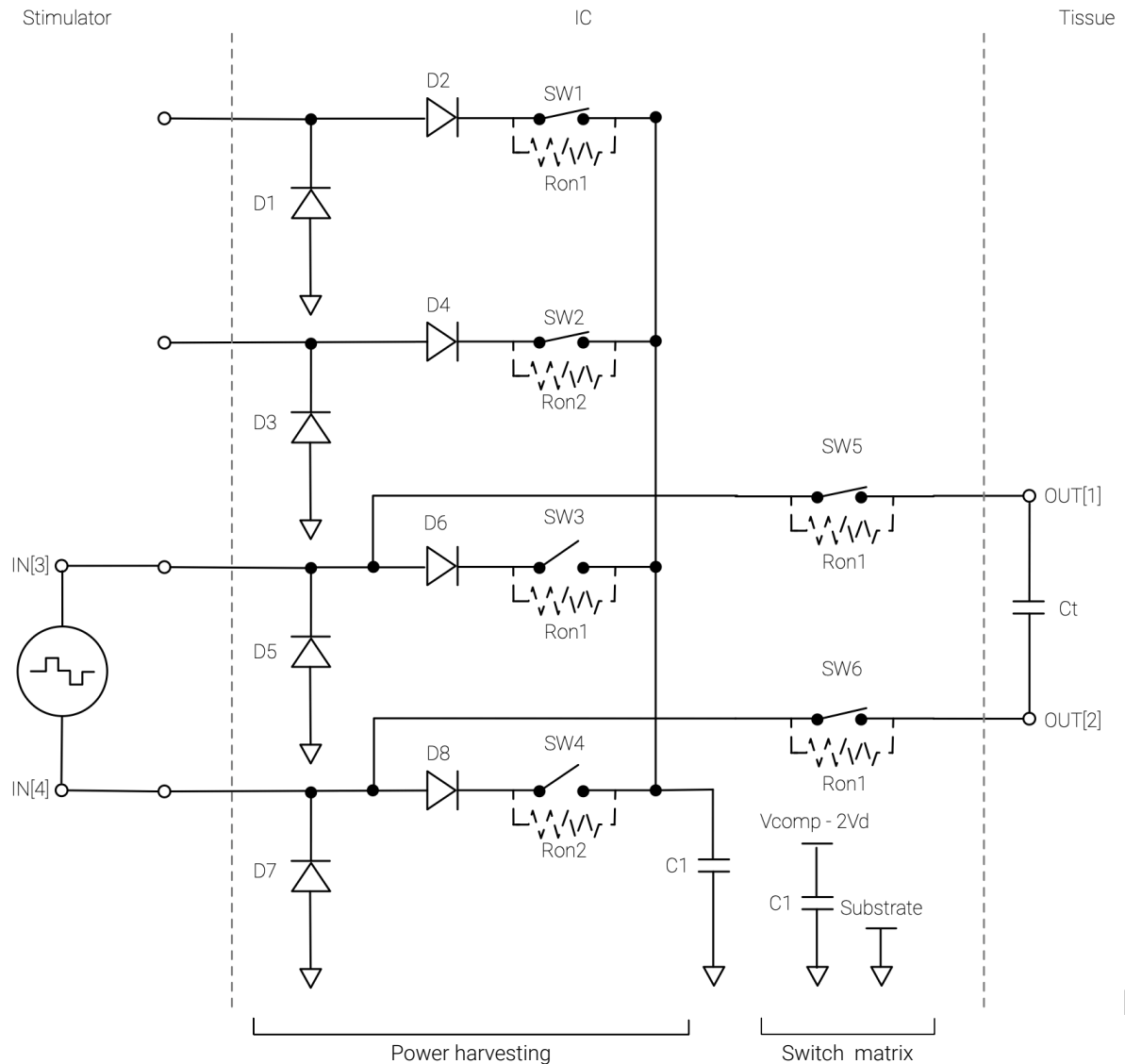


Figure 2-13 A simplified model of the IC showing interactions between power harvesting and switch array.

Therefore, returning to the question around floating raised in Section 2.3.2, it is clear to see that, once the IC is configured in such a way as to allow power to be derived from any pin, there will be by necessity a diode on each, D1, D3, D5 and D7. When the stimulator is off, the chip will float.

With power and communication lines established, how will it gate stimulation pulses? The sinking side of the stimulator will be set to 0V and, via reverse leakage of the input diodes, this will be approximately equal to the substrate. That is, as shown in Figure 2-14, the nodal voltage X must lie somewhere between 0V presented at IN[4] and whatever the positive stimulation voltage is at IN[3]; let's say for example 10V. Since D5 is reverse biased while D7 is forward biased, the equivalent resistance of D5 will be far greater than D7 and, therefore, the nodal voltage will be approximately 0 V. Another way to look at this is that D7 is biased with a very small current and hence via the Schottky equation, $V_D \propto \ln(1+I_D) \approx I_D$, for very small currents, which will be a very small voltage.

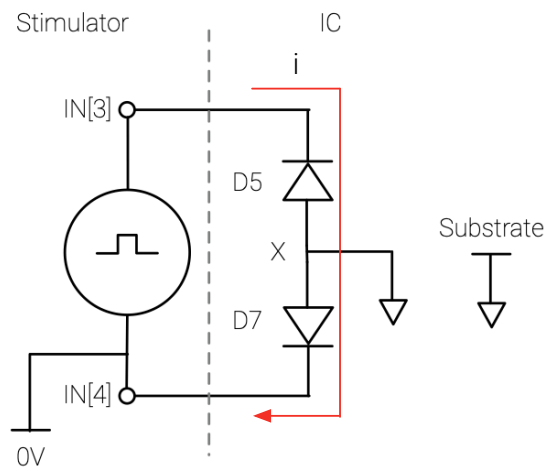


Figure 2-14 Interaction of the power harvesting circuit in regard to ground formation for stimulation signals.

2.4 Communication

In section 2.3, we discussed how biphasic stimulation incoming to the IC could be harvested to create an pseudo independent-supply on-chip. This power supply is necessary of course to control and configure the cross point switch. The question, which is the key focus of this

section, is how can biphasic current stimulation pulse be used to transfer data used to configure a switch array, and how can this work in the context of a two wire interface that is also required to power the chip. This problem is not unlike that faced by radio frequency identification (RFID) circuits [99].

2.4.1 Digital communication

A communication link can be described at multiple layers of abstraction from the physical layer all the way through to network layers used to describe the internet for example [100]. For chip-to-chip communication, the layer of concern is the physical layer.

There are a multitude of protocols familiar to many due to popularisation in consumer application as they are exposed as external ports on computers and other devices. These include protocols like USB and ethernet. For chip-to-chip communication, however, there are an array of common protocols that are less known outside of the world of hardware engineering. These include protocols like [101]:

- Parallel
- Serial UART (Universal Asynchronous Receiver/Transmitter)
- SPI (Serial Peripheral Interface)
- I2C (Inter-Integrated Circuit Communication)
- I2S (Inter-Integrated Circuit Sound Bus)

All these protocols come with trade-offs in flexibility and communication transmission speed that are too extensive to address here. Suffice to say that the communication link most akin to what is required for this application is actually UART. What makes this the case is that UART only requires two wires to communicate in one direction and three for bidirectional, unlike protocols like SPI and I2C that require an additional clock line. The ability to transmit information in one direction is referred to as simplex and the ability to transmit information in both directions is called duplex. There are two variants of duplex: half-duplex, where information cannot be simultaneous transmitted in both directions, and full duplex, where information can be transmitted in both.

The simplest communication protocol, as described by UART, is shown in Figure 2-15. Here there is some kind of trigger to start the transmission of a data frame. Once initiated, the data is sent as symbols. It is important to note that D_n does not necessarily refer to a single data bit. D_n denotes a symbol and each symbol can be one or more bits depending on the modulation scheme used.

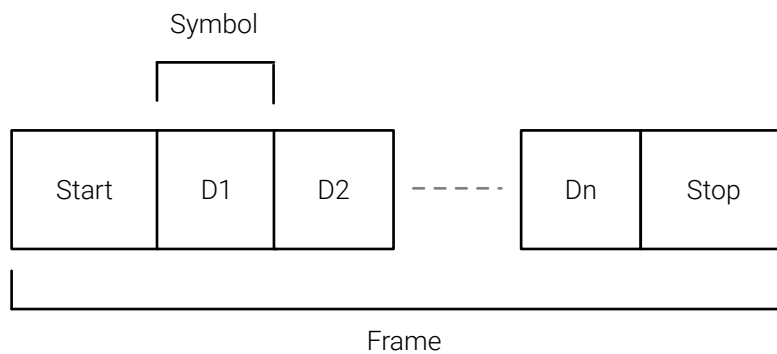


Figure 2-15 Basic data frame structure.

In the context of digital wireless communication, there are numerous modulation schemes that act on the modulation of a carrier wave. These include:

- ASK (amplitude-shift keying):
- PSK (phase-shift keying)
- FSK (frequency-shift keying)

Illustrations of these schemes are shown in Figure 2-16. In these examples, only one bit is transmitted per symbol. If the sine wave carrier shown above is now substituted for a biphasic stimulation pulse, the modes of modulation can be explored.

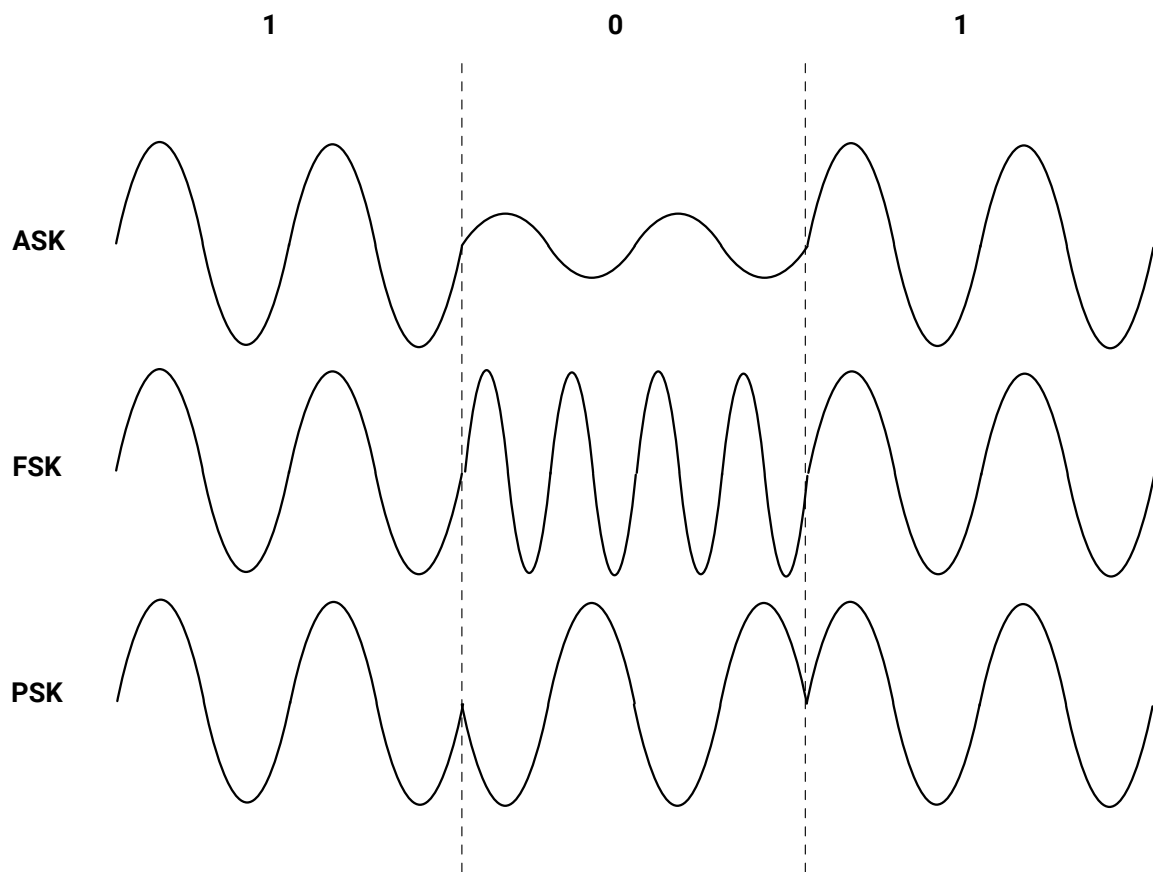


Figure 2-16 Fundamental modulation methods of a sine wave carrier.

2.4.2 Modulating a Biphasic Current Pulse

The fundamental parameters of a biphasic current pulse are shown below in Figure 2-17.

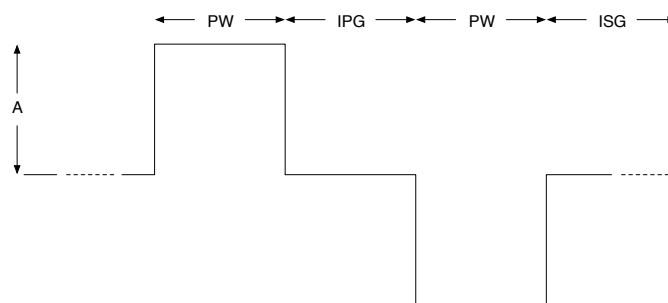


Figure 2-17 The biphasic pulse parameters.

ISI: Inter-Stimulus Interval
PW: Phase Width
IPG: Interphase Gap
A: Amplitude

It is now important to also define the symbol and the frame:

Symbol: Interchangeable with stimulation pulse, which is capable of carrying multiple bits of data.

Frame: A frame is used to communicate and latch a switch configuration.

As shown in Figure 2-18, fundamental modulations outlined above for a sine wave carrier can be translated to biphasic pulses modulations. In the examples, it is clear that for each of the three fundamental modulations, there is substantial redundancy. That is, the symbol representing a single bit is comprised of a multitude of parameters as shown in Figure 2-19.

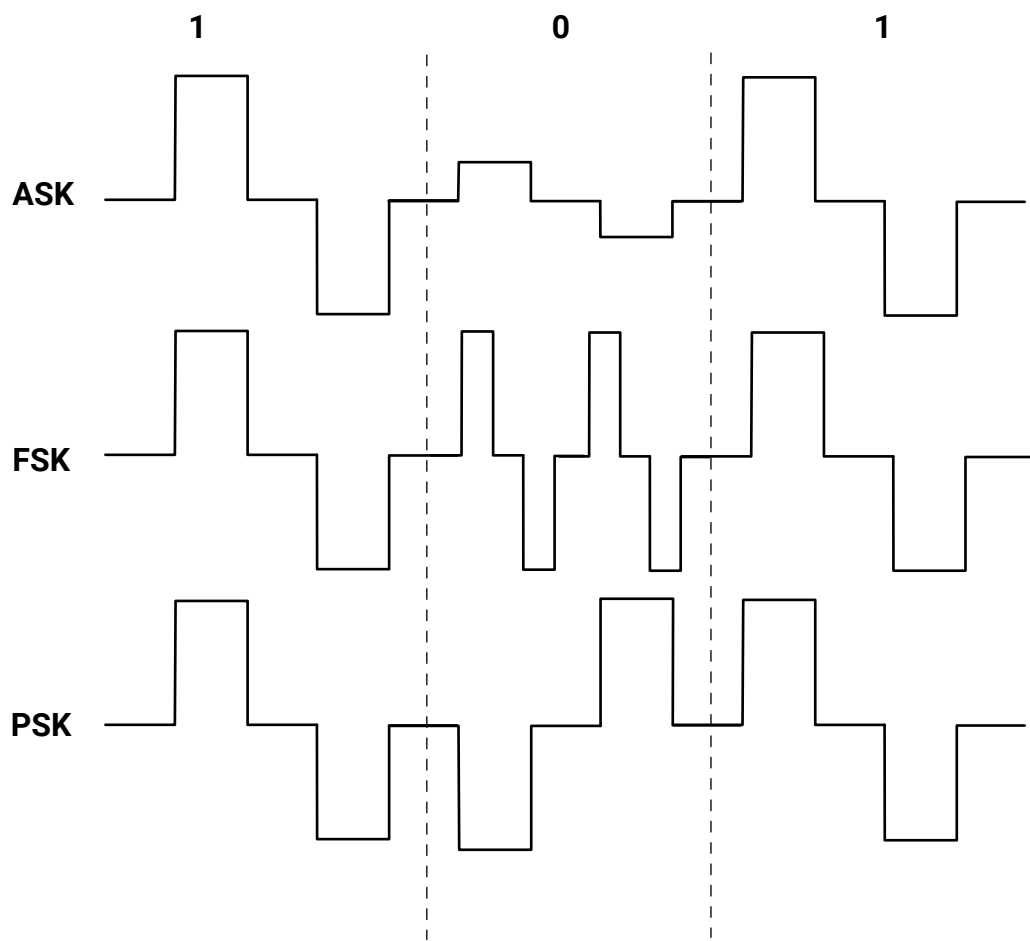


Figure 2-18 Modulation of Biphasic Current Stimulation pulses for ASK, FSK and PSK.

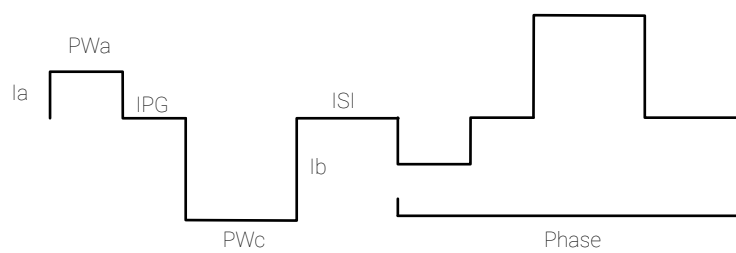


Figure 2-19 Modulation of all parameters without constraint.

Practically speaking, amplitude modulation presents a fundamental challenge. That is, stimulation is delivered as a current amplitude, not a voltage amplitude. What this means is that a fixed resistive load must be presented to convert the current mode waveform into a voltage via ohms law ($V = IR$) or the charge must be accumulated in a capacitor (which would need to be small and hence limit pulse charge). This would disturb the full-wave rectification process by limiting to some extent the size of the voltage waveform presented. It does, however, offer a clue to how full duplex communication can be achieved. Excluding amplitude – there remains IPG, ISI, PW_a , PW_c and Phase.

A further constraint can be applied to this problem. That is, the charge delivered in each phase must be equal to preserve charge balance. This was covered in Section 1.3.5, where tissue safety was discussed. Since the amplitudes must be equal, so too must the pulse widths.

This leaves IPG, ISI, PW and Phase as the four fundamental modulation parameters to be explored.

2.4.3 Symbol rate

In Section 2.4.2, four fundamental parameteres of the biphasic pulse have been identified for modulation.

1. Interphase Gap (IPG)
2. Pulse Width (PW)
3. Interstimulus Interval (ISI)
4. Phase

The degree to which these parameters are modulated is rerred to as the modulation index, and can be written as

$$\mu = \frac{A_M}{A_C}, \quad (2-7)$$

where A_M is the modulated signal amplitude and A_C is the carrier amplitude. Increasing the modulation index, can increase the signal immunity and error rate. However, in the case of time

base parameters being discussed here, it will come at the cost of reducing the overall speed of transmission.

A general expression can be derived for the speed of transmission that relates the symbol rate and the bits carried by each symbol,

$$T_{IPG,min}(1+b_0 \cdot \mu_{IPG}) + 2 \cdot T_{PW,min}(1+b_1 \cdot \mu_{PW}) + T_{ISI,min}(1+b_2 \cdot \mu_{ISI}), \quad (2-8)$$

where $T_{IPG,min}$, $T_{PW,min}$, $T_{ISI,min}$ are the minimum pulse widths for IPG, PW and ISI, respectively, b_1 , b_2 and b_3 are the first, second and third bits of the symbol, respectively, and μ_{IPG} , μ_{PW} and μ_{ISI} are the modulation indexes corresponding to IPG, PW and ISI, respectively. Note that the phase does not actually impact the symbol duration.

The instantaneous symbol rate can, therefore, be expressed as

$$\frac{1}{T_{IPG,min}(1+b_0 \cdot \mu_{IPG}) + 2 \cdot T_{PW,min}(1+b_1 \cdot \mu_{PW}) + T_{ISI,min}(1+b_2 \cdot \mu_{ISI})}. \quad (2-9)$$

It is clear that the average symbol rate will actually be a function of the data being transmitted.

The maximum symbol rate will occur when all bits are 0 and the minimum will occur when all bits are 1 (assuming modulation occurs on the bit 1). Although this analysis is being kept general, it is worth mentioning that for our application more switch cells will be switched off for any given configuration than will be switched on. That is, the data stream will be dominated by zeros. This works favorably to maximise the communication speed.

$$\frac{1}{T_{IPG,min}(1+b_0 \cdot \mu_{IPG}) + 2 \cdot T_{PW,min}(1+b_1 \cdot \mu_{PW}) + T_{ISI,min}(1+b_2 \cdot \mu_{ISI})} \quad \text{Eq 2-10}$$

$$\text{Symbol rate}_{min.} = \frac{1}{T_{IPG,min} + 2 \cdot T_{PW,min} + T_{ISI,min}} \quad \text{Eq 2-11}$$

$$\text{Symbol rate}_{max} = \frac{1}{T_{IPG,min}(1+\mu_{IPG}) + 2 \cdot T_{PW,min}(1+\mu_{PW}) + T_{ISI,min}(1+\mu_{ISI})} \quad \text{Eq 2-12}$$

Following on from these equations and assuming that 4 bits are carried with each symbol, the actual data transmission speed will be given by

$$\frac{4}{T_{IPG,min}(1+b_0 \cdot \mu_{IPG}) + 2 \cdot T_{PW,min}(1+b_1 \cdot \mu_{PW}) + T_{ISI,min}(1+b_2 \cdot \mu_{ISI})} \quad \text{Eq 2-13}$$

From this equation, it is clear that of all parameters, the pulse width will be the least efficient to transmit. This is because of its redundancy as it is repeated twice per symbol with equal pulse width to ensure charge balance.

2.4.4 Demodulating a Biphasic Current Pulse

Three classes of modulation have been identified. Namely, amplitude, phase and pulse width. Considerations will now be provided around the practicalities of demodulating these signals.

Pulse width can be readily measured by charging an on-chip capacitor with a current source as shown in Figure 2-20. The practical constraint of such a circuit is making sure the pulse width is not too long for the given I and C values, and also making sure that V_a is not too low, where it will be prone to noise and hence demodulation errors will occur.

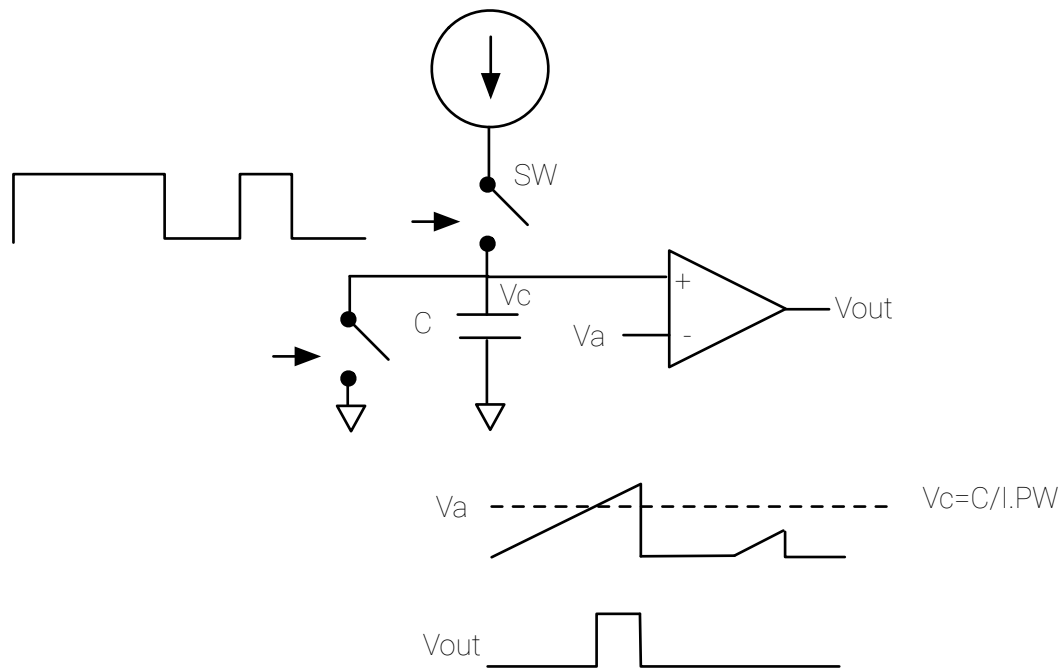


Figure 2-20. Simplified schematic showing basic mechanism of pulse width detection.

Rather than using a current source, it could be argued that the biphasic pulse itself could be used. If realistic values are considered though, like 100us pulse width, current 100uA, and a large on chip capacitor of 10pF, the voltage will already reach 1V. So, control of an ultra-low current source will be necessary in order to keep the capacitor sizes reasonable.

Next, amplitude modulation can be considered (although for practical reasons will be excluded as mentioned) as shown in Figure 2-21. In this diagram a resistive load is required to convert the current waveform into a voltage waveform and then compared to a detection voltage.

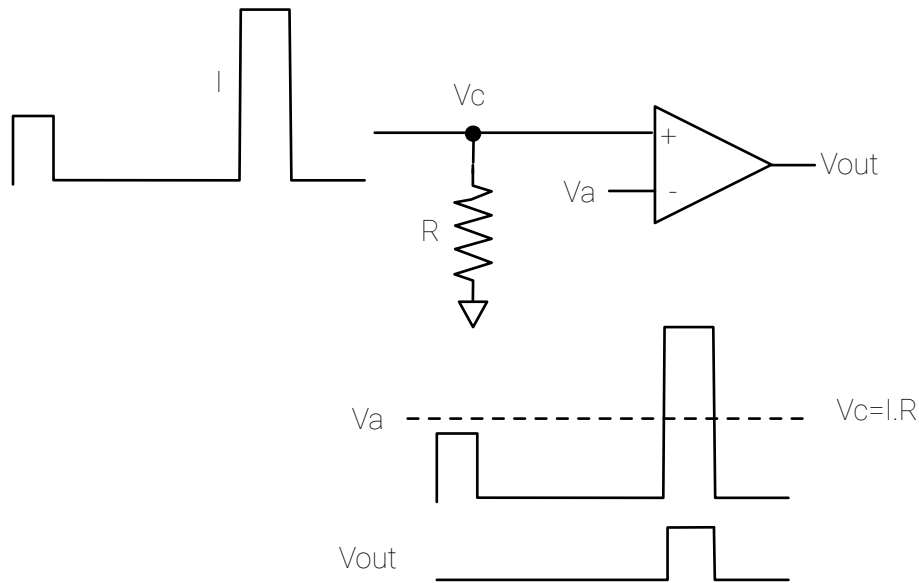


Figure 2-21 Current amplitude modulation detection.

One of the limitations of both the PW and amplitude demodulator circuits described is that they are based on a fixed threshold. This fundamentally limits the compatibility of the chip with different stimulators. A way to avoid this limitation is to base the demodulation on differential comparisons rather than establish an absolute threshold. What this means is that it is simply about a comparison to the past symbol and not to any absolute signal. This can be implemented for pulse width detection, which intrinsically contains a capacitor necessary to hold past values, but is more difficult for amplitude demodulation, where some kind of sample and hold capacitor would be needed.

Finally, phase detection can be inferred using simple logic on the differential pulse width detector. Since there are two capacitors, one for each pulse, logic can be used to detect a phase reversal.

2.4.5 Simulations of transmission rate

If we assume that the IPG, ISI and PW all have minimum values of 10 μ s and that the bits correspond to phase, IPG, PW and ISI (in that order), a simulation of the data rate can be obtained. Shown below are instantaneous data rates for 4 and 3-bit per symbol paradigms with modulation index ranging from 0.1 to 1.



Figure 2-22 Theoretical 4-bit instantaneous data rate based on transmission code and minimum pulse width of 10us.

Since the PW encoding will have some redundancy, it is worth also considering a 3-bit per pulse encoding strategy whereby the PW is not modulated.

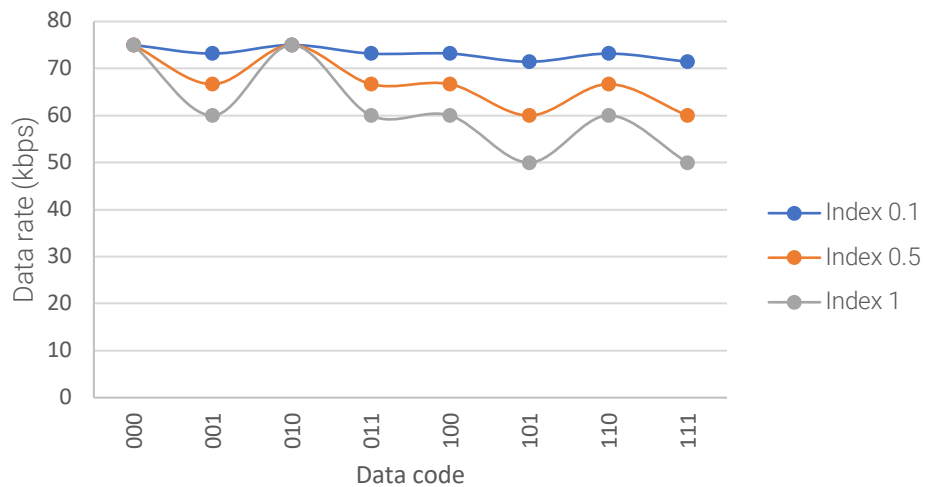


Figure 2-23 Theoretical 3-bit instantaneous data rate based on transmission code and minimum pulse width of 10us.

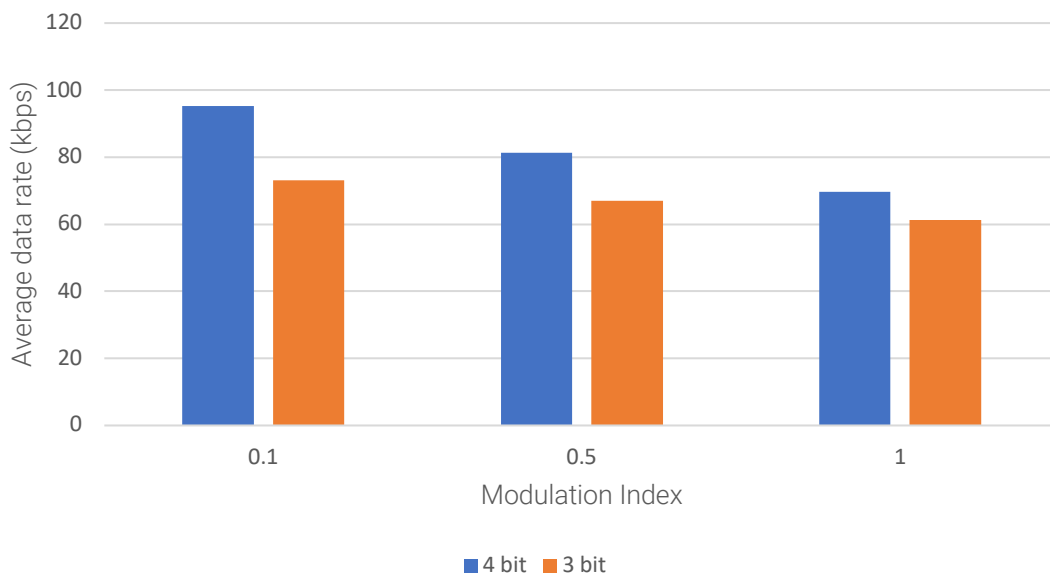


Figure 2-24 Average transmission rate for 3 and 4 bit for modulation index's of 0.1 to 1.

These simulations show, for a modulation index of 0.5, the average data rate for the 4-bit paradigm is only 18% better than for the 3-bit paradigms. Of course, this does not consider stimulator constraints in delivering ISI, IPG and PW of 10 μ s.

Whilst commercial stimulators typically do not advertise their parameter space, a device named neuroBi designed by Slater, Sinclair et al [107] for retinal stimulation will be used as an example. The minimim parameters of neuroBi are shown in Table 2-1. Based on these values, re-simulations of the 4-bit and 3-bit paradigms are shown in Figure 2-25 and Figure 2-26, respectively, with average transmission rate shown in Figure 2-27.

Table 2-1 neuroBi stimulation parameters.

Timing Parameter	Min (μ s)	Step size (μ s)
ISG	100	1
IPG	20	1
PW	20	1

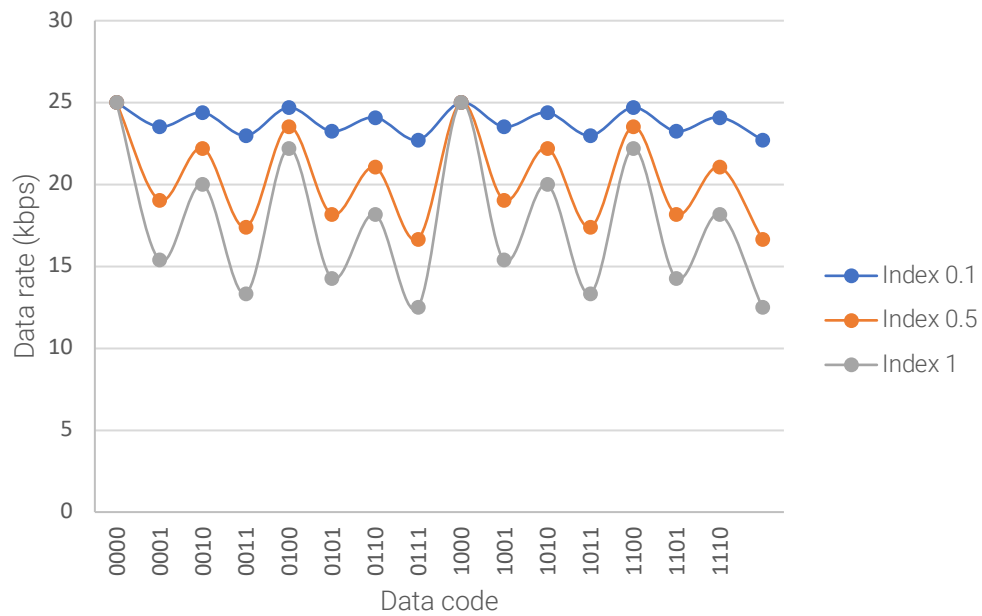


Figure 2-25 Instantaneous 4-bit data rate based on transmission code and neuroBi stimulator constraints.

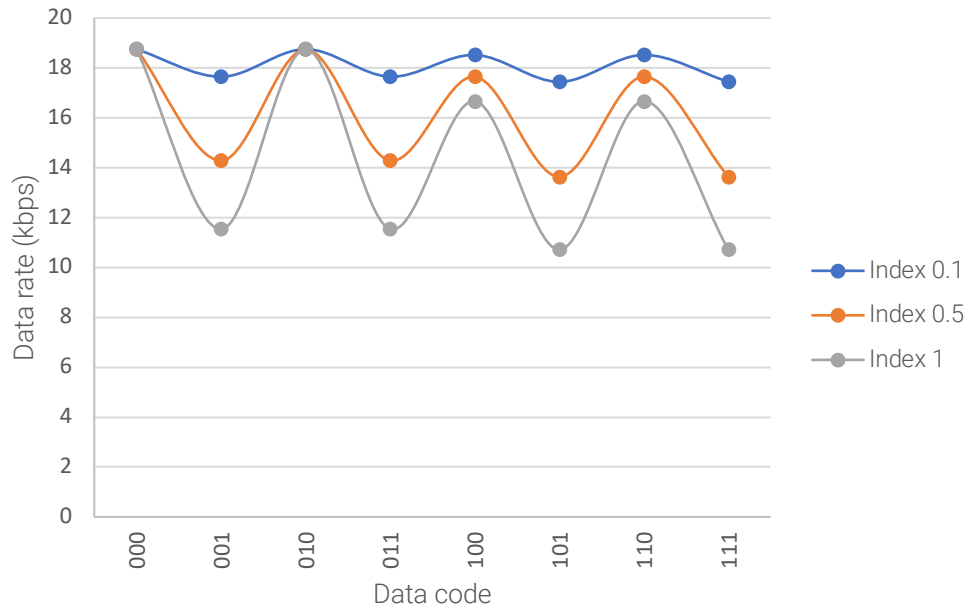


Figure 2-26 Instantaneous 3-bit data rate based on transmission code and neuroBi stimulator constraints.

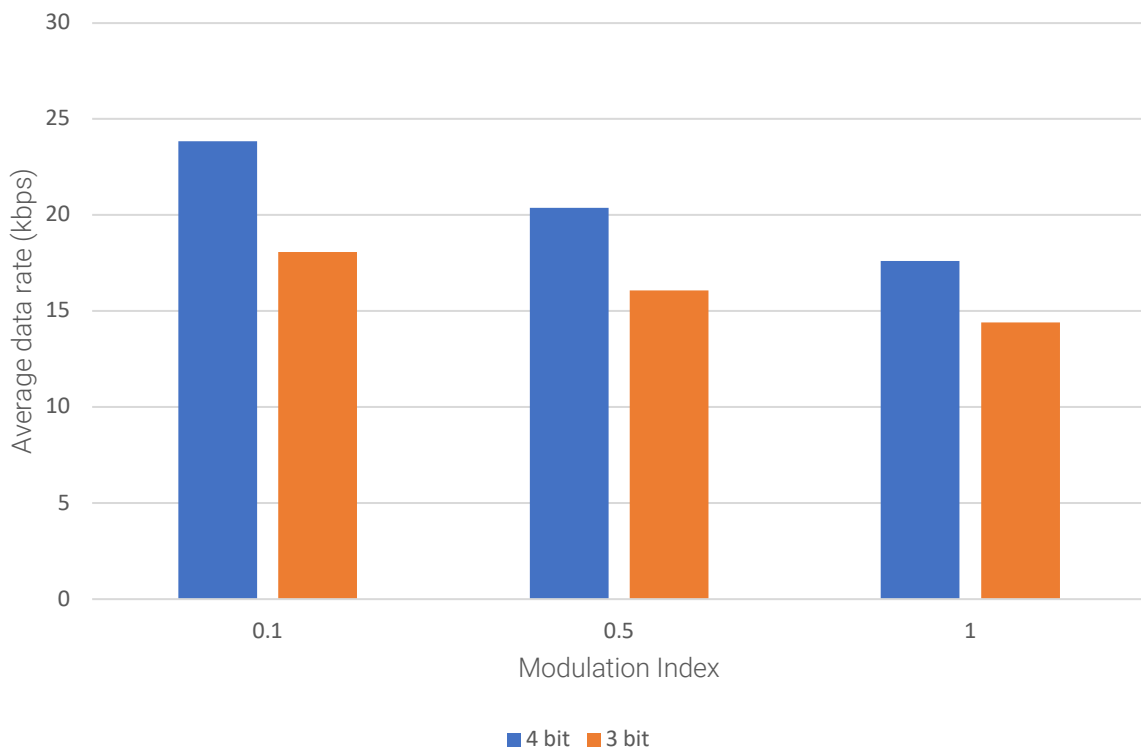


Figure 2-27 Average transmission rate for 3 and 4 bit for modulation indices of 0.1 to 1 and neuroBi stimulation constraints.

The simulations shown in Figure 2-25 through Figure 2-27, show a marked reduction in the average data rate possible when the constraints of a real stimulator are enforced.

There are several key points to summarise:

- If each symbol is encoded by 3 and not 4 bits (by ignoring the pulse width), for robust modulation indexes the decrease in transmission rate is only 18% and not 25% as may be intuitively expected when not factoring in the redundancy.
- The bit rate will be fastest when coding 0s rather than 1s.

2.4.6 A Two Wire Biphasic Protocol

In Sections 2.4.1-2.4.5, the fundamental framework for how to construct a novel protocol using biphasic pulses was presented. The biphasic pulse can be described as a symbol in which pulse width parameters are modulated. Simulations were performed that demonstrated the theoretical limits of the transmission rate.

With this analysis complete, a number of conclusions and considerations were outlined. However, it is now time to piece together the protocol in a way that respects the practical limitations and considerations outlined in previous sections.

The first step in the transmission of data is the identification of the data frame itself. Since pulse width was not used in modulation, as described in Section 2.4.5, it is an ideal candidate to form the start of frame (SOF). Modulating the symbol such that SOF has a larger pulse width compared with the symbols within the frame that make up the data makes the most sense since there are less SOF than Data symbols.

Next, we can assume that the data will be modulated using the IPG, ISI and Phase: 3 bits per symbol. However, there is a catch with pure differential modulation schemes as illustrated in Figure 2-28, namely that once you increase the PW to encode a 1 say, you must actually keep it at this PW, otherwise you will encode another 1.

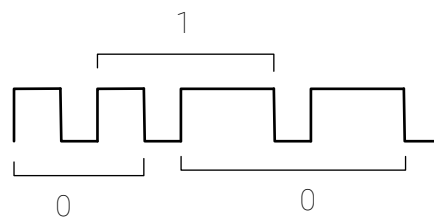


Figure 2-28 Differential pulse encoding can lead to long transmission rates when data does not change often.

This is not ideal, particularly considering that 1s will be infrequent in comparisons to 0s for most switch configurations (less switches on than off). To overcome this issue, the start of frame

IPG, which does not encode data, can instead be used to set the comparison pulse width for which all data frame symbols will be compared.

So, putting this all together. A start of frame is detected when the pulse width increases relative to the past pulse and an end of frame event occurs the pulse width decreases relative to the past pulse. The start of frame also encodes the pulse width comparison via its IPG and all data frame symbols compare to this as show in Figure 2-29.

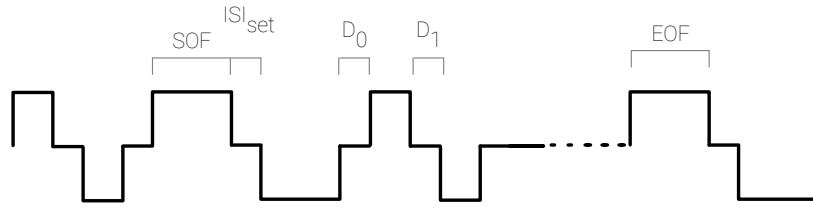


Figure 2-29 Biphasic pulse train protocol showing SOF, ISI threshold, data transmission and EOF.

Finally, if we assume the parameters of the neuroBi as outlined in Table 2-1, we factor in that there are now only 2 bits per symbol and assume a modulation index of 0.5. The average data rate will be approximately equal to 10kbps. If we assume a 6 x 64 element array (384 switches), the configuration time will be 38.4ms. This could present a limit depending on the application and is an important consideration when using XPAND. Efforts to reduce this by encoding will be discussed in 2.4.7.

The average transmission rate, assuming random distribution will be given by equation 2.14.

$$\frac{\sum_{(b_0, b_1)} \frac{2}{T_{IPG, \min}(1+b_0 \cdot \mu_{IPG}) + 2 \cdot T_{PW, \min} + T_{ISI, \min}(1+b_2 \cdot \mu_{ISI})}}{4} \quad (2-14)$$

2.4.7 Encoding

In practice, the switch array will be required to be configured mostly in a set of common configurations and encoding can be used to reduce raw data size. Additionally, the data frame can be made more robust with the use of parity bit and cyclic redundancy checking (CRC) [102], which would be needed in a commercial release of the integrated circuit. Such a circuit can be readily implemented using asynchronous logic fed with the input data and clock generated by

the biphasic pulse train. This logic would consist of XOR and shift register blocks. This will not, however, be discussed in detail as it was not implemented in this version.

Rather than sending 384 bits of data to explicitly configure the array, a set of commands that define a specific paradigm can be defined and, in the event that the configuration is not covered by these commands, there can also be a command that enables full definition of each switch cell. If we assumed 8 commands, this could be represented by only 3 bits. So, in the event the 384 is needed, there is only a very marginal cost of 3 bits, and these 3 bits define the way in which proceeding configuration data is treated.

A set of commands for the sake of example is shown in Table 2-2.

Table 2-2 Hypothetical commands for key configurations.

Command	Function
000	Full config
001	Bipolar
010	Common Ground
011	-
100	-
101	-
110	-
111	-

Full Config

In this mode, the command is set to 000. The proceeding data then specifies every single switch.

Bipolar

In this mode, the command is set to 001. The proceeding data then specifies the row and columns of the two switches to be set.

Common Ground

In this mode, the command is set to 010. The proceeding data then specifies the active switch and enables all others.

As an example, say the crosspoint needed to be configured such that IN[1] was connected to OUT[1] and IN[2] connected to OUT[64]. This could be achieved using the Bipolar command shown in Figure 2-29.

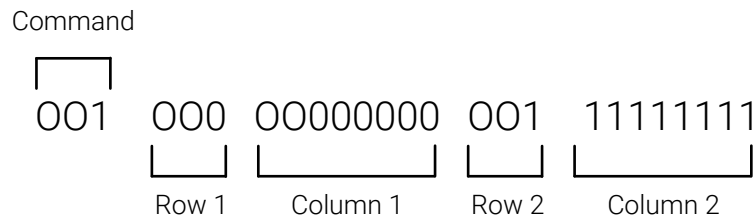


Figure 2-30 An example data packet construction consisting of command and configuration data.

In total, this is 25 bits, which is only 6.5% the size of the data required if a full configuration requiring 384 bits were sent. Assuming a data rate of 10kbps, the transmission time for this configuration would be 2.5ms (6.5% of 38.4ms required when not encoded). This would substantially improve the flexibility of XPAND for applications requiring rapid re-configuration.

2.4.8 Bidirectional communication

There are two types of communication interface. Simplex that communicates in only one direction and duplex that communicates in both directions. Of duplex there are two types: half duplex where communication is done in one direction at a time and full duplex that enables simultaneous transmission in both directions.

This chapter has covered a variety of topics relating to the stimulation and recording expansion of commercial stimulators. But what if the stimulator does not have dedicated recording channels that can be connected to the array once configured by the stimulator? On first pass, this may seem an impossibility since the stimulator is connected only via a couple of stimulation lines. However, many implantable devices include some degree of measurement of the voltage waveform resultant on the internal current source to measure the tissue impedance and as such can receive information about the outside world. The central idea here is that a

load could be switched in and out of the loop of the stimulator that would in turn modulate the resultant voltage waveform thus communicating information back to the stimulation.

Consider the system shown in Figure 2-31. This circuit modulates the voltage across the cathodic phase of the biphasic current pulse. If the stimulator includes a voltage waveform ADC (which many do), this can simply be demodulated on the stimulator side. In this way, each stimulation pulse will have a corresponding sample. This is complex and is pushing very close up against the constraints of the system and the complexity and complication is potentially beyond the return it would deliver.

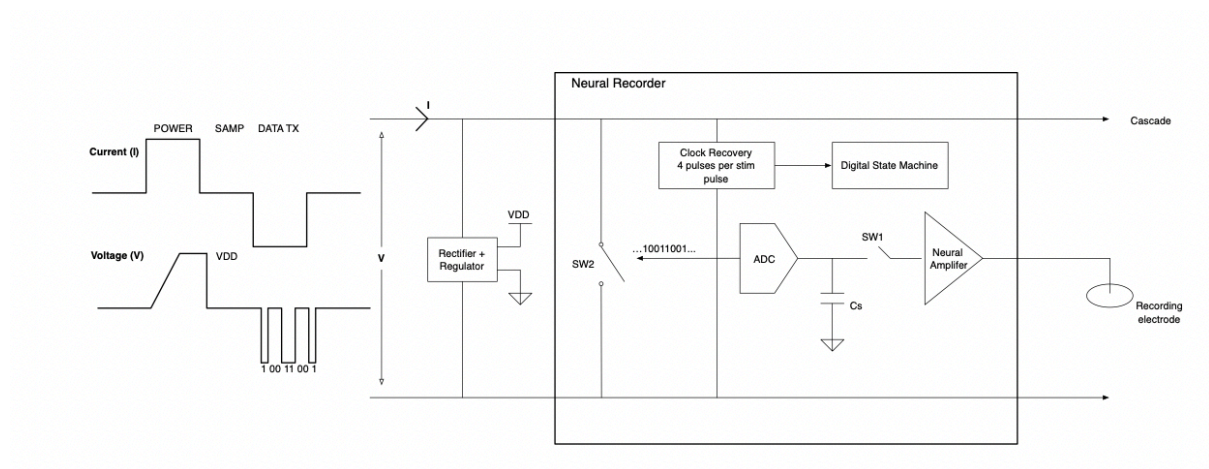


Figure 2-31 A concept neural recording structure to enable 1 sample for stimulation pulse.

A simpler use of this concept of load modulation applies to the back-communication of basic IC state. Since amplitude is not used to encode data from the stimulator to the IC, it can be used for telemetry. In this way, full duplex communication is possible using a Biphasic Protocol as shown in Figure 2-32. Pulse Width encodes SOF and EOF, ISI and IPG encode data, and the biphasic pulse voltage (created by load modulating the current pulse) encodes XPAND state.

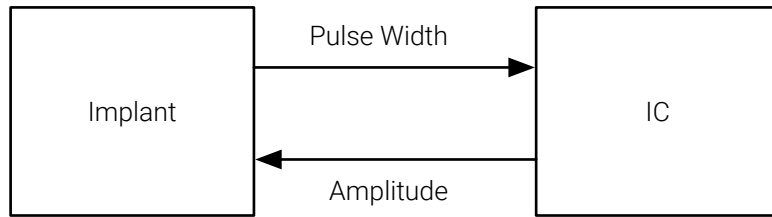


Figure 2-32 Data interface between implant and IC showing pulse width coding transferring data to IC and amplitude coding simultaneously being transferred back.

2.5 Summary

In this chapter, some fundamental considerations were explored towards the premise of developing an expansion integrated circuit to increase electrode count of commercial stimulators for use in brain recording and stimulation applications. The concept of using a large cross point switch or clusters thereof was proposed and the architecture of such an array discussed in relation to stimulation and recording considerations.

It was next argued that the use of existing stimulation lines for power and communication to such a chip would minimise the modifications required to a commercial stimulator whilst having the benefit of being intrinsically safe due to the charge balanced nature of the stimulation signals.

Based on the assumption that biphasic pulses would be used, harvesting such pulses for the purpose of powering the IC was discussed. A full wave rectification method was outlined with key considerations given to the terminal voltages such a scheme would elicit.

Next, a systematic review of the fundamental parameters of biphasic pulses was explored in relation to communication of data. First, the data encoding of a symbol was explored in relation to the modulation of fundamental electronic parameters of the biphasic pulse, namely amplitude, pulse width and phase. With symbol modulations outlined, realistic symbol rate showed transmission rates as high as 100kbps. However, taking into account stimulator

limitations and the practical constraints of implementation, a more realistic communication rate of 10kbps was determined.

To reduce the amount of data needed in transmission, a compression strategy was proposed and shown to reduce config data by nearly 95% for a bipolar switch array configuration. This gave head room to incorporate more sophisticated transmission protocols including cyclic redundancy checking (CRC). Such methods could be readily employed using asynchronous logic circuits acting on the main data input register but were not discussed in any detail as they were not implemented. In its minimalist form, the protocol suggested included a start of frame (SOF), command, data and an end of frame (EOF).

Finally, a conceptual framework for understanding how bidirectional communication is possible with only two stimulation lines was outlined. In essence, the configuration of the switch array can be performed using the pulse width modulation of the ISI and IPGs comparing with the IPG of the start of frame pulse while back communication can be performed using amplitude modulation. In such a way, an ultra-low redundancy and low wire count interface is possible and biologically safe. Every controllable parameter of the biphasic waveform is exploited. The pulse width for the SOF and EOF. The ISI and IPG for the communication of data within the frame, and finally the stimulation amplitude controlled by load modulation in the IC enables full duplex communication.

3 XPAND Architecture and Circuit Design

In Chapter 2, the basic conceptual framework for expansion of commercial stimulators was discussed. The prime motivation for such an approach is to minimise the hardware changes required to commercially available stimulators and, thus, regulatory overhead to expand capabilities for brain recording and stimulation applications. In this chapter, the architecture of an integrated circuit called “XPAND” will be described. Following this, the key functional blocks will be discussed in detail. This will essentially take the work of Chapter 2 and focus on the circuit level abstraction.

This chapter is based on the following stimulator parameter specifications as shown in Table 3-1 and Table 3-2, which are consistent with the parameter space of the target neural stimulator “neuroBi” [107]. Note that in a commercial release of the chip, architecture need not change, but tuning of the timing circuitry would be needed to best match the stimulators pulse parameter specifications.

Table 3-1 Stimulation input requirements.

	Min	Max
Pulse Width	5us	150us
Current Level	10uA	10mA
Compliance Voltage	5V	15V

Table 3-2 Biphasic Pulse Requirements.

	Min	Max
ISI/IPG	5us	150us
SOF Pulse Width	30us	-

3.1 XPAND Architecture

A Crosspoint switch to expand stimulator capability does not sound like a complex proposition. However, as was described in Chapter 2, such a system in practical applications for the

expansion of commercial stimulators will necessitate the use of single biphasic pulse power communication delivery to control the switch array. The highly nested nature of this problem makes it extremely complex to design. Not being able to fan out the design easily to known functional blocks which is possible when power, communication and I/O signals are established in a conventional way.

Much thought and consideration were given to the formulation of how an IC could be designed to power up and configure using the biphasic stimulation pulses alone and configure a switch array that can enable expansion of the number of electrodes for which can be stimulated and recorded from. The architecture was eluded to in Chapter 2, but now can be fully expressed in terms of the key building blocks as shown in Figure 3-1.

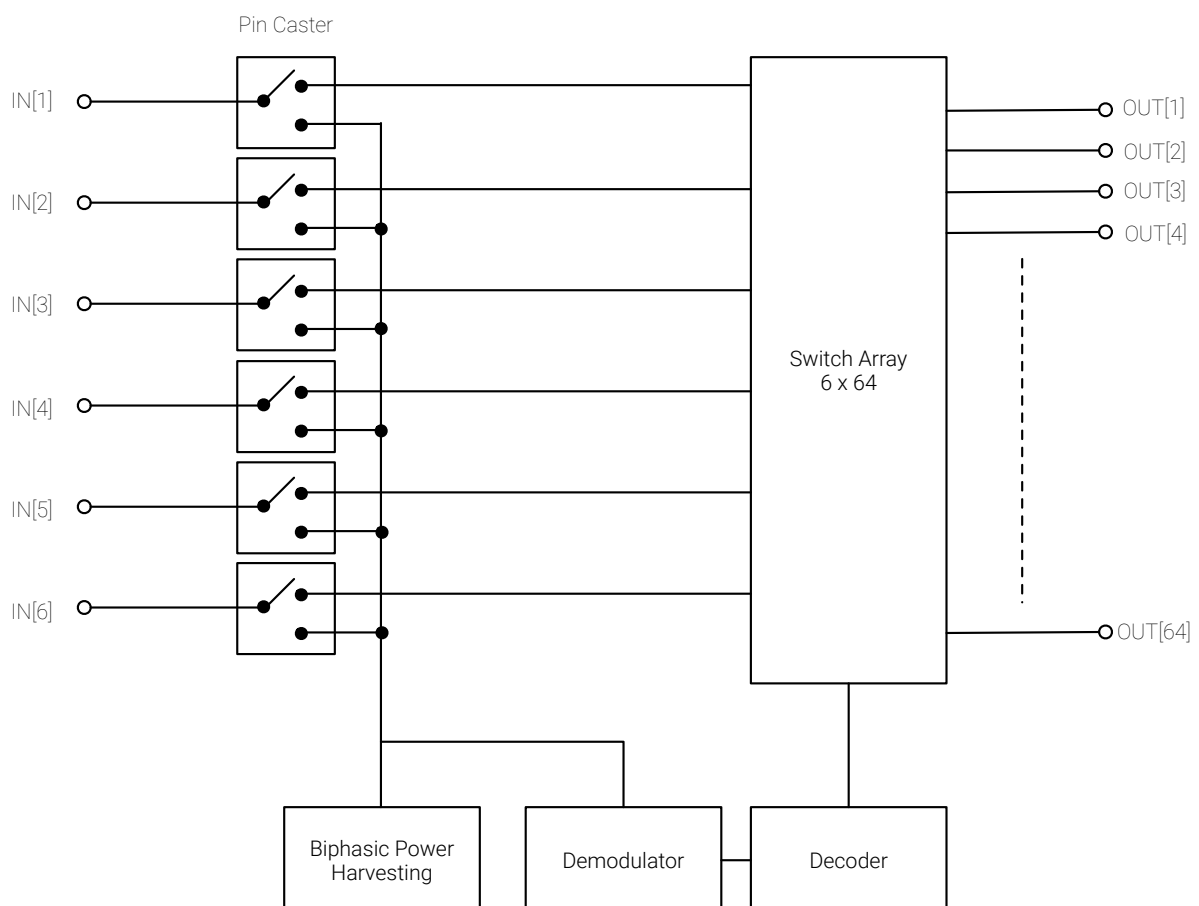


Figure 3-1 Complete architecture of the XPAND chip.

In describing the architecture, the switch array is a good place to start, as it provides the core functionality of the chip; i.e., to enable an array of input stimulation lines coming from a commercial implantable stimulator to connect to up to 64 output electrodes. Again, this is of benefit for applications such as epilepsy, where broader electrode coverage can be an advantage with high density arrays.

If XPAND were powered by DC supply and standard digital communication interface, the design would be a trivial crosspoint switch. However, this application excluded the use of a DC supply because of the unacceptable risk of contacting tissue if the chip were to be embedded outside the implant within an electrode array for example. Tissue damage through DC is a well-documented phenomenon covered in Section 1.3.5. Mounting the chip within the hermetically sealed container is another option but would require substantial change to the internal electronics and also the feedthrough and cable assembly, which would need to be redesigned to support ultra-high-density channel count. For these reasons, it was deemed necessary that power and communication be delivered via biphasic stimulation pulses.

In addition to the sole use of biphasic stimulation lines for the power, communication and configuration of the chip, it was desirable to provide redundancy in the event that a stimulation lead was damaged. In embodiments where the chip could be sealed inside a flexible silicon electrode assembly, for example, breakage of a wire is a distinct possibility. Therefore, it was decided that the chip should allow for multiple lines to be used for power and communication. The issue this introduces, however, is a reduction in the number of functional stimulation lines; i.e., lines that can be used for stimulating and recording from the brain.

To overcome the challenge of multipurpose connections, a novel structure called “pin casting” is proposed. The idea of pin casting is that any of the input lines from the stimulator connecting to XPAND can be set to function as either power/configuration or be used for stimulation/recording. XPAND input lines are “cast” upon start-up of the chip. The chip needs to be reset to establish new lines. This introduces redundancy to the chip interface while not compromising the number of electrodes that can be used in a functional sense. It does, however, substantially complicate the design and, of all the challenges in the design of XPAND, the challenge that proved most difficult. To be ready and waiting on start-up, but not interfere beyond start-up, required deep consideration of the power-up region.

Assuming power and communication lines are cast, this leaves the last three blocks, which are somewhat related at start-up but operate largely independently once power is stabilised: power harvesting, demodulation and decoding blocks.

The harvesting block is responsible for charging an internal supply capacitor within XPAND using the biphasic stimulation pulses. Since XPAND is designed to operate at a current far lower than the charge delivered for power and communications, it will essentially replenish once power is established. In addition to storing power on the built-in capacitor, the harvesting circuit also includes a regulator required to establish a clean 3.3V signal for digital circuitry and sensitive analogue circuits like the demodulator.

The demodulator is responsible for detecting pulse width changes for start of frame (SOF) and end of frame (EOF), and also the ISI and IPG widths that carry the data of each frame. With the signal demodulated, it can be “self-clocked” through to a data frame register. If explicit programming of each switch cell is required, the data frame size will equal the number of switches, which in the case of a 6 x 64 array will be 384 elements. Previously, in 2.4.7, an encoding methodology was described as a way of reducing the number of configuration bits and hence the configuration time. This was not, in the end, implemented due to time constraints.

XPAND operates in three distinct phases power up, configure and low power mode, which will now be discussed.

Power Up

Power is derived from biphasic current pulses applied to any two inputs of XPAND on start-up. This energy is stored on an integrated capacitor build using an array of thousands of high voltage NMOS device gates (2644 37x37um HV NMOS). When sufficient charge is stored on this capacitor, a CAST signal is asserted. This signal casts the current state of the input pins; i.e., the two that were used to deliver power are cast to that function and all other pins are isolated from power and communication systems. The state of the input casting cannot be changed within any given power up cycle. The biphasic power stimulation of the chip must happen continuously to ensure the internal capacitor is kept well charged. This is discussed in

Section 3.1.1. The pulses used to power up XPAND should be minimum width to allow for efficient modulation of the SOF which is detected on an increase in pulse width.

Configuration

The theoretical limits of communication via biphasic pulse delivery were considered. This exploration in Chapter 2 started with an unconstrained and idealist construction that was then whittled down by practical considerations. The conclusion was that two bits are transmitted per stimulation pulse for data transmission, encoded via the pulse width of IPG and the ISI and that each data frame comprises a SOF pulse, to initiate configuration data followed by an end of frame. The SOF is detected when the pulse width is longer than the previous pulse. Power and configuration data are always transmitted with the stimulator's minimum pulse width. When SOF is detected, the data demodulation is enabled.

With data demodulation enabled, IPG and ISI widths are demodulated to extract a binary string. The threshold width is set by the IPG of the SOF pulse. The demodulated data stream is clocked into a large configuration shift register via a clock signal derived from the biphasic pulse. The EOF is detected when the pulse width is longer than the previous pulse. The switch array is configured on detection of the EOF pulse.

XPAND has no general-purpose processor or a clock and, as such, needs to rely on asynchronous events triggered by the stimulation pulses. This is necessary for clocking in the demodulated data to the frame register and configuring the array on the EOF.

Low Power mode

With the configuration asserted on EOF, it is ideal for XPAND to enter a low power mode where all non-essential components are shut down. The question then arises: how is it woken up? There are two methods explored for this. The first involves detection of an ISI or IPG longer than a certain duration. The second involves the simply shutting down core blocks when an EOF is detected. In this mode, it will enter an ultra-low-power state where all logic is disabled and the HV states remain latched. In this configuration, the only losses will be due to leakage, which will be in the order of picoamps. In this configuration, the state of the array can be maintained with

the need to only top the array up infrequently. It becomes clear that the demodulator is necessary to detect a wake-up event, and that by necessity so too are core components used to provide power.

3.1.1 Power Considerations

Choice of communication and power parameters are restricted by the amount of energy that can be stored on the main storage capacitor and the power requirements of XPAND. The storage capacitor will be made as large as possible but, as a conservative estimate, a size of 100pF will be assumed to set a lower bound for these calculations (though a higher capacitance was actually achieved). With this assumed capacitance, we have two parameters that can be defined: the **maximum off time** (time period in which no power is being delivered to the chip) and the **static power consumption**. These parameters, along with the capacitor size, define the maximum droop,

$$\Delta V_D = \frac{T_{\text{Off}} \cdot I_{\text{Static}}}{C_S}, \quad (3-1)$$

where T_{Off} is the maximum time no current is delivered (ISI and IPG), I_{Static} is the quiescent consumption, C_S is the main storage capacitor and ΔV_D is the maximum droop. If the supply on chip is allowed to droop too low, this could impact the regulator for low supply voltages since it will struggle to regulate to 3.3V. Additionally, it will lead to possible switching issues as the stimulation signals may overshoot the chip supply. A reasonable compromise is to assume 0.5V is allowable or less than 10% of the supply. This still leaves T_{Off} and I_{Static} to define.

It is important to note that this analysis relates to the period in which a data frame is being transmitted; outside this region, I_{Static} may or may not be the same and this is dependent on whether sleep mode is activated. Consider this analysis as it relates to the transmission of the data frame. When communicating a data frame with XPAND, the maximum off time will simply be equal to the maximum IPG/ISI (assumed to be equal). T_{Off} will depend on the stimulator; the choice of this parameter must not exclude stimulators that may have larger minimum IPG and ISI. A maximum IPG and ISI is chosen to be **150us**. This will accommodate the neuroBi stimulator, which has a minimum ISI of 100us. This then leaves the maximum static consumption to be **330nA**.

The static power consumption of XPAND at a high level will be the contribution of a current reference/bias generator, demodulator and the regulator. All other circuits have a static current consumption of approximately zero (picoamp leakage in low and high voltage complimentary logic),

$$i_{\text{Static}} = i_{\text{Regulator}} + i_{\text{Bias Gen}} + i_{\text{Demodulator}} \quad (3-2)$$

If the regulator and bias generator circuits are chosen to have a current consumption of **200nA** in total, this leaves **130nA** for demodulation. The choice of 200nA was estimated based on early simulations of the architecture under consideration.

Before progressing to the demodulator, it is necessary to consider the sleep mode. When XPAND is not being provided with power, it is essential that static power consumption is minimised so that it is able to float and the main storage capacitor does not discharge. Since the demodulator uses the off period for data encoding; this can be used to detect when to shut down XPAND. If the capacitor in the demodulator charges past a threshold, it has exceeded the maximum off-time and SLEEP is asserted. This shuts down the bias generator and regulator but still provides a voltage of 3.3V to the demodulator. This is essential to supply the demodulator logic as it waits for the next detected signal. When a signal is detected on the demodulator, the SLEEP mode is disabled and, after a short time, T_{Enable} , the bias circuit and regulator switch on.

The demodulator needs to accommodate current pulses of 5-150us. Assuming the maximum charging voltage of the demodulator is 2.5V (for 3.3V supply) to allow adequate headroom for sleep mode detection and a demodulation bias current of 10nA. The required capacitor can be calculated to be 600fF using

$$C_{\text{Demodulator}} = \frac{i_{\text{Charge}} \cdot T_{\text{PW,max}}}{V_{\text{MAX}}} \quad \text{Eq 3-3}$$

Key parameters relating to chip power and storage are summarised in Table 3-3.

Table 3-3 Chip power and storage requirements.

	Min	Max
Capacitor (HV)	>100pF	-
Capacitor (LV)	>10pF	-
Regulator Voltage	3.3V	-
Regulator (I _q)	-	100nA
Bias Generator (I _q)	-	100nA

3.2 Crosspoint switch

A basic illustration of a crosspoint switch is presented in Figure 3-2. While the complexity of the design resides mostly in the power and communication to configure the array, careful consideration was still required in the design of the crosspoint switch and each individual switch cell. Each switch must be able to withstand the maximum voltage of the stimulator, which was assumed to be 15V, and deliver a maximum current of 10mA. In addition to this, the switch must be able to tolerate negative transients, which will result to some extent from rapid current phase reversal and also positive transients beyond supply since the supply voltage can droop, and will never in any case reach the compliance of the stimulator because of the voltage drop of the full wave rectifier.

The on resistance of the switch is not a major factor for recording, where the impedance is largely dominated at the electrode interface but is important to consider at large stimulation currents as it will have the effect of reducing the compliance voltage of the stimulator. The effective compliance voltage of the stimulator is given by

$$V_{\text{comp}} = V_{\text{comp,stim}} - 2 \cdot R_{\text{on}} \cdot I_{\text{stim}} \quad (3-4)$$

Finally, the switch must be bidirectional, controlling current flow in both directions.

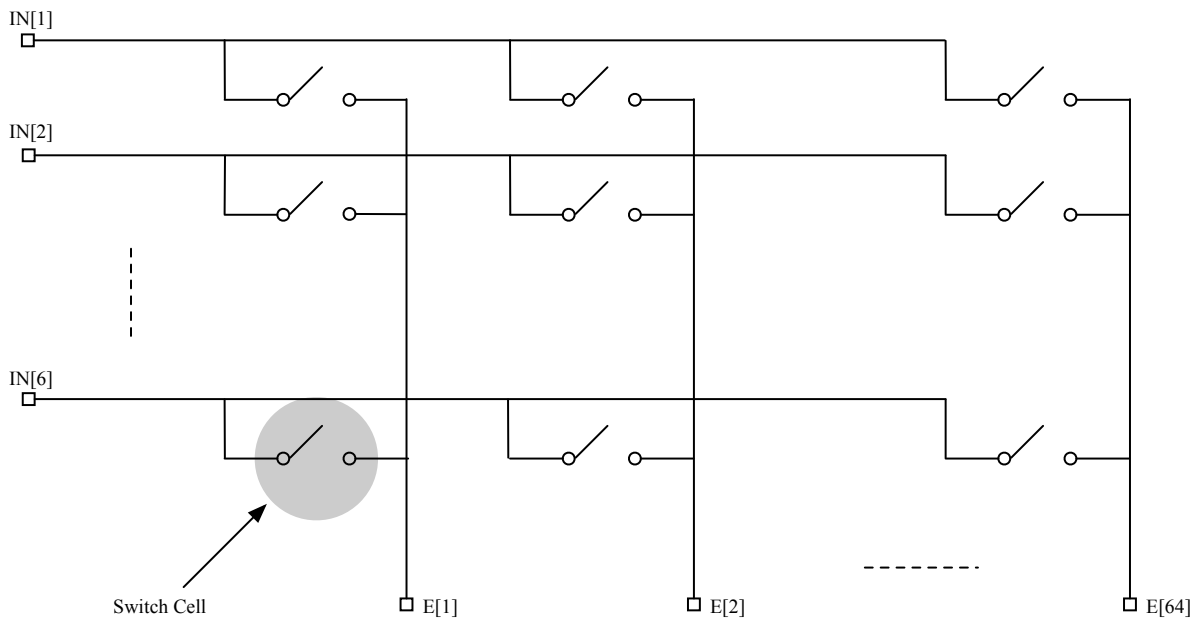


Figure 3-2 The single switch cell context of the entire switch array.

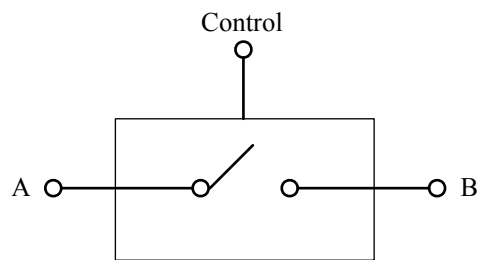


Figure 3-3 The basic switch cell functional block

To summarise, the key requirements are:

- $R_{on} < 100 \text{ ohm}$
- $V_{input(max)} = 20V$
- Bidirectional
- Latch-up prevention
- Minimal footprint
- Current transmission of 10mA

While the switch cell can be as simple as a high voltage transistor, there are implementations that are more complex requiring dozens of transistors to implement but offer major benefits to

footprint size and control. Dozens of low voltage transistors can have a smaller footprint than one single high voltage one. The various transistor topologies will now be described.

3.2.1 Switch topology options

In consideration of the design of switch topologies, a significant amount of time was devoted to investigating a novel solution to reduce the switch cell footprint, substantially reducing the physical size of the chip and thus cost of fabrication. These will now be discussed.

Transmission Gate

The transmission gate, shown below in Figure 3-4, is ubiquitous in mixed signal electronic design [97]. The benefit of using complimentary NMOS and PMOS devices in parallel is to create a more constant switch resistance across input signal range and terminal voltage range, as illustrated in Figure 3-4. In such an arrangement, the NMOS device will be most conductive for lower signal levels and the PMOS for higher signal levels. This is a result of the relationship between the conduction of the transistor and its gate source voltage. That is, as the gate source voltage approaches zero, so too will the current (in reality it is not zero, but the conduction is low).

With a high voltage applied to the NMOS gate of V_a say, the signal will switch the NMOS off when the signal approaches the voltage of V_a minus the threshold. This is because the transistors gate-source will be less than the threshold of the transistor. Similarly, the PMOS will begin to switch off when the signal approaches 0V plus the threshold of the PMOS. This effect is illustrated in Figure 3-5 where conduction across full signal is relatively constant. It is important to note that the body of the PMOS must be tied to the highest potential; otherwise, conduction through the substrate will occur since the body of the PMOS and the substrate form a PN diode. The NMOS (in its conventional form) is actually tied directly to the substrate.

For both devices, an effect called the Body Effect will occur [103]. Put simply, this phenomenon increases the effective threshold voltage of the transistor when the source is not tied to the ground for NMOS or VDD for PMOS.

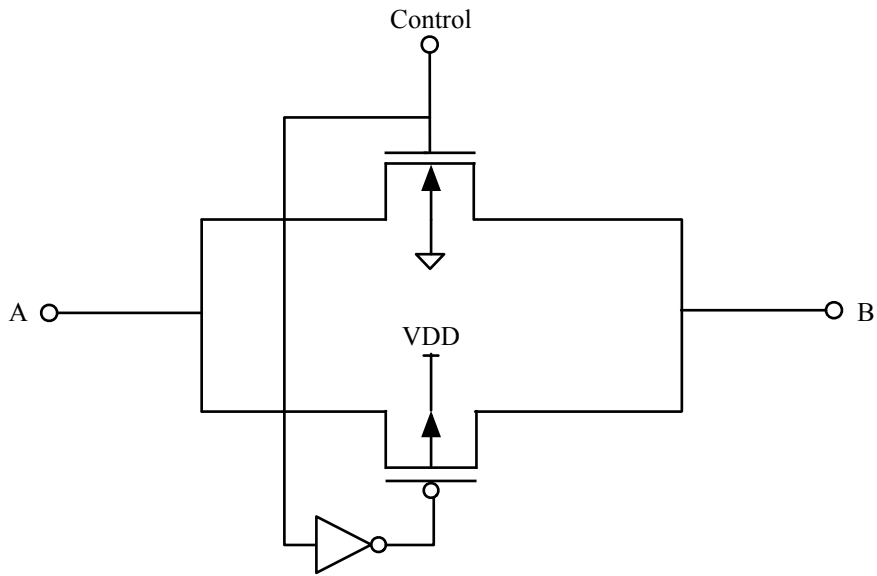


Figure 3-4 Conventional CMOS transmission gate topology.

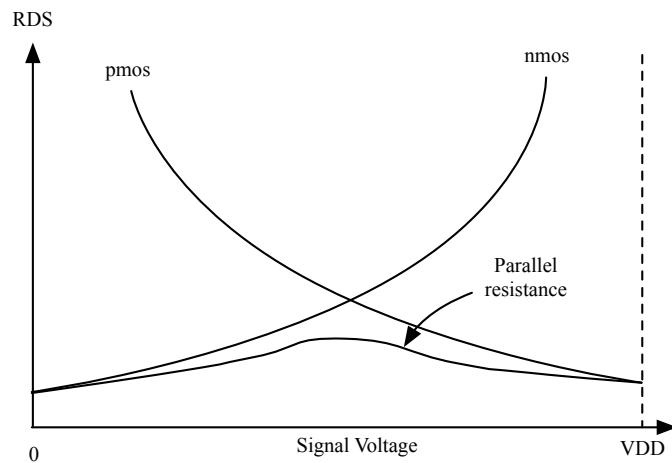


Figure 3-5 Characteristic On-resistance curve of CMOS transmission gate.

The transmission gate topology necessitates control signals and thus supply rails that are as large as the signal being transmitted. In addition to this, care must be taken to prevent a phenomenon known as latch-up [93]. Latch-up is caused by a parasitic bipolar transistor combination formed in the substrate. It forms what is known as a Silicon Controlled Rectifier (SCR) as shown in Figure 3-6. A SCR is a very useful component when used for purpose but, in the case of its parasitic formation in CMOS circuits, can lead to low conduction path from the supply to ground causing damage to the switch and other components.

Latch-up can be triggered when negative terminal voltages occur, which may happen on current phase transitions. This has been discussed previously in Section 1.3.2 and is particularly problematic when tissue is being stimulated, as the impedance is capacitive in nature, thus holding the voltage of one phase prior to reversal and leading to negative terminal voltages.

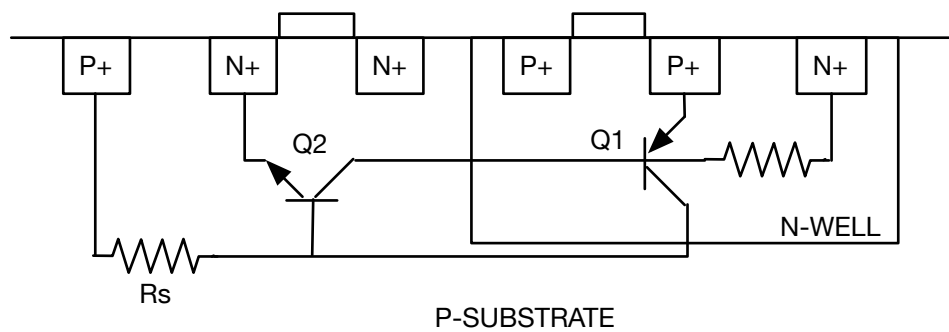


Figure 3-6 CMOS cross section showing parasitic SCR.

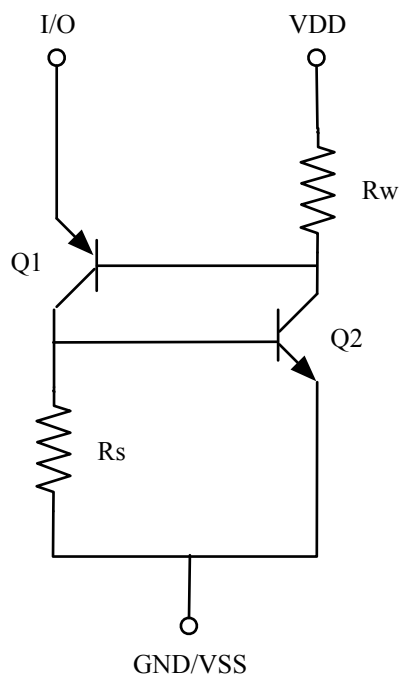


Figure 3-7 SCR circuit.

Layout techniques to reduce the gain of the SCR and guard rings can be used to prevent formation of the bipolar components. These are effective mitigation techniques that can readily be employed. However, as will be discussed, there are also circuit level design techniques to prevent latch-up from occurring.

Floating Gate

A technique known as bootstrapping or floating gate was of particular interest due to its ability to switch signals above the voltage of the switching control signal [104]. If the switch cell were able to be isolated from the substrate, this approach would enable switching of high voltage signals with low voltage devices reducing the need for large high voltage processes and even the possibility of using an entirely low voltage process. This technique is now readily employed in commercial ICs to manage signals beyond voltage rails. It is a topic worthy of lengthy discussion but will be kept brief as the implementation is complex and this approach was not taken in the end. This was largely because no easy method, after great efforts, could be found to satisfy concerns that latch-up would not be an issue. Using a process with galvanic isolation to the substrate could solve this issue but complicate others. In addition to this, the floating gate approach requires numerous control signals to function. Since XPAND is driven by asynchronous logic, with no central processor and hence clock source, the floating gate approach involved insurmountable challenges but will still be briefly presented.

The floating gate topology is shown in Figure 3-8 and works by first charging a capacitor C1 by enabling switches SW1 and SW3. Once charged, these switches are disconnected, and the capacitor is connected between the gate and source of the main switching transistor M1 by switching on SW2 and SW4.

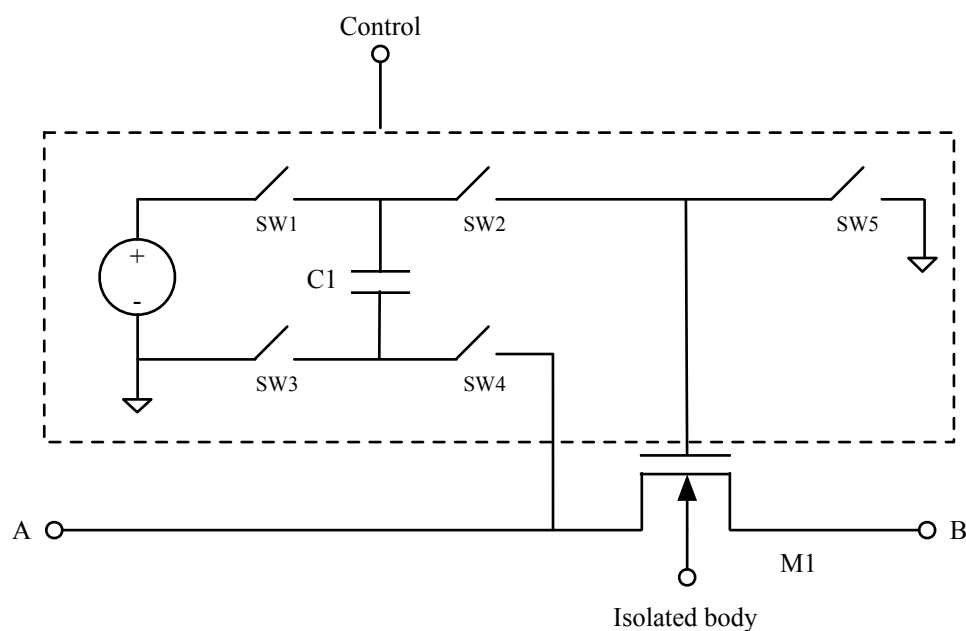


Figure 3-8 Floating gate switch cell.

With an isolated floating capacitor now applied across the gate-source of the main pass transistor, it remains switched on regardless of the input voltage. For example, assume terminal A is 10V. The gate voltage will just bump up to $10 + V_{C1}$ where V_{C1} is kept greater than the threshold of the transistor M1.

In practice, due to charge decay across C1, SW1/SW3 and SW2/SW4 are alternately switched to keep the charge topped up.

To switch off, all switches are opened except for SW5 which is switched on, grounding the gate.

What is abstracted in Figure 3-8 is the complexity around the substrate connections and the implementation of the switched circuit. As previously mentioned, this involves dozens of transistors and careful timing of control signals, which is difficult to achieve when the clock is simply derived from biphasic pulses.

Common Source Configuration

The common source switch, as shown in Figure 3-9 eliminates the body effect by enabling the body to be tied to the source of transistor. The body effect, as described earlier, will effectively increase the gate source threshold voltage and, therefore, limit the available swing. However, by tying the body of the transistor to the source, an additional diode is introduced via the substrate, which conducts when the source is higher than the drain. In effect, the transistor can no longer be switched off in one direction and so it is not bilateral in operation.

However, by connecting two sources, what one diode passes, the other blocks. This comes at the cost of an additional device and higher on resistance since the total on resistance is the sum of two transistors M1 and M2 in series.

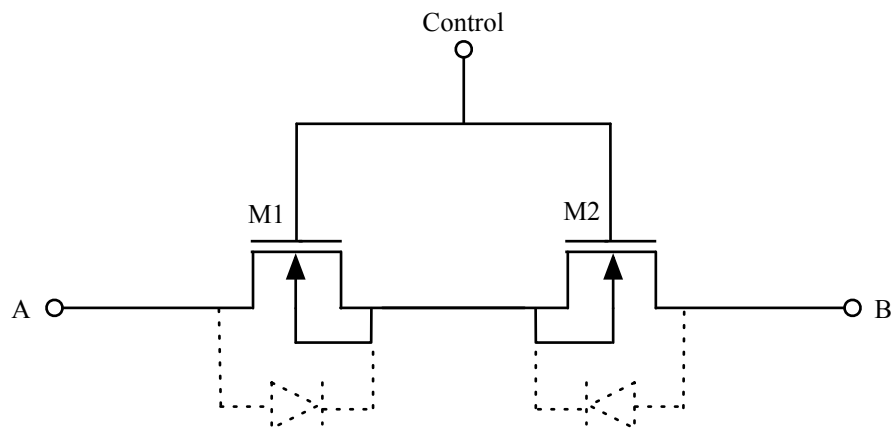


Figure 3-9 Common-Source Switch.

Transmission Gate with Body Cross Coupling.

We have presented three switch cell architectures. The transmission gate provides the easiest path from a design perspective but necessitates the use of high voltage transistors that are much larger in size. As it was decided that the floating gate approach would not be feasible within the constraints of this thesis, it was determined to press ahead with a high voltage transistor solution.

One unresolved issue with the transmission gate approach is the risk of latch-up. As discussed previously, this can be mitigated to some extent with good layout. However, there is a circuit layout technique that was eluded to in 3.2.1 and will now be presented.

Consider the circuit presented in Figure 3-10 and the transistors M1, M2 and M3. This configuration is known as Body Cross Coupling and gets its name from the fact that the body of the transistor M1 takes on the higher of the drain or source terminal voltage keeping the body at the highest potential, but not at the supply such that the body effect would occur. To understand how this works, consider terminals $A = 10V$, $B = 5V$ and $G = 0$. To start with, V_b will be established in the first instance via the body diodes (formed within the PMOS as shown in

Figure 3-11) and will be approximately equal to terminal A. Additionally, since terminal B is low compared to V_b , transistor M2 will turn on, hard pulling V_b all the way to terminal A. M3 will be fully off with its source and gate both at voltage A.

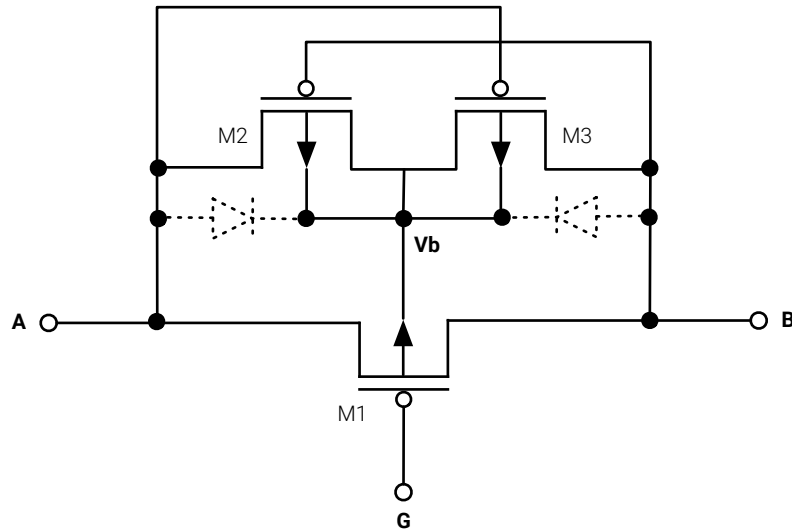


Figure 3-10 Modified transmission gate with Body Cross Coupling.

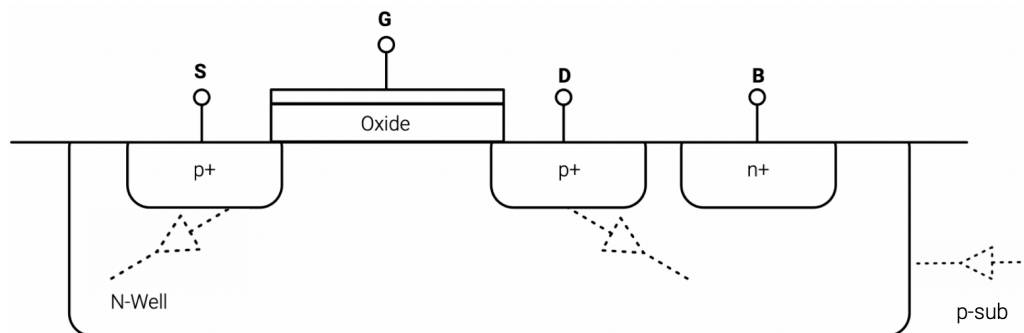


Figure 3-11 Cross section of standard PMOS device showing parasitic PN diode formations.

By extending this concept to include NMOS devices to create a transmission gate as previously discussed, for more constant conduction, the circuit can be drawn as in Figure 3-12. This, however, suffers a fundamental issue: the body of the NMOS is tied directly to the substrate and must, therefore, be tied to ground. For this reason, as shown in Figure 3-14, the Body Cross Coupling transistors on the NMOS are removed. Whilst the NMOS will still suffer from the body effect, this effect will be felt most around the lower signal swings (A and B terminal voltages) where M1 is most conductive.

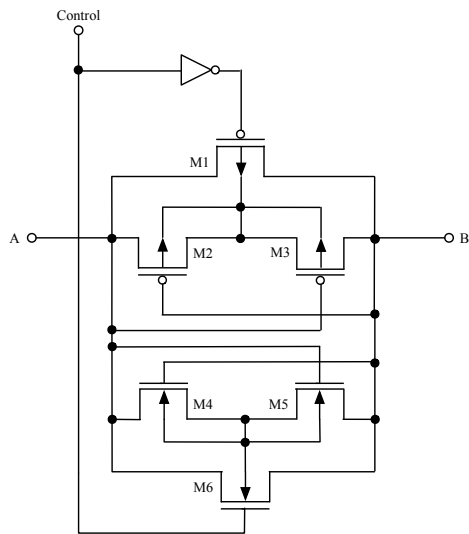
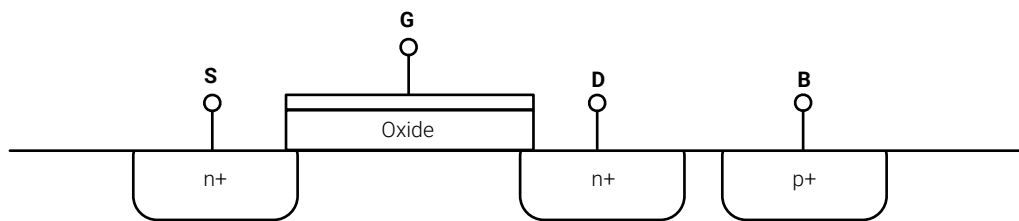


Figure 3-12 Modified transmission gate with Body Cross Coupling.



P - substrate

Figure 3-13 Standard NMOS device semiconductor cross section.

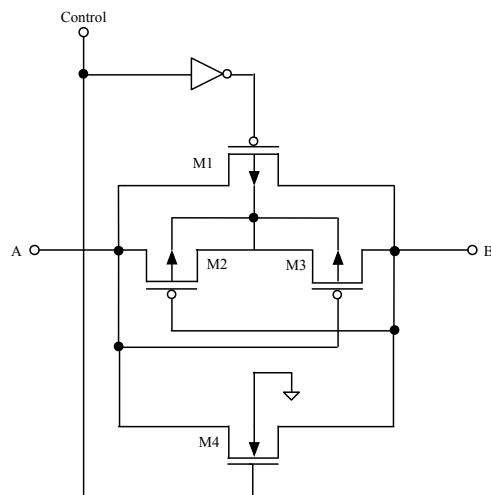


Figure 3-14 Transmission gate with Body Cross Coupling on PMOS.

One issue that remains unresolved from a circuit design perspective is the conduction that will occur through either the source or drain of M4 for voltages less than one diode drop than the substrate. This is due to the PN junction diode formed between the source-substrate and the drain-substrate as shown in Figure 3-11. Some leakage can be tolerated and it is most important that the gain of the SCR described in Figure 3-7 is minimised. Layout is the only remaining mitigation and can be used to limit the likelihood of latch-up substantially by for example spacing the NMOS at a distance from PMOS devices (increasing R) and by use of guard rings.

In summary, the topology in Figure 3-14 was chosen as the switch cell for the switch array as it provides a good compromise between the standard transmission gate topology but with better conduction at larger signal swings.

In order to control the switch cell, low voltage control signals (3.3V) need to be translated to high voltage control signals. This can be achieved using a high voltage level shifter. Shown in Figure 3-16, this circuit has what is often referred to as a cross coupled latch.

Assume a low voltage control signal CTR is asserted and _CTRL is not. M2 will switch on, which will turn on M3 whilst M1 is off, turning M4 off. These dynamics are very easy to see. However,

what it is very important that both CTRL and _CTRL are not asserted at the same time. If this occurs, both M3 and M4 will conduct and “shoot-through” will occur. To prevent this from occurring, non overlapping CTRL signals are required and the control signals should not be independently controlled. That is, asynchronous logic guaranteeing CTRL and _CTRL are the inverse of each other is necessary.

In addition to this, the voltage on the CTRL and _CTRL lines cannot change instantaneously. If they do, the state that the circuit will be in under the condition where CTRL and _CTRL are equal as illustrated in Figure 3-15. This situation can lead to partial conduction of both branches and lead to transient shoot-through currents on state transitions. One additional method to minimise the chance of this occurring is by skewing the branch conduction, say by widening M1 and M4 transistors. This alters the transition point and minimises shoot through dramatically.

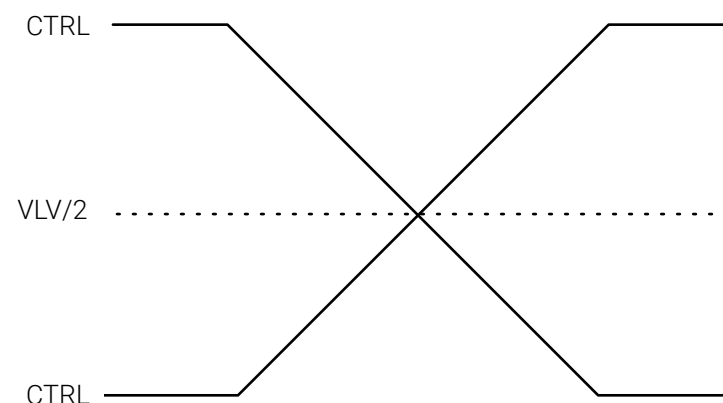


Figure 3-15 The simultaneous transition slope leading to partial conduction state when both CTRL and _CTRL are mid supply.

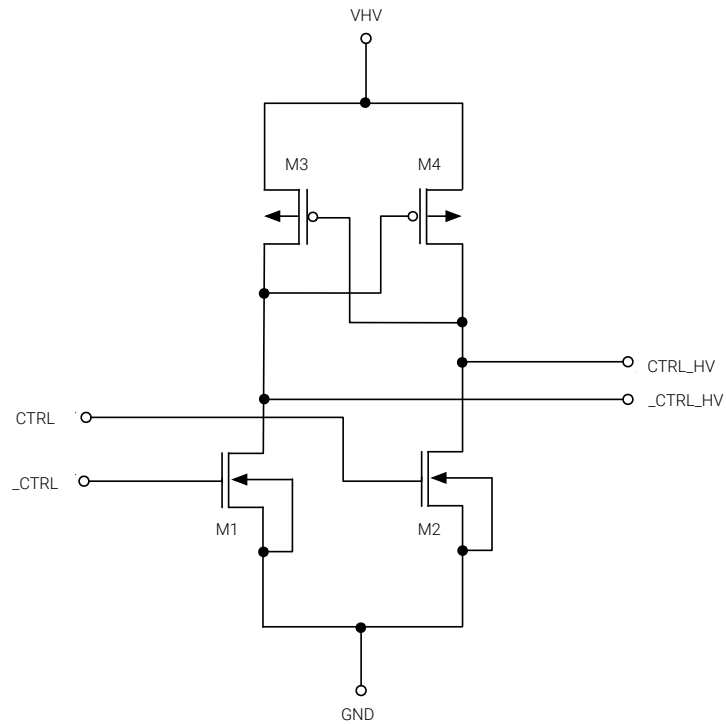


Figure 3-16 High voltage cross coupled level shifter.

Simulation of the on resistance for Figure 3-14 for NMOS and PMOS devices is illustrated in Figure 3-17. This graph shows the change in resistance of the switch for different input signal levels. The resistance is not monotonic with signal level as expected, since the NMOS device is low in resistance for low signal levels (when the gate-source is highest) and vice versa for the PMOS.

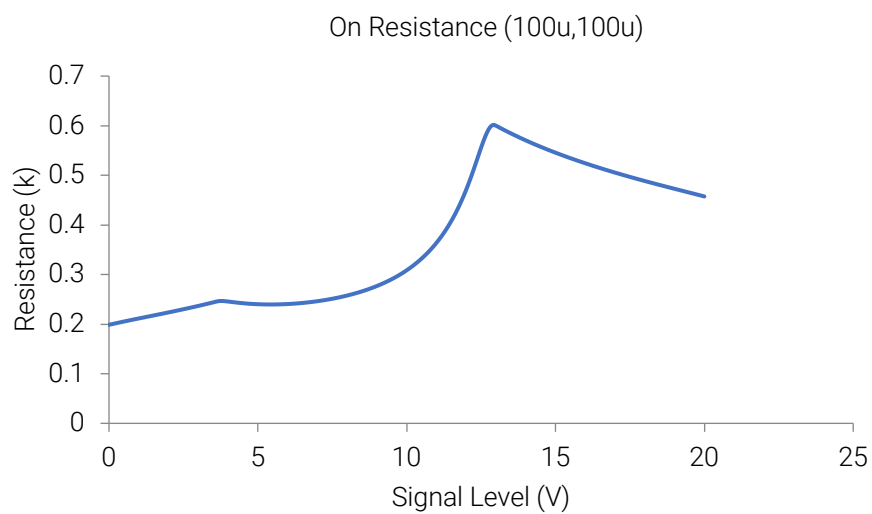


Figure 3-17 Simulation of on resistance for the proposed modified transmission gate.

3.2.2 Addressing switch array

So far, the switch cell and control circuitry has been described. It is now time to look at the final element of the switch array: the register that stores the configuration of the switch array. For flexibility, individual control of each switch cell is required. This necessitates a register equal in length to the number of cells required to be programmed. In the case of XPAND, this is $6 \times 64 = 384$.

The register, which will be described as the input frame register, must receive a serial stream of 1s and 0s and then, once full, transfer them to an output register that controls each cell. In essence, what is being described here is a serial shift register and a parallel buffer. This common configuration is shown below in Figure 3-18 and comprises an array of D flipflops. This topology is now synchronous in the sense that it is dependent on a CLK rising edge state transition to change output; however, the CLK is simply a delayed version of the rectified biphasic pulse. For a D flipflop, the output value is simply equal to the input value on the rising edge of a clock transition.

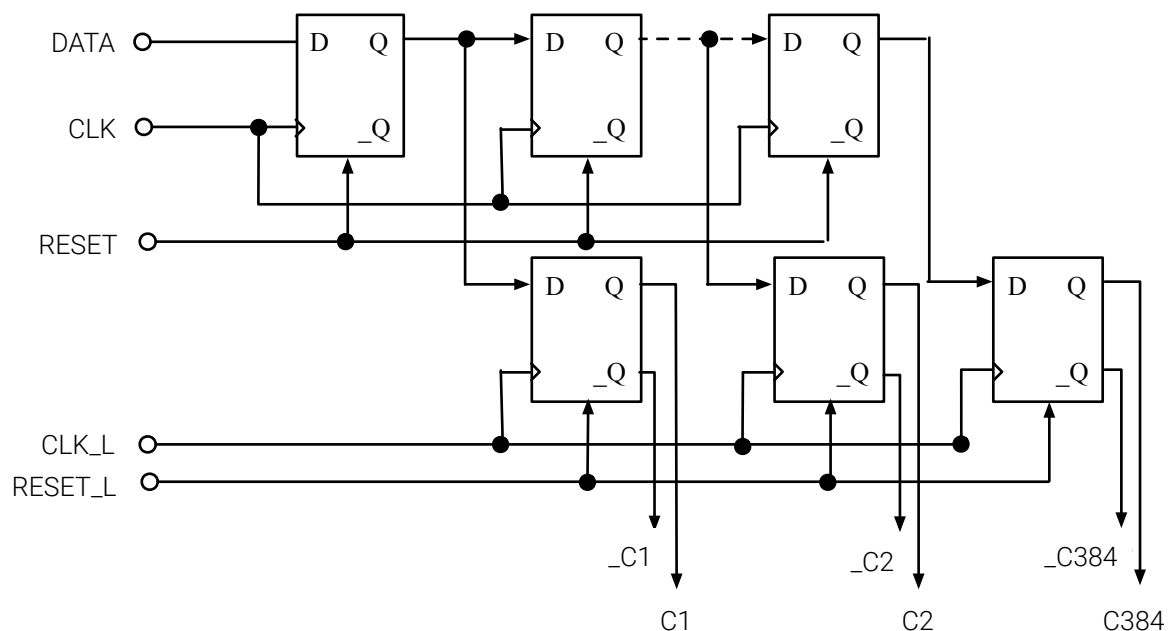


Figure 3-18 384-bit shift register with load buffer.

3.3 Pin Casting

One of the biggest design challenges in the implementation of XPAND was managing the power and communication lines. As discussed in Section 2.3.3, it is desirable for any of the input lines to be cast as power and communication on start-up. The motivation for this is that this would greatly improve redundancy in the event of a wire breakage, which is a real possibility for high density arrays.

The architecture formulation was challenging due to the nested and integrated nature of the start-up phase. That is, on the one hand, the input lines must be preserved for stimulation and recording; on the other hand, they must be capable of deriving power and communication. Detangling these requirements required some conceptual leaps rather than a more conventional architecture design based on the use of standard functional blocks, which are then specified and designed.

The final architecture for pin casting is shown in Figure 3-19. At least two pin casting cells are required for operation; i.e., a minimum of two leads to provide a return path for the stimulator. With that said, for the purpose of analysis, only one cell will be studied.

The Pin Casting cell has two modes. When it is not cast as a power and communication line, it provides a direct line through to the Switch Array. Almost all the electronics are disengaged except for the demodulator line, which is very high impedance. When it is cast as a power and communication line on start-up, a main switch SW1 is latched closed providing a low impedance path to the main storage capacitor C2.

In this section, the pin casting circuit will be discussed in the context of its phases of operation. A good starting point for this is exploring how power is established in the first place.

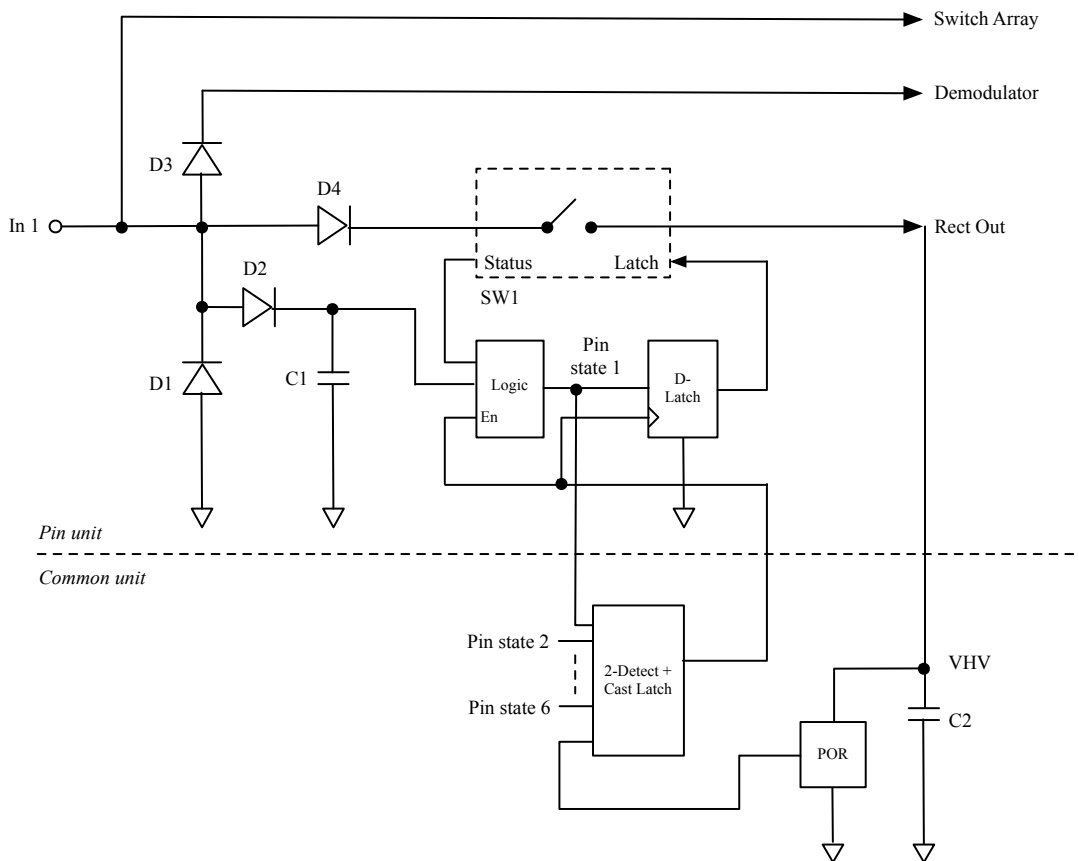


Figure 3-19 Complete Pin Casting architecture.

3.3.1 Establishing Power

When the first biphasic stimulation pulses are applied to the XPAND chip, the current signal interacts primarily with the rectification circuits as discussed in Section 2.3. If interaction with the switch array and demodulator is excluded, this leaves a full wave rectifier, as shown in Figure 3-20. What is critical to the operation on start-up is that the main switch is not in an off state. To show how this works, the switch control circuit must be discussed. For now, assume that the switch will not be in an off state on start-up. If this is the case, C2 will be charged via D2 and D3 on the Anodic phase and D4 and D1 on the Cathodic phase, as illustrated in Figure 3-21.

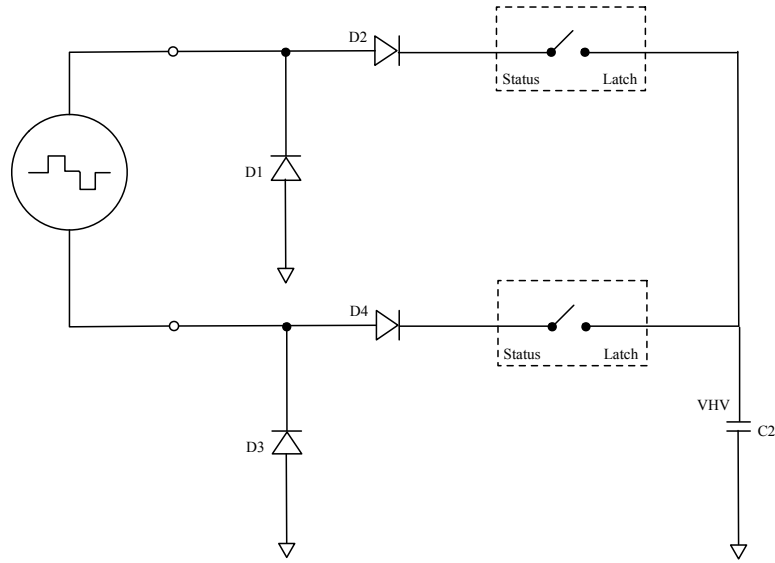


Figure 3-20 Full wave rectifier on Start-Up via leaky switches.

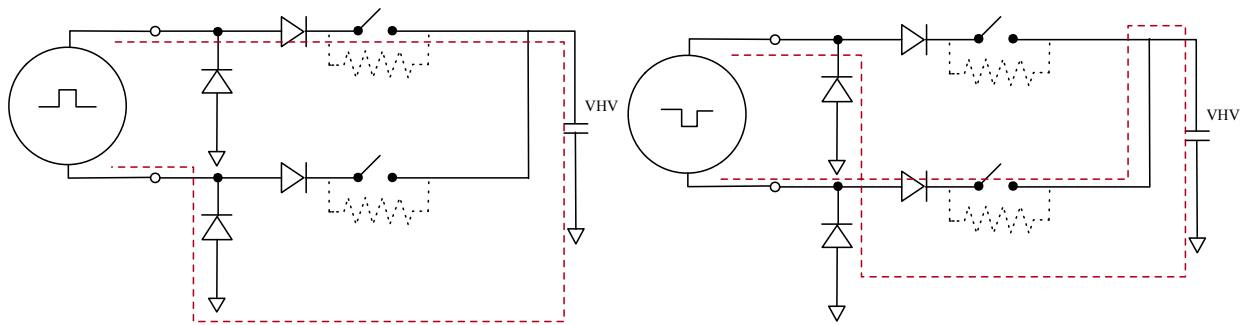


Figure 3-21 Charging of high voltage capacitor on Anodic phase (left) and Cathodic Phase (right).

High voltage diode devices were not available in the process technology of choice. Instead, HV PMOS devices were tied in diode configuration as shown in Figure 3-22. For reasons previously discussed, Body Cross Coupling techniques were used to ensure the body of the PMOS was kept at the highest potential. This is essential on start-up.

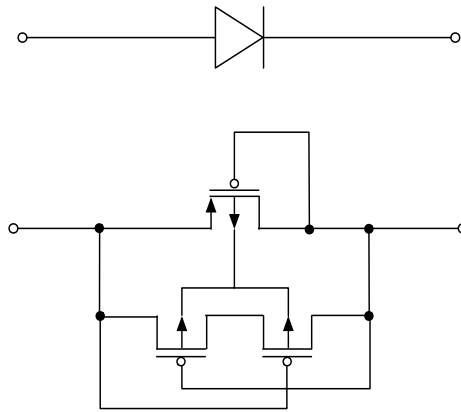


Figure 3-22 Diode connected PMOS with Body Cross Coupling.

The method by which power is initially delivered and stored on C2 has now been discussed. Next, the POR circuit critical to establishing power to logic is discussed.

3.3.2 Power On Reset

As the voltage of C2 is charging, it is essential to keep the rest of the circuitry disconnected from power until it reaches a sufficiently high voltage. If this were not the case, circuits could easily enter meta-stable states causing the chip to malfunction in the best case and cause damage in the worst. To resolve this issue, a circuit called Power On Reset (POR) can be used. PORs wait until the supply is at a sufficiently high voltage before enabling chip logic.

The topology of the POR is shown in in Figure 3-23. M1-M4 are two inverters connected to each other forming a latch. This is illustrated in Figure 3-24. The binary state at the output of each inverter must be opposite, but once it is established, it cannot be unlatched.

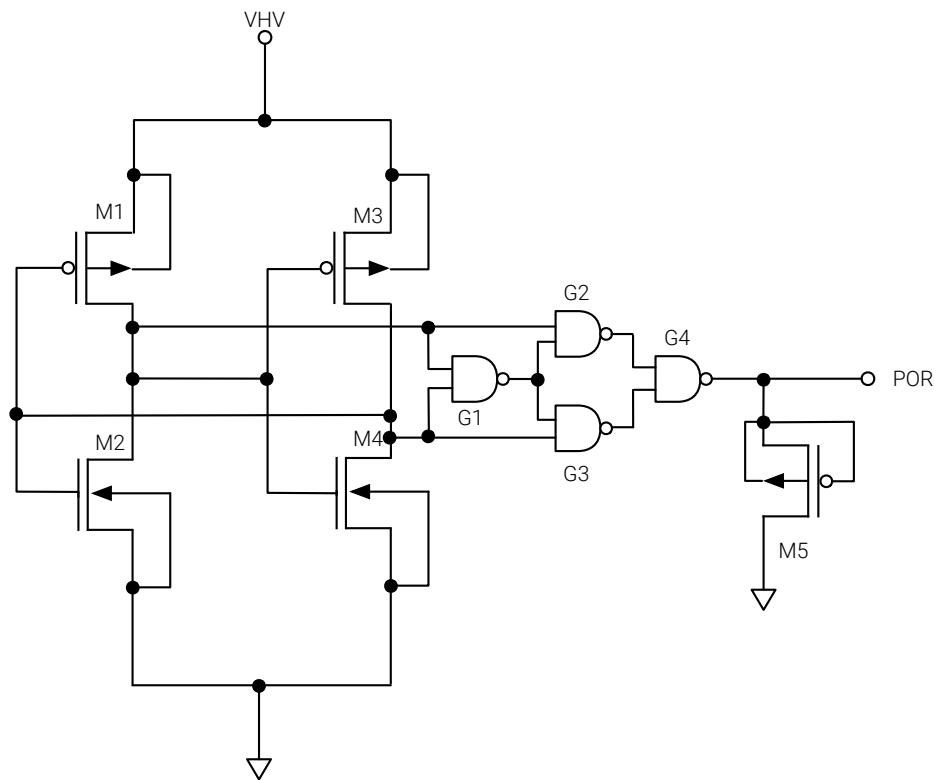


Figure 3-23 Power On Reset (POR) circuit.

The logic formed by NAND gates G1-G4 is equivalent to an XOR gate such that the POR signal is only asserted when the latch formed by M1-M4 reaches a stable state. The voltage at which this occurs is mostly a function of the transistor threshold voltages, which for the high voltage devices will exceed that of the smaller low voltage devices. M5 is a diode connected PMOS, which helps to keep the POR signal low prior to the latch reaching stable state.

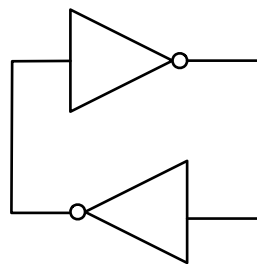


Figure 3-24 Simplified Power On Reset (POR) diagram.

A simulation of this circuit of the POR is shown below in

Figure 3-25. The green line represents the climbing supply voltage as biphasic current pulses are rectified and stored. The pink line represents the POR output signal. As the supply voltage

begins to climb, the output of the POR is kept low by M5 while the transistors in G4 are all off. At around 640 us, the M1-M4 begin to conduct and the loop quickly converges to a state due to the high positive feedback of the inverter loop. Since the output value of both inverters must be opposite, the XOR will assert when this is the case. The POR signal is then used to switch power on to the full XPAND circuit.

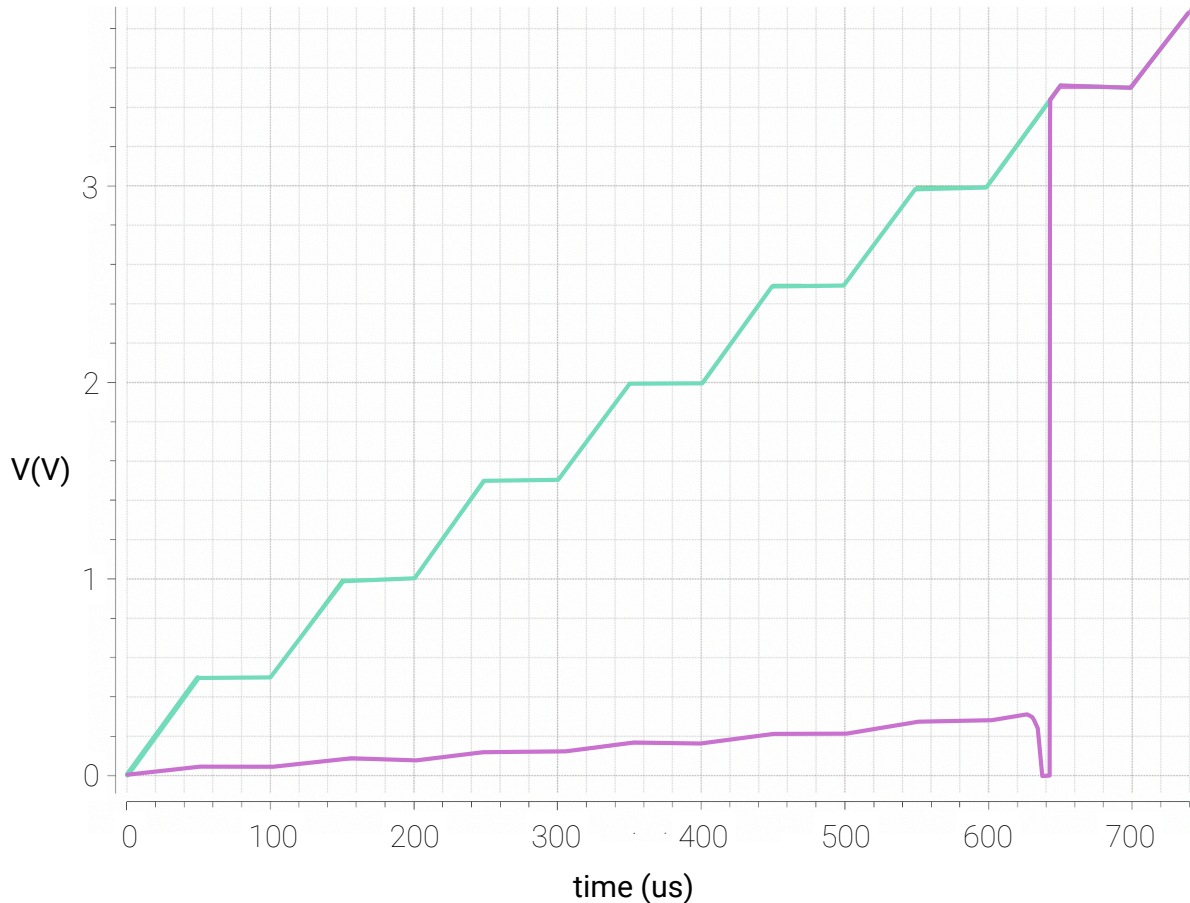


Figure 3-25 Simulation showing the POR start-up phase. Green indicates the supply voltage and pink indicates the POR output.

3.3.3 Casting

With power established and the POR activated, the 2Detect logic becomes active. The 2Detect circuit is shown in Figure 3-26.

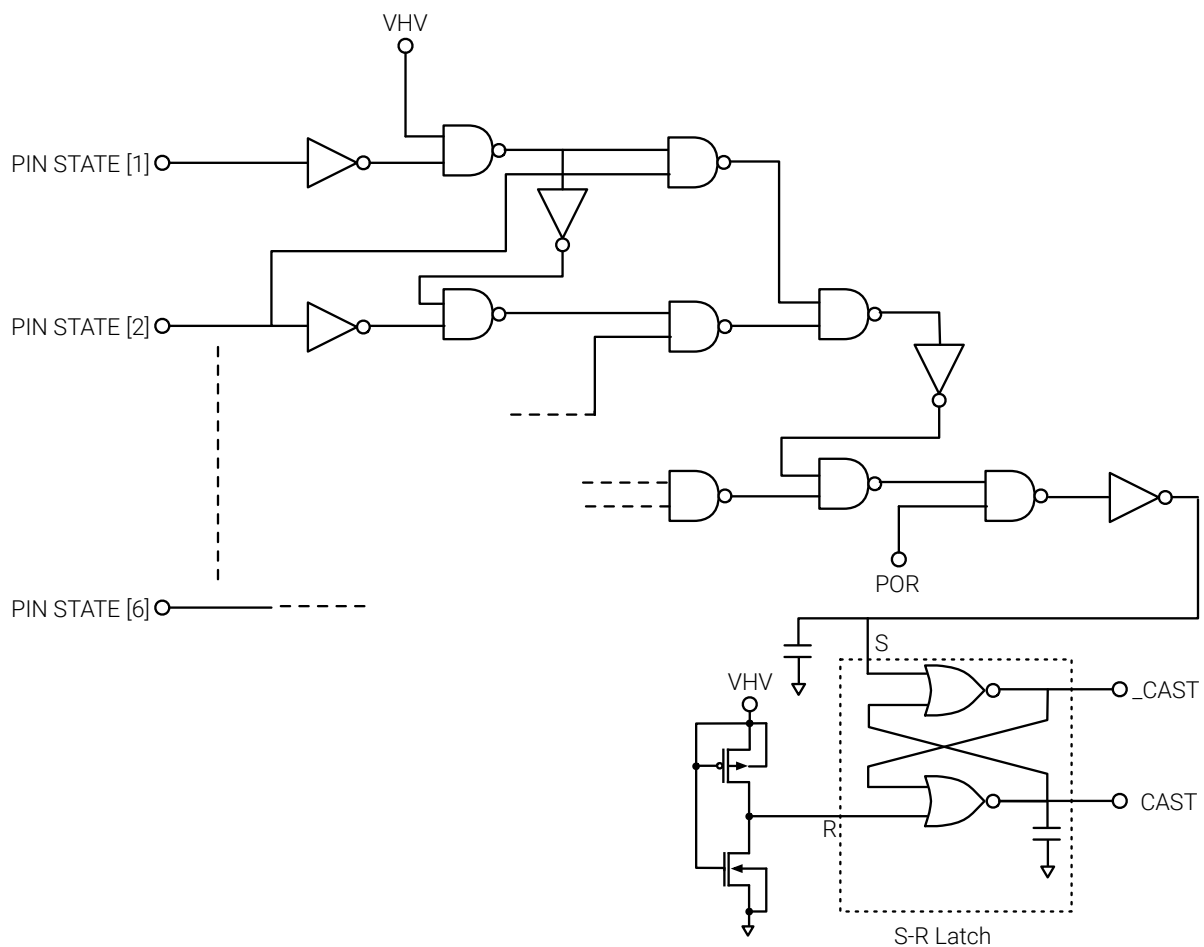


Figure 3-26 2Detect logic block responsible for activating casting.

The 2Detect circuit creates a trigger signal when any two input pins are high, and the POR is asserted. The Pin State is high on the pins used to establish power to the XPAND. It results from D2 and C1 as shown in Figure 3-27, which are charged as power is delivered. Pins not used to “prime” the XPAND will have a low Pin State. This trigger signal “Sets” an S-R Latch. The S-R latch reset terminal R is held low by a two-transistor circuit which holds the R low on start-up with the minimum of bias current. It is essentially an inverter tied to supply. Capacitive loading on the CAST and S terminals of the latch ensure the latch is in a primed state ($S=0$) and that in this state it is falling into a state whereby the CAST is low. Without this capacitive loading there is a 50% chance all things equal that it could start with CAST high which was not desired. The capacitive loading was chosen to be of similar value to the gates within the latch, and further simulated to ensure reliable performance.

When the 2Detect asynchronous logic asserts the S pin, a CAST signal will be asserted and latched.

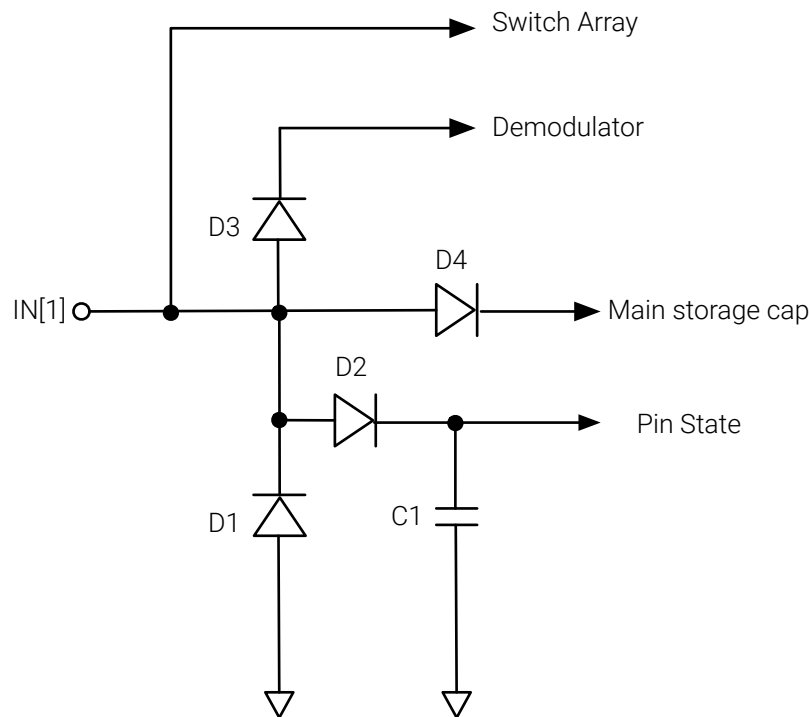


Figure 3-27 Pin State detection circuit.

3.3.4 Pin Switch Casting

The power up sequence, POR and casting have now been discussed. Next, the actual latching of the pin state will be explored.

Figure 3-28 shows the full switch module denoted SW1 in Figure 3-19. The main pass switch is M3 with Body Cross Coupling formed by M1-M2. As discussed earlier, the switch must not be in an off position in start-up. M4 is configured as a capacitor and helps to keep the gate of M3 low on start. It does this by virtue of the fact the capacitor needs to be charged to have a voltage and there is no direct charging path and, hence, it retains the value of approximately 0. In a similar fashion, diode configured transistors M5 and M8 create very high impedance paths to the high supply side and ground, respectively. This helps to ensure the correct initial state of the cross-coupled level shifter formed by M6, M7, M9 and M10.

When the cast signal is asserted, the pin state is effectively sampled and latched by G1-G4, which form a NAND latch. If Pin State is high, a high signal is provided to the gate of M7 that, when turned on, pulls M3 low, switching it on hard. The pin is then cast to its function of power and communication.

Alternatively, if the Pin State was sampled low, this would imply that the Pin in question was not used to power up the XPAND. This would cause a low signal on gate of M7 and high on the gate of M8. This would, in turn, pull the gate of M3 essentially to the body potential, which via Body Cross Coupling will be equal to the higher of the drain or source of M3. In other words, M3 is switched off and hence the input line is isolated from the power and communication circuitry such that it can pass through to the switch array without interference for either recording or stimulation.

It is worth noting that the level shifter taps its high voltage supply from the Body Cross Coupling circuit of M1 and M2, which guarantees that the gate is always held at the highest voltage applied to the switch, be it on the storage cap side or the stimulator side. Since the stimulator voltage will often exceed the stored voltage, this was an important consideration.

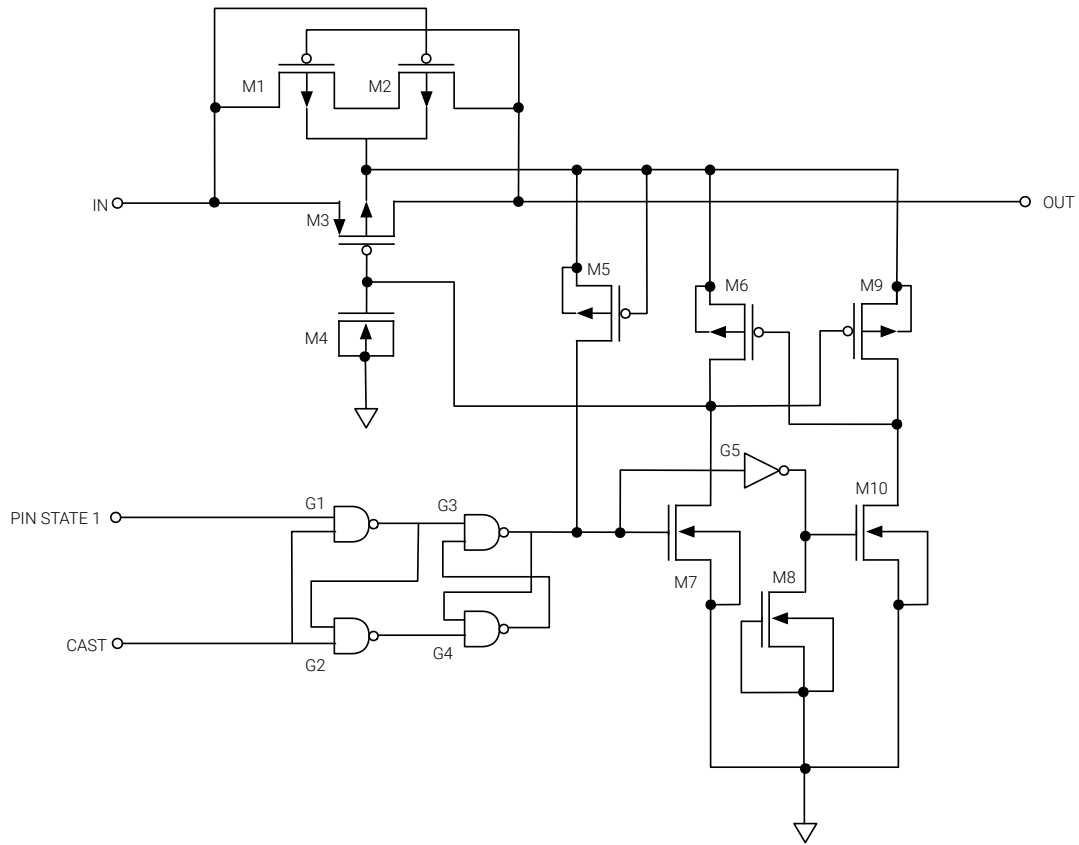


Figure 3-28 Pin State latching.

3.3.5 Four input simulation

Simulation of pin casting was performed by modelling a biphasic current source that was switched in using simulated relays to model the isolated nature of the configuration. Convergence issues were often a problem for these simulations as can be the case with current mode simulation. That is, for a finite controlled current, for very high impedance states the voltage will also be really high. To get around this, a compliance voltage switching circuit was added to the current source such that it would clip, as would occur with a real stimulator with a finite supply voltage.

Figure 3-29 shows the actual Cadence circuit model used, which is abstracting transistor level circuitry that became too unwieldy for these kinds of simulation. The simulation results, shown in Figure 3-30, show the POR being asserted in pink and then the bifurcation of casting state for two separate input lines, one that was used to power up and the other that was left floating, shown by the green and blue lines respectively. At around the 500us point, one is driven to the

Figure 1 is a line graph showing the voltage ($V(V)$) of the enable line and the cast signal from the POR over time (ms). The x-axis ranges from 0 to 0.5 ms, and the y-axis ranges from 0 to 3 V. Three traces are plotted:

- Cast signal from POR (purple line):** This signal rises in steps, reaching 3 V at approximately 0.45 ms and remaining at 3 V until 0.5 ms.
- Enable line (setting to power/com) (blue line):** This signal rises in steps, reaching 1.2 V at approximately 0.35 ms, then 2.5 V at approximately 0.45 ms, and finally 3 V at approximately 0.5 ms.
- Enable line (setting to stim/record) (green line):** This signal rises in steps, reaching 1.4 V at approximately 0.35 ms, and then drops sharply to 0 V at approximately 0.45 ms.

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3.4 Power storage and regulation

Power storage and regulation is a standard functional block of many CMOS integrated circuits. What made this design challenging was the extremely low power consumption required.

3.4.1 Supply Independent Nano-ampere Current Reference

The Bias currents in the demodulator, frame detector and delay unit are all derived from the voltage reference. They rely on precision voltage generation that needs to be largely independent of the supply to account for different supply voltages and fluctuations due to droop. In addition to this, as it is one of the only circuits in XPAND that necessitates static current, efforts to make this current as small as practically possible were made.

Generation of a bias current that is independent of the power supply voltage is ubiquitous in analogue electronic circuits [97]. The design of circuits that can produce nanoampere currents efficiently is particularly critical in ultra-low power systems, such as implanted devices and sensor networks. A popular solution to the problem, shown in Figure 3-31, is to use a positive feedback loop that forces an equal drain current through two weakly inverted MOSFETs with a W/L ratio of 1:K.

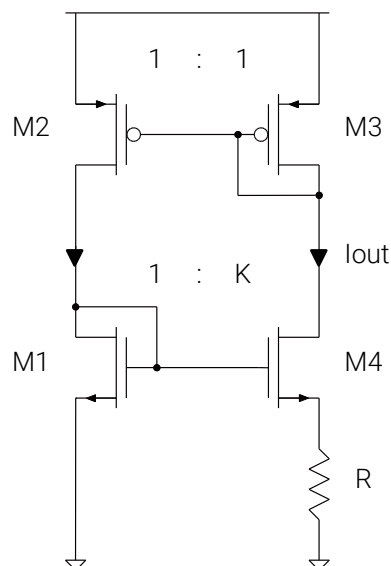


Figure 3-31 Schematic of conventional current reference.

In this circuit the current is given by,

$$I_{OUT} \propto \frac{1}{R^2} \cdot \left(1 - \frac{1}{\sqrt{K}}\right)^2, \quad (3-5)$$

which is independent of the supply. One drawback of this approach is that it will consume exactly twice the current that is desired since branches of M2 and M3 are mirrored because they both have the same gate source potential and transistors are assumed to be identical. Thus, this configuration effectively consumes twice as much power as theoretically needed.

The inefficiency can be overcome with the circuit shown in Figure 3-32, where M3 is scaled in size by S and M4 is scaled by SK. This reduces the total current consumption to $I_{ref}(1+1/S)$ at the cost of increasing component spread to SK. Since threshold mismatch between such transistors directly adds to the ΔV , and is dominated by the smaller geometry element, unit device area must be increased by a factor S to maintain current accuracy, which increases the accuracy-area occupation trade-off.

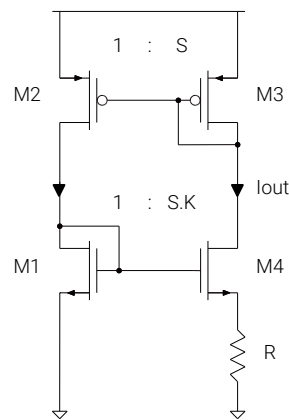


Figure 3-32 Scaled branch current reference.

A modification to this circuit, which forces equal current through the resistor R, and hence equal I_{out} but with lower component spread, is shown in Figure 3-33.

It can now be shown that the proposed current reference has identical loop gain and hence to first order Power Supply Suppression Ratio (PSRR) to the topology it replaces. To calculate the loop gain, we cut the loop at the gate of M4 in Figure 3-33. This gives,

$$V_s = g_m \cdot (V_p - V_{s2}) \cdot (1+S) \cdot R \quad (3-9)$$

$$I_1 = \frac{g_m}{g_m R(1+S)+1} V_p \quad (3-10)$$

$$T = \frac{1}{g_m R(1+S)+1}. \quad (3-11)$$

Also,

$$g_m = \frac{q I_1}{n K T} \quad (3-12)$$

$$I_1 = \frac{n K T}{q R(S+1)} \log(K). \quad (3-13)$$

Substituting Eqs. 3-14 and 3-15 into the loop Eq. 3-16, the loop gain is found,

$$T = \frac{1}{\log(K)+1}. \quad (3-17)$$

This value is identical to that obtained by the conventional solution. Notice also the value is positive and less than 1, as expected for stable positive feedback.

The final nano-ampere current reference is shown in Figure 3-34. Note that C1, M1 and M4 form a basic start-up circuit that helps to get the loop going when 3.3V is switched on. When the supply is switched on, M4 will begin to conduct as the capacitor will have 0 V across it. This turns on PMOS and NMOS transistors in the reference. As M1 begins to turn on, it will charge C1, which will eventually turn M4 off. C1 will charge to a saturation point and, whilst M1 will be on, no current will flow.

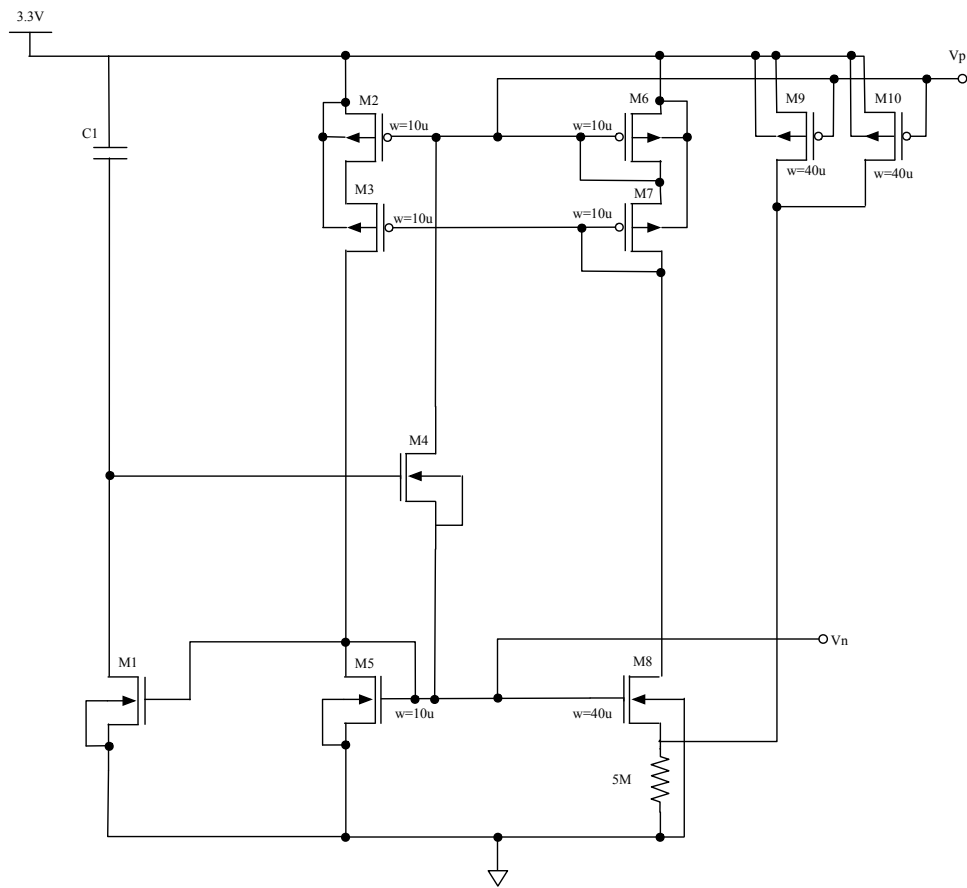


Figure 3-34 Supply independent nano-ampere current reference.

3.4.2 3.3V Regulator

Stimulators often have high compliance voltage to allow delivery of charge to high impedance tissue interfaces. As such, XPAND was developed on a high voltage CMOS process with devices that can handle up to 20 V. That said, these devices are physically large in size in terms of their silicon footprint and will consume more power due to leakage for this reason. Therefore, it was desirable to establish a low voltage supply for low voltage logic. A standard linear regulator topology is shown below in Figure 3-35. Essentially, the OTA will control the voltage on the gate of M1 such that the output is equal to the reference voltage delivered to the positive terminal of the OTA.

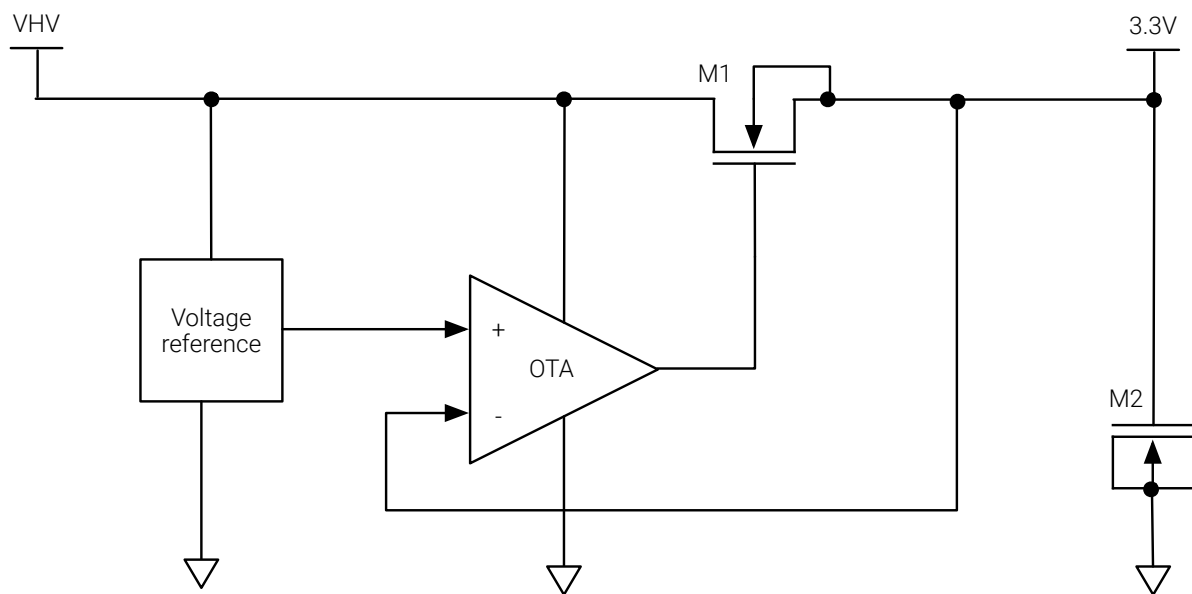


Figure 3-35 Architecture of standard linear voltage regulator.

There were two major design aspects to the voltage regulator. The first was the low power Voltage Reference and the second was the design of the OTA. The reference provides a stable 3.3V, but also can provide the reference voltage for the OTA's own internal current source.

The complete linear voltage regulator is shown in Figure 3-36. Starting with the bias generator/voltage reference, the operation is very similar to that of the nanoampere supply independent current reference described in detail in Section 3.4.1. There is, however, a key difference: the use of stacked diode connected NMOS devices that convert the branch current into the reference voltage. Each transistor is connected in diode configuration with a fixed current flowing through that is set by the reference circuit. The voltage across each drain source will simply be equal to the gate-source voltage, which will reflect the required VGS to “match” the I_d in subthreshold. This results in a voltage approximately equal across each device and device sizes and count were simulated to generate the 3.3V required. Variation in supply voltage due to device variation was tolerable as the bias currents for the demodulator (which is the only analogue module powered by the 3.3V supply) are derived from the high voltage current reference.

Of important consideration in this design is the body effect. If the body of the transistors were simply tied to ground, the conduction characteristics would no longer be symmetrical across devices. For this reason, isolated low voltage NMOS devices were used. These devices are contained within a deep N region (DNTUB), which is held at the highest potential. Using these devices, the NMOS device bodies can simply be connected to their source which can be greater than zero volts. This essentially eliminates the body effect.

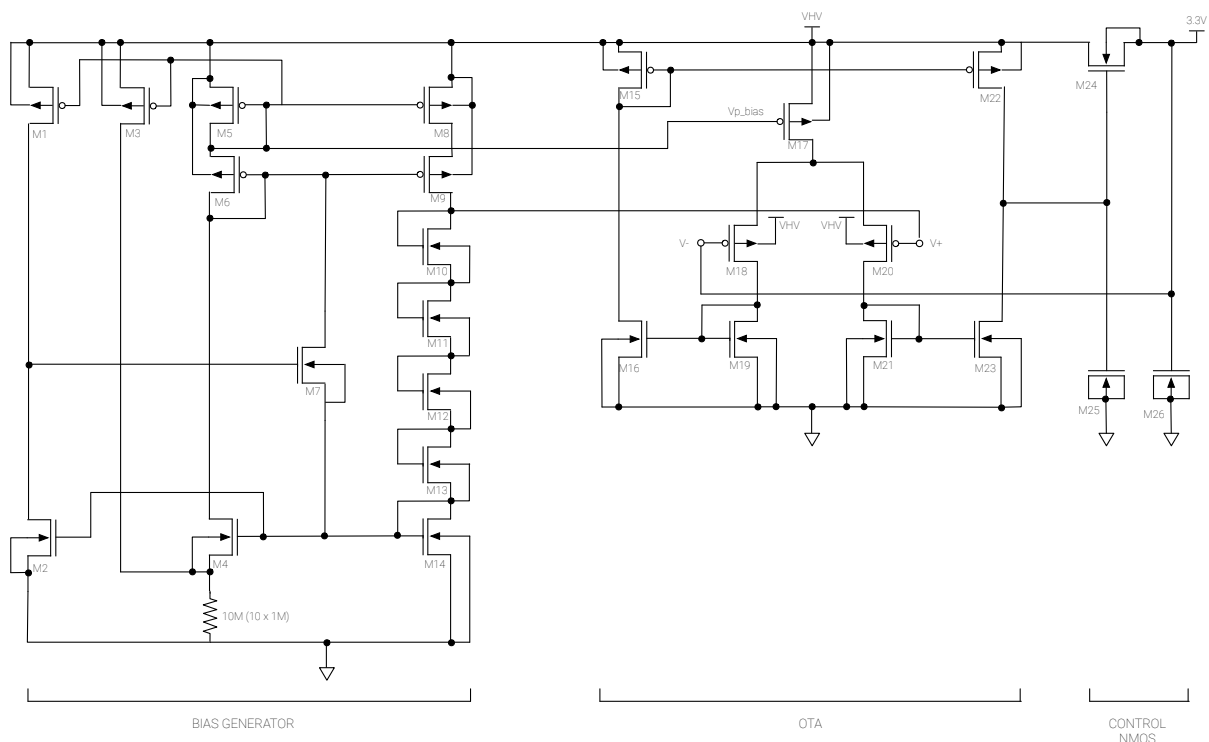


Figure 3-36 Ultra low power 330nA linear voltage regulator.

The OTA is biased by M17, which acts as a current source sized to mirror the current of the reference. In this way, the reference is providing both the voltage reference and the bias voltage for the OTA. M18 and M20 form what is known as a differential pair. Terminal V₊ is tied to the top of the transistor stack, which is set to 3.3V. The output is measured through terminal V₋, which controls M18. If the Output is, say, 10V, M18 will be on less than M20 and more current will flow down the M20 branch than M18. This is mirrored to M22, which becomes less conductive, and M23, which becomes more conductive, which lowers the voltage on the gate of the Control NMOS M24 thus reducing the voltage. This is a simplistic and intuitive description of the operation. In reality, aspects to consider include issues of matching that

cause offset and error, as well as the gain, which is important to settling time and stability. This design is completed analytically and, of course, through simulation to size the transistors appropriately.

3.5 Biphasic Pulse Demodulator

As discussed in Section 3.5, there are numerous ways to encode binary information into biphasic stimulation pulses. Configuration of the switch array is sent in data frames. In this work, a data frame is defined by a Start of Frame (SOF), Configuration Bits (DATA) and End Of Frame (EOF).

While encoding was discussed in previous chapters, it was decided to instead just implement a shift register of length 384 for first iteration and save the encoding block for a future chip iteration in the interest of time. The chip was already substantially large and complex to layout.

An example of the data frame implemented is shown in Figure 3-37.

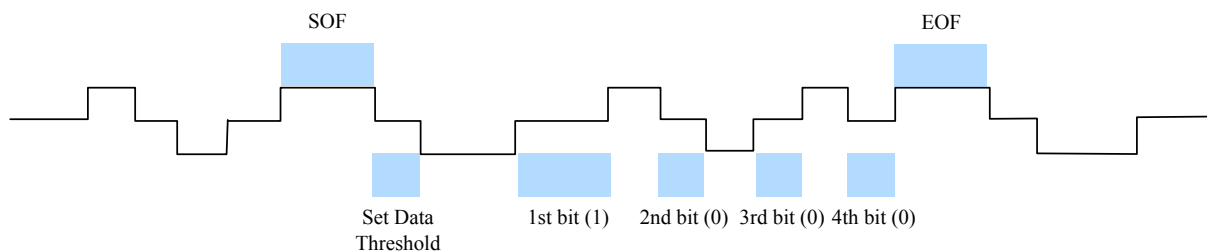


Figure 3-37 Biphasic stimulation pulses modulated according to protocol established in 2.4.

The demodulation state transitions is summarised in Figure 3-38.

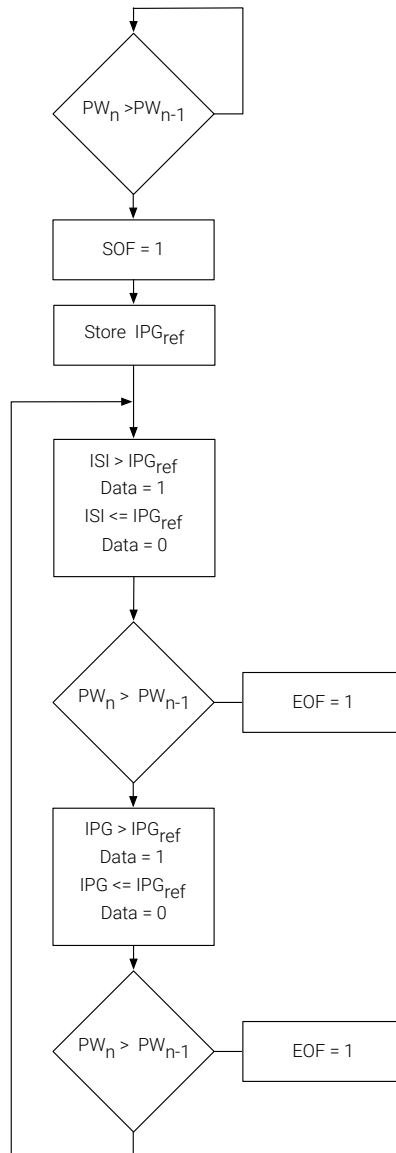


Figure 3-38 State diagram of Biphasic Stimulation Protocol.

Start Of Frame (SOF)

The SOF is detected when the pulse width is longer than the previous pulse. By making this relative rather than absolute, the XPAND can work with a wider variety of stimulators. The minimum detectable SOF width is limited essentially by noise and offset of the comparator in the detector circuit, which is approximately 50mV, and the maximum width is limited by the input voltage range of the comparator. Very safe margins can be used to relax analog design constraints to be optimised for power consumption. Power and configuration data should always be transmitted with the stimulator's minimum pulse width to maximise the transfer rate.

It should also be noted that the SOF is always a larger pulse width as compared to the data pulses since they occur less frequently, and this maximised the transmission rate.

Configuration Bits

Data is encoded via modulation of the Interphase Gap (IPG) and the Interstimulus Interval (ISI) relative to the SOF IPG. That is, the threshold width is set by the IPG of the SOF pulse. This again means that modulation of data is not fixed to any absolute width but can rather be programmed on the SOF. To maximise throughput, this width should be as small as possible.

Two bits per biphasic pulse can be reliably delivered by modulating the IPG and ISI. Smaller than the SOF IPG encodes a 0 and larger encodes a 1.

End Of Frame (EOF)

The EOF simply works the same as the SOF but in the opposite direction. That is, when the previous pulse width is smaller than the current one, EOF is detected.

The architecture and design of the biphasic communication circuitry will now be described.

3.5.1 Biphasic Demodulator Architecture

Four key blocks are required to transform the biphasic pulse stream to a data stream and clock that can be used to program the switch array register. These are summarised below:

Pulse Generator:	Deconstructs the biphasic pulse into a collection of useful signals
Frame Detector:	Demodulator circuit for SOF and EOF
Data Pulse Train:	Generates the data signal contained within frame
Data Demodulator:	Demodulator circuit for the DATA

For reference to the design work presented herein, these steps are broken out into function blocks in Figure 3-39. A core architecture that is used in both the frame detector and data demodulator is the pulse comparator and before discussing the four blocks to the biphasic demodulator, it will be described.

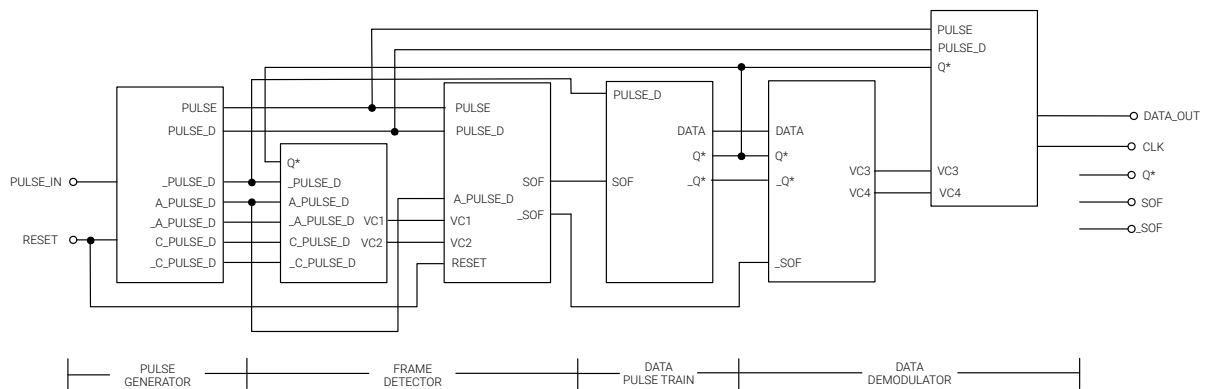


Figure 3-39 Complete demodulator system.

The architecture of the pulse comparator is shown in Figure 3-40. When switch A is on and current is routed through capacitor A, this results in a linear charging of capacitor A to a voltage that is determined by the time switch A is on.

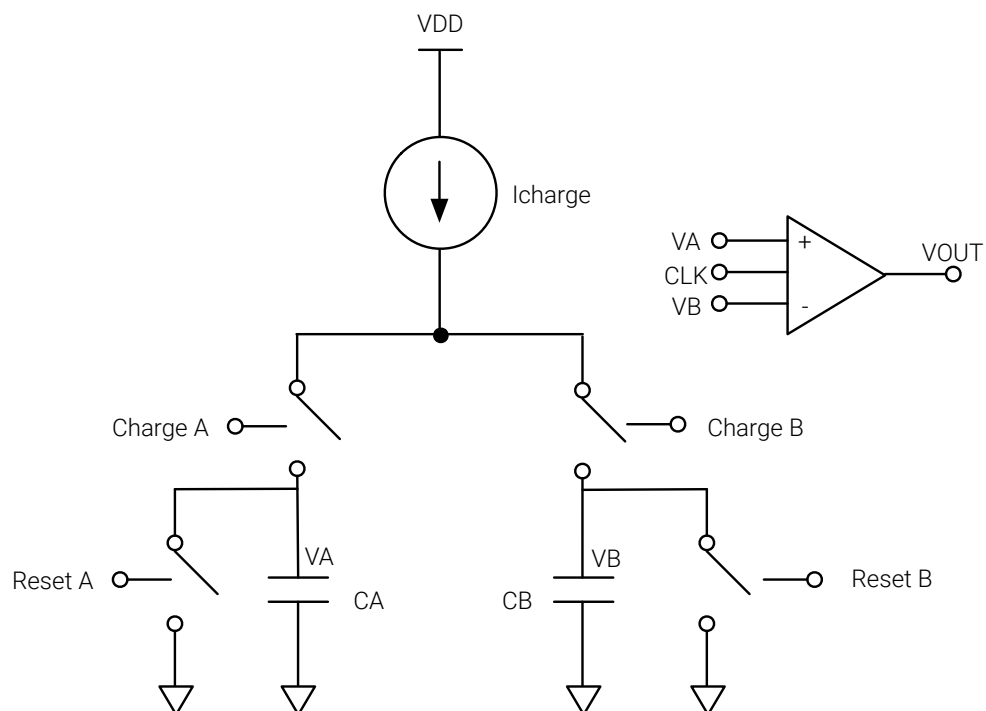


Figure 3-40 Architecture of pulse comparator.

The resulting voltage is given by

$$V = I_{\text{charge}} \cdot T_{\text{on}} / C. \quad (3-18)$$

Reducing the charge current to reduce power consumption necessitates a reduction in capacitor size, which also reduces physical size. To this end, it works towards our goals of making the demodulator as small as possible and as low power as possible. That said, as the capacitance and currents become smaller, more care must be taken due to higher sensitivity to current fluctuations. Variation in the current due to internal disruptions such as supply noise, or external factors like temperature are larger for smaller capacitors where less charge is required to accumulate a higher potential.

This approach to demodulation also necessitates some logic to generate the appropriate control signals to reset and charge the capacitors at the appropriate times. All control signals are derived from the biphasic input pulses by the Pulse Generator block and asynchronous logic surrounding the demodulators for both frame detection and data demodulation.

3.5.2 Pulse Generator

The pulse generator is responsible for extracting a set of useful control signals from the biphasic current pulse. A functional block is shown below in Figure 3-41.

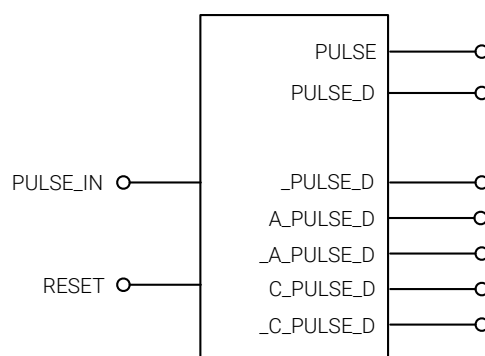


Figure 3-41 Functional block of Pulse Generator.

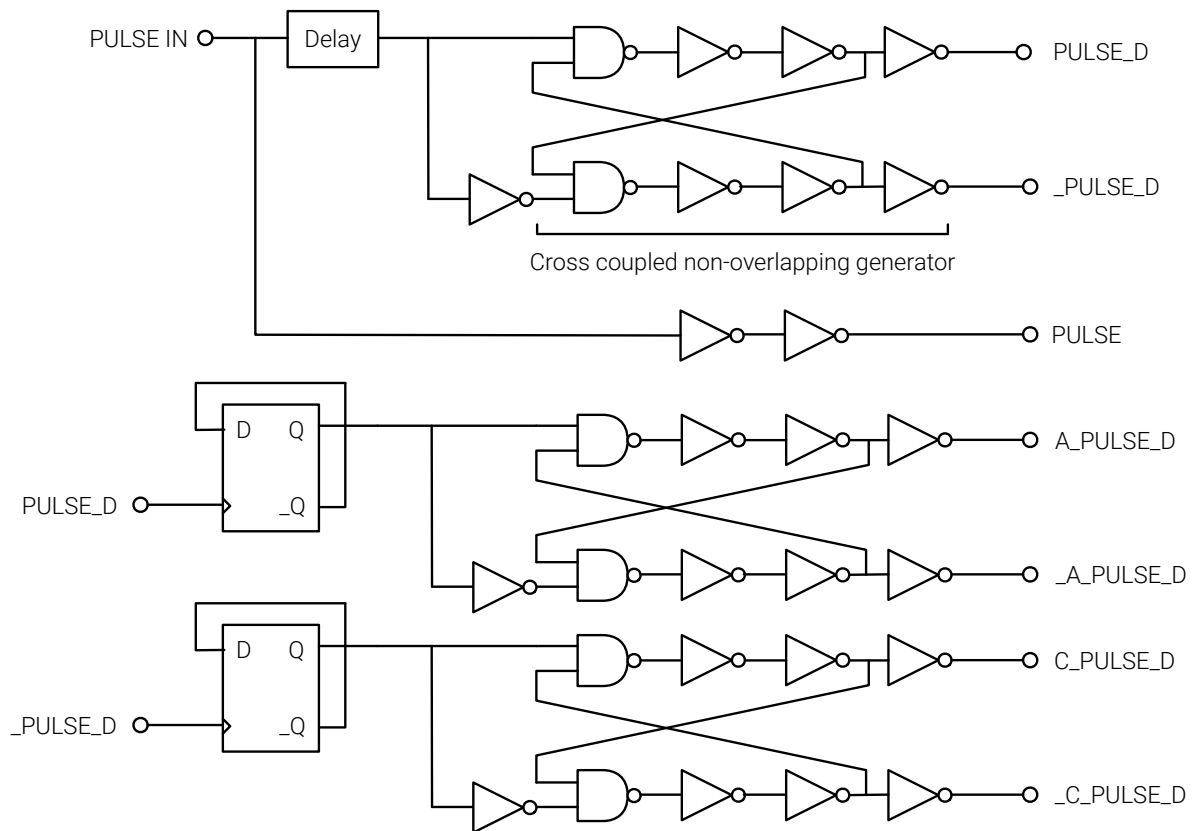


Figure 3-42 Circuit design of Pulse Generator.

The Pulse Generator is presented with a rectified version of the biphasic stimulation signal and is based around D-flip-flops, current-starved delay units, cross-coupled non-overlapping two phase clock generators as shown in Figure 3-42 [105].

The Delay Unit is based on the topology shown in Figure 3-43. This is an example of what is known as a current starved delay element [106]. In such a configuration, the current source and sink control the time it takes for the output capacitance to charge and, hence, for the output to reach the inverted state for any given input. This is important for the pulse generator circuit where the clock signal for the synchronous elements, such as the D flipflops, need to be derived from the biphasic pulses. The current source and sink bias voltages are derived from the XPAND current reference and widths were tuned to achieve a delay of approximately 1 μ s, which is about 10% of the minimum PW measured and also sufficiently larger than asynchronous logic transitions, which happen in the low nanoseconds. The effect of parasitic capacitance was negligible since device size was large.

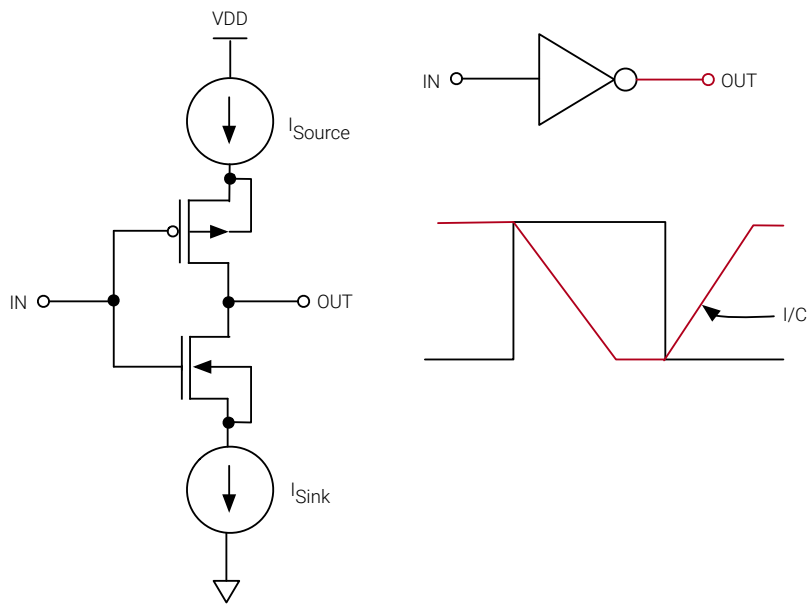


Figure 3-43 Current-starved delay element.

The cross-coupled non-overlapping generator is responsible for creating complimentary non-overlapping signals and is shown in Figure 3-45. This circuit also employs small delay elements that just need to be sufficiently larger than the transition time of the output signals of the primitive logic blocks.

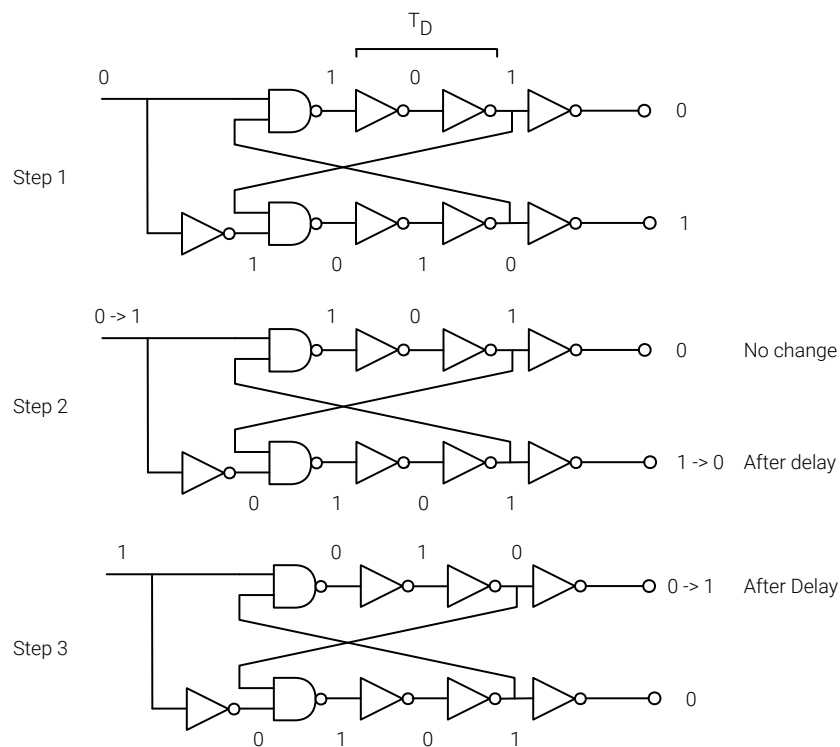


Figure 3-44 Schematic showing three steps to generation of non-overlapping signals.

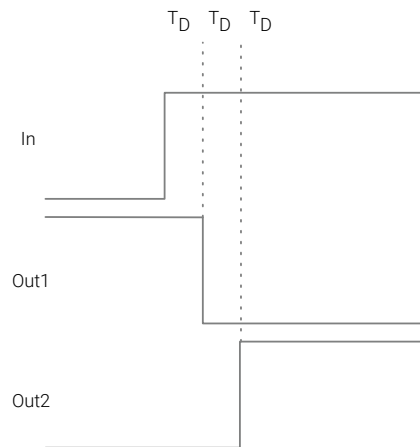


Figure 3-45 Three distinct steps showing no overlap between each transition.

D flipflops are used to capture the Anodic and Cathodic phases by toggling on the rising edge of PULSE_D and $\overline{\text{PULSE_D}}$. The inverse to these signals is generated again using cross-coupled non-overlapping generators. The waveforms generated by the Pulse Generator are shown in Figure 3-45. Note that delay in the transitions is not shown, rather it is illustrating the state transitions.

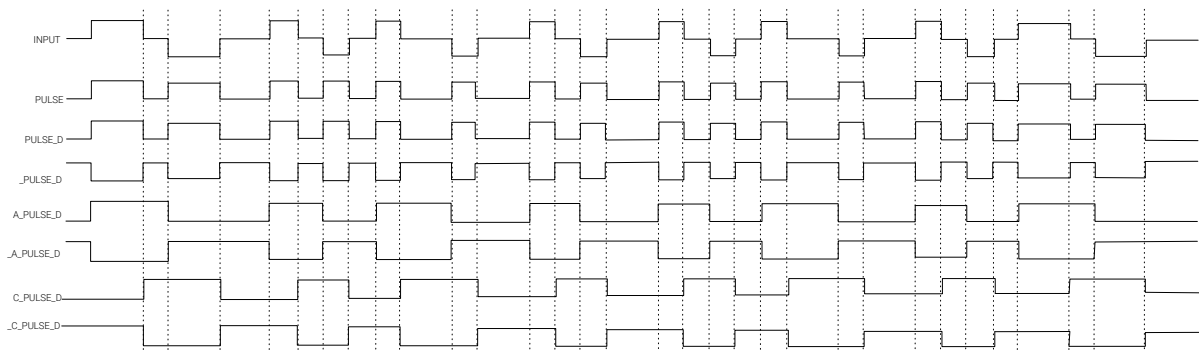


Figure 3-46 Waveform illustration for Pulse Generator

3.5.3 Frame Detection

The frame detector plays the critical role of detecting an SOF and an EOF. This is achieved using the Pulse Generator control signals and a Pulse Comparator. The functional block with control signals is shown in Figure 3-47.

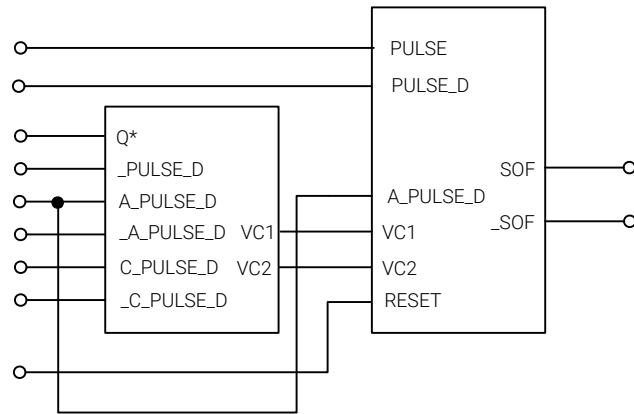


Figure 3-47 Functional diagram of data frame detector.

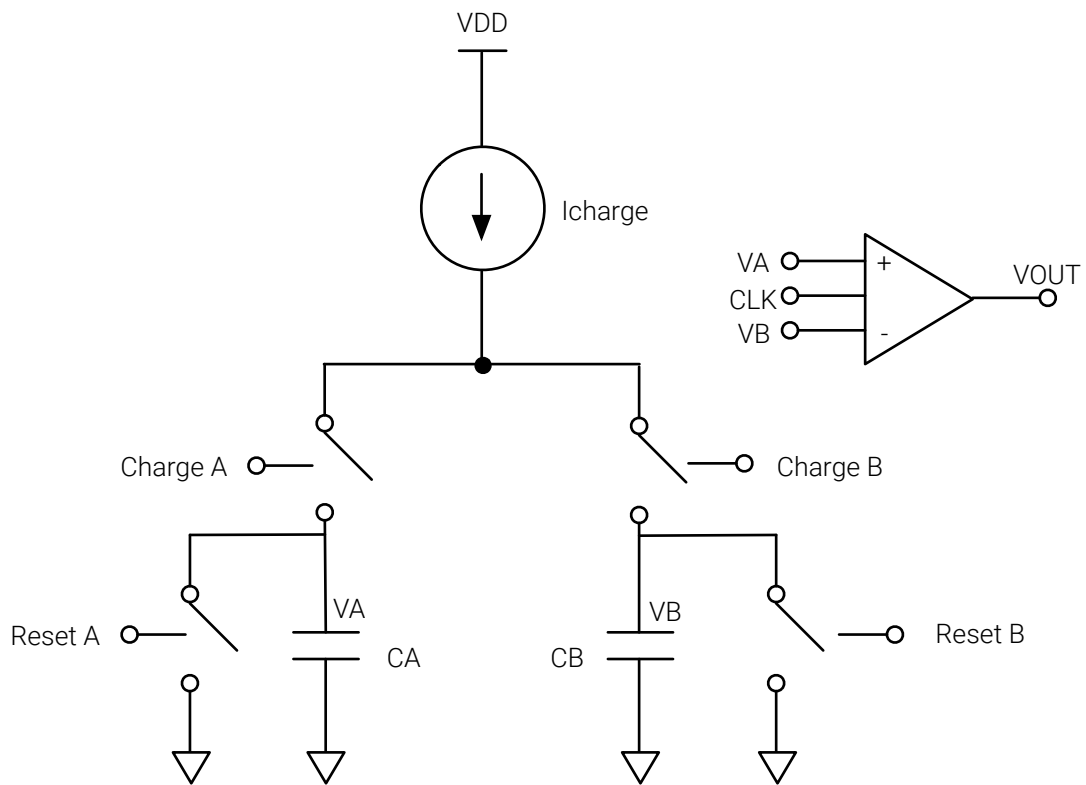


Figure 3-48 Architecture of pulse comparator.

Switches Charge A, Reset A, Charge B and Reset B are driven by asynchronous logic that transforms the Pulse Generator signals as follows.

Table 3-4 Pulse generator control signals

Anodic Phase (Charge A On)	A_PULSE_D . _C_PULSE_D
Cathodic Phase (Charge B On)	C_PULSE_D . _A_PULSE_D
ISI (Reset A On)	_A_PULSE_D . _PULSE_D
IPG (Reset B On)	A_PULSE_D . PULSE_D

Capacitor CA in Figure 3-48 is charged during the Anodic Phase and reset during the ISI. Capacitor CB is charged during the Cathodic Phase and reset during the IPG. The charging current is chosen to be as low as possible to minimise power consumption, and the capacitor sized as small as possible to minimise size. Ultimately, there is a trade-off. Sizing the capacitor too small results in higher sensitivity to leakage and disturbances. A capacitance of 1pF was fabricated on chip as it suited the nano ampere current generators and typical pulse width ranges.

To ensure voltage is maintained on the capacitor during the hold phase, an ultra-low leakage switch was needed. The topology for this is shown below in Figure 3-49. When a high voltage is applied to the gate M2, it brings the source of M4 low, switching it on. This pulls the Drain terminal to ground with a low impedance, essentially equal to the sum of M2 and M4 on resistances. When the Gate terminal is low, M2 switches off and M1 switches on. This pulls the source of M4 high thus reverse biasing M4 V_{gs} , putting it in a deep off state and ultra-high impedance state with low leakage.

Stacking NMOS transistors is possible using isolated NMOS devices as discussed in Section 3.4.1 where they are used to create a supply independent voltage reference.

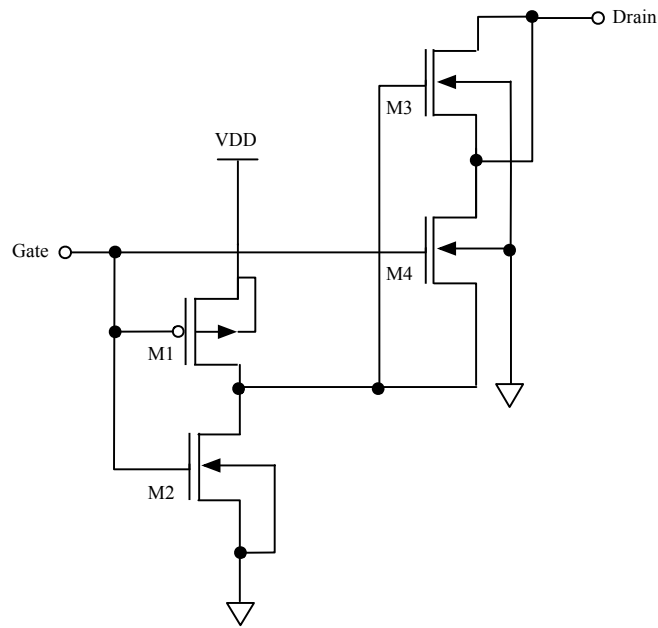


Figure 3-49 Ultra low leakage switch.

In addition to the pulse width control circuitry and detector, a dynamic latch comparator was implemented. The CLK is driven by `_PULSE`, and samples every time this is asserted, which happens on the ISI and the IPG. It is important to note that this is a non-delayed signal, and thus samples the pulse width detector prior to a reset.

When the CLK is asserted, there is a competition between M7 and M13. Assuming all things equal – the higher of the two gates will result in latching of the M9/M10 and M11/M12. When the internal latch state is established, the OUTp and OUTn drive the outer branch latch formed by M1-M4 and M16-M19. The outer branch latch is essential for maintaining state while the CLK is not asserted. In this event, both OUTp and OUTn will drift close to VDD keeping M1 and M19 asserted, which will not influence the output state; i.e., M4/M16 will remain off and M1/M19 will both become active. This will not alter a latched output state. In summary, the outer branch preserves the latched state.

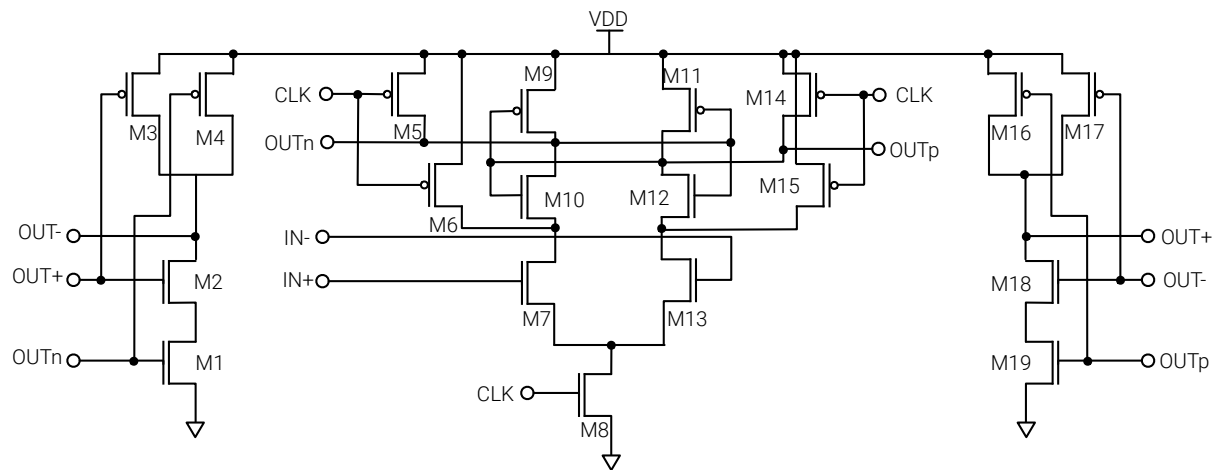


Figure 3-50 Dynamic latch comparator.

The complete frame detector circuit is shown in Figure 3-51, and a simulation of its operation is shown in Figure 3-52.

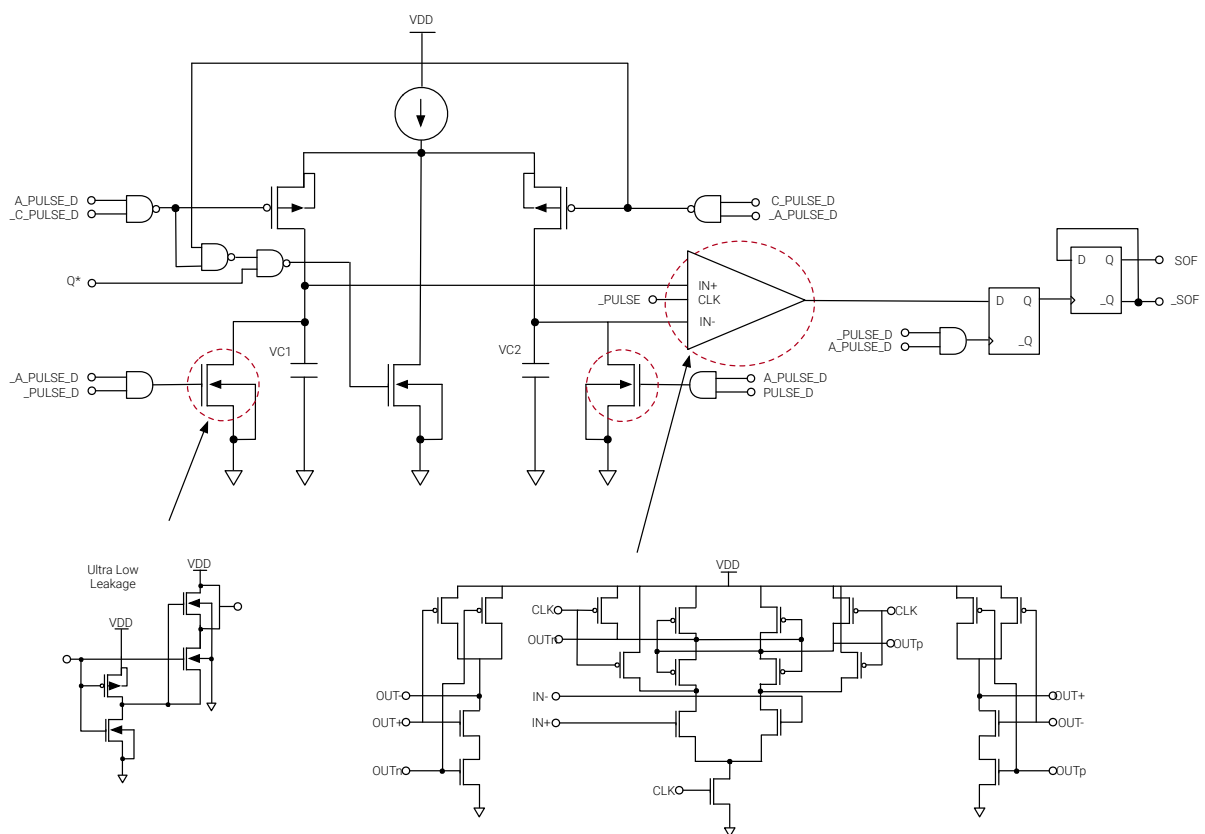


Figure 3-51 Complete SOF and EOF detector circuit.

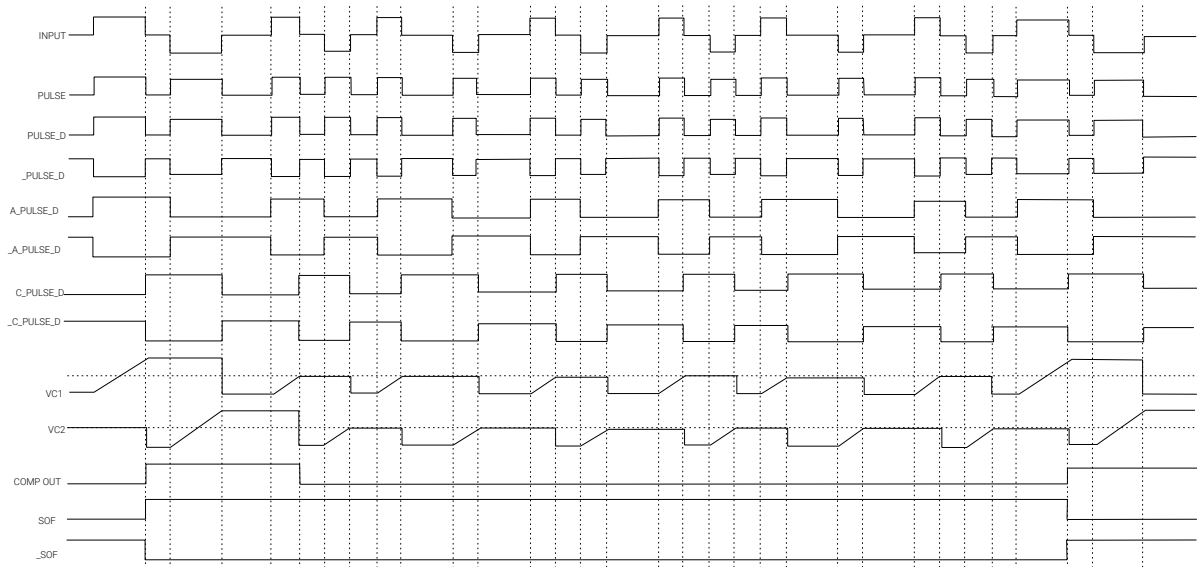


Figure 3-52 Waveform illustration of the Frame Detector.

3.5.4 Data Demodulation

Data demodulation comprises a data generator block enabled by the SOF that transfers an inversion of the Biphasic Pulse train such that the pulse are comprised of ISI and IPG widths. This is achieved using the circuit shown in Figure 3-53 with simulation shown in Figure 3-54.

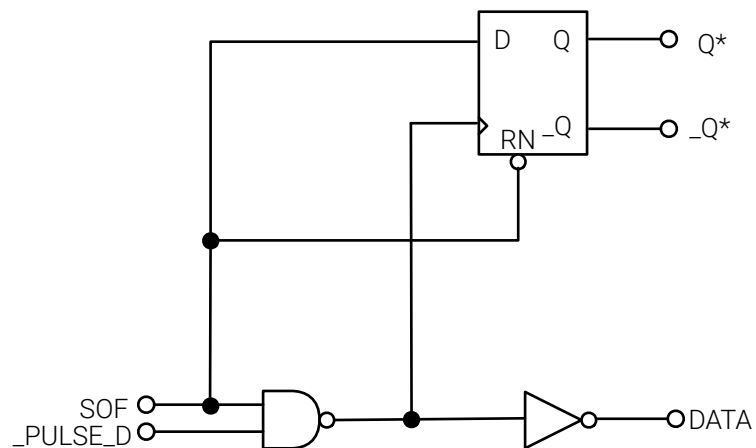


Figure 3-53 Circuit generating the data pulse train.

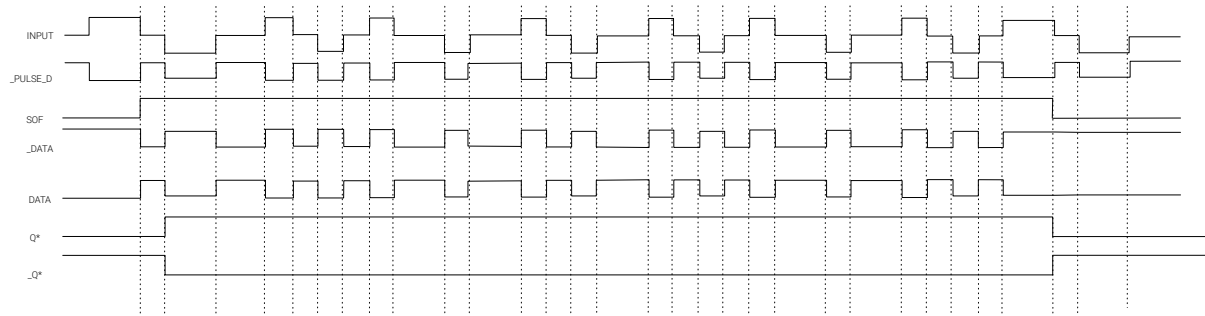


Figure 3-54 Waveform illustration of Data Pulse Train generation.

Data demodulation works fundamentally the same way as the Frame Detection, discussed in Section 3.5.3. It is worth, however, discussing the details of how the control signals are derived. As previously discussed, the Data Demodulation works by comparing the ISI of the SOF pulse with the following ISI and IPG's contained within SOF and EOF.

The control systems and associated logic enable the switching as shown in

Table 3-5 Control signals for data demodulator

ISI of SOF	DATA . _Q*
IPG and ISI	DATA . Q*

The ultra-low leakage discharge switches are especially important in the data demodulator, as the capacitor serves as a point of comparison for the entire data transmission period. This requires storage in the range of milliseconds, which was achievable without substantial decay in stored voltage. Careful considerations in the layout were noted to minimise any stray leakage.

The Data Demodulator and waveforms are presented in Figure 3-55 and Figure 3-56. The waveform illustrates the transmission of a data sequence [1001101001100].

Finally, the data demodulation phase shows successful extraction of the modulated data. The green pulses are clocked into the shift register using phase leading pulses derived directly from the biphasic pulses. Multiple inverters are used to increase the slew to ensure clean sampling.

Non-linearity in the charging on last phase is noted. This is due to the inability of the demodulators current source to deliver constant current as the drain-source voltage across it becomes small and it transitions from the saturation to the linear region. ($V_{ds} = V_{gs} - V_{th}$).

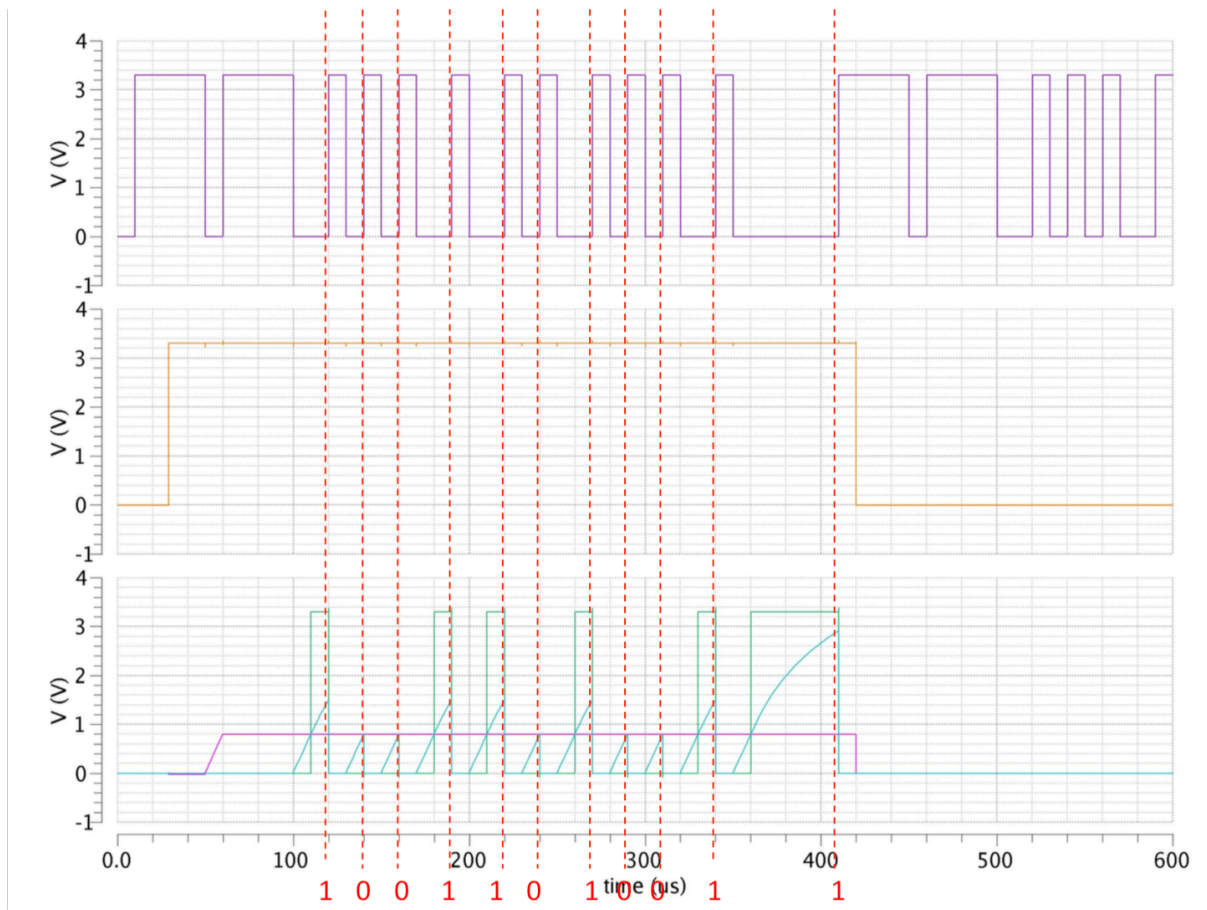


Figure 3-57 Complete demodulation simulation showing SOF detection, data demodulation and EOF detection.

3.6 Conclusion

In this chapter, the architecture for a 6 x 64 crosspoint switch to seamlessly expand the electrode count of commercial stimulators for both recording and stimulation was presented. Building a crosspoint switch in and of itself is not particularly complex when using dedicated power and communication lines. However, the use of dedicated power and communication lines in this application was not permitted for biological safety reasons (potential direct current tissue exposure) and also because this would necessitate substantial change to the design of the commercial implant by requiring the feedthrough of additional wires from the hermetically sealed package. For these reasons, the challenge was to develop a novel architecture that could derive both power and configuration data from biphasic pulses alone.

An architecture to achieve this was presented in Section 3.1, with some of the central ideas discussed briefly to pave way for a more in-depth discussion of the design. In Section 3.2, the crosspoint switch cell design was discussed, starting with a review of popular topologies. A modified transmission gate architecture with Body Cross Coupling was shown to be a good compromise between maintaining relatively low impedance across signal range, whilst also limiting the occurrence of latch up. Design considerations around addressing the switch array were then provided with the introduction of the cross-coupled level shifter and a decision to control this uniquely for each switch cell with a 384 shift array, with work to improve efficiency reserved for a second chip iteration once proven in principle.

One of the most challenging aspects of the design was the Pin Casting structure, which undergoes important state transitions in the power up cycle of the chip. This nested structure was detangled into core function blocks that were described. Ultimately, a simulation was run demonstrating the circuit operation in principle. It was a very difficult design to simulate as it required a lot of attention to the actual stimulus delivery (to be as realistic as possible) and all the initial starting conditions. This required careful consideration to open states on the current sources that lead to convergence problems, which were solved by switching in high impedance loads with voltage controlled “relays”. In hindsight, the design could have been greatly simplified if the ability to power/communicate from any two pins was relaxed.

Power storage and regulation was an exercise in maximising on chip capacitance and designing the reference circuits and regulator such that power consumption was minimised. This meant operating transistors deep in their subthreshold regions. A supply independent nanoampere reference was designed using a single transistor modification to a conventional reference design. This optimised the area required to deliver ultralow power references whilst maintaining accuracy, and it was shown that the loop gain and PSSR were analytically equivalent.

Finally, the design of the biphasic pulse demodulator was outlined. The demodulation for both frame detection and data transfer was all based around pulse width detection circuitry, which was done by charging capacitors with very small currents derived from the aforementioned voltage reference design. Given low currents and capacitors involved, attention to leakage in the switches, designed using NMOS devices, was important. An ultra-high impedance off state design was devised such that the voltage stored across capacitors was maintained whilst being compared by comparators. This was especially important for data demodulation where the SOF IPG pulse width was the point of comparison by which all successive IPG and ISI pulses within frame were compared.

Finally, the demodulator was simulated and shown to successfully detect frame and data for a typical biphasic pulse modulation paradigm.

With design of XPAND discussed, the layout of the chip, fabrication and testing will now be presented.

4 XPAND layout, fabrication and testing

In this chapter, the full layout, fabrication and testing of the XPAND chip is presented. The layout of XPAND was not purely a linear progression from the design, but rather modifications to the design were needed so the chip could be contained to a silicon area of reasonable size. This was not simply a question of cost, but also to prove such a system could be implanted in an area that was suitably small for its intended purpose. The task of laying out the complete 6 x 64 element array was complicated by the use of exotic High Voltage devices and the circuit's mixed signal nature. This meant layout needed to be painstakingly done rectangle by rectangle. What was estimated to take 6 months ended up taking 18 months.

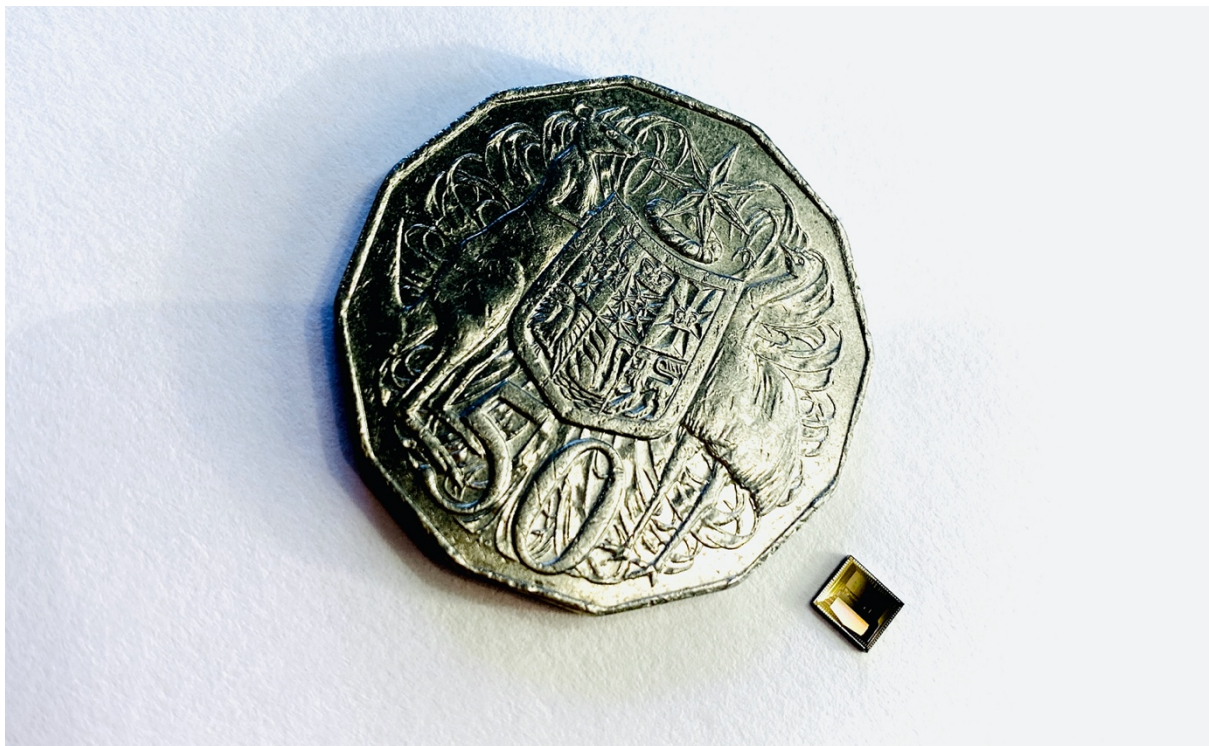


Figure 4-1 An image of the XPAND die alongside an Australian 50 cent coin.

4.1 Process Selection

It was important to first identify and gain access to the Process Design Kit (PDK) for a technology capable of withstanding high voltages well in excess of standard CMOS low voltage technology. The process was also required to support mixed signal design. The Austria Microsystems (AMS) H35 high voltage process was chosen as it supported these requirements and an agreement was established with the University of Melbourne to gain access to the PDK. Installation of the PDK and integration with Cadence proved to be a very arduous exercise in part due to an inexperience in using the software and, in part, due to the fact the installation needed to be done by the University's Central IT and could not be installed locally.

As access to the PDK was established via a non-disclosure agreement (NDA), device details cannot be reproduced. Suffice to say that the kit included standard low voltage primitive devices and some logic. The high voltage devices were more exotic and required much more semiconductor level understanding and consideration particularly regarding nuances around the guard ring and body biasing.

All primitive low voltage transistors, low voltage isolated transistors, high voltage transistors, resistors, capacitors and isolated NMOS devices were provided. Whilst low voltage primitive logic gates were included, high voltage logic devices needed to be designed at a transistor level.

4.2 Definitions for layout

In Chapter 3, the architecture for XPAND was described. For this chapter, there is a change in the definitions of the functional blocks. The demodulator and decoder are simply the demodulator and the registers are assumed to be within the switch array. Also, the Biphasic Power Harvesting block is now simply denoted as POR (Power On Reset). These definitions are based on legacy and to simplify understanding of the test pin out. Figure 4-2 shows the architecture presented in Chapter 3, whilst Figure 4-3 will be referenced in this section.

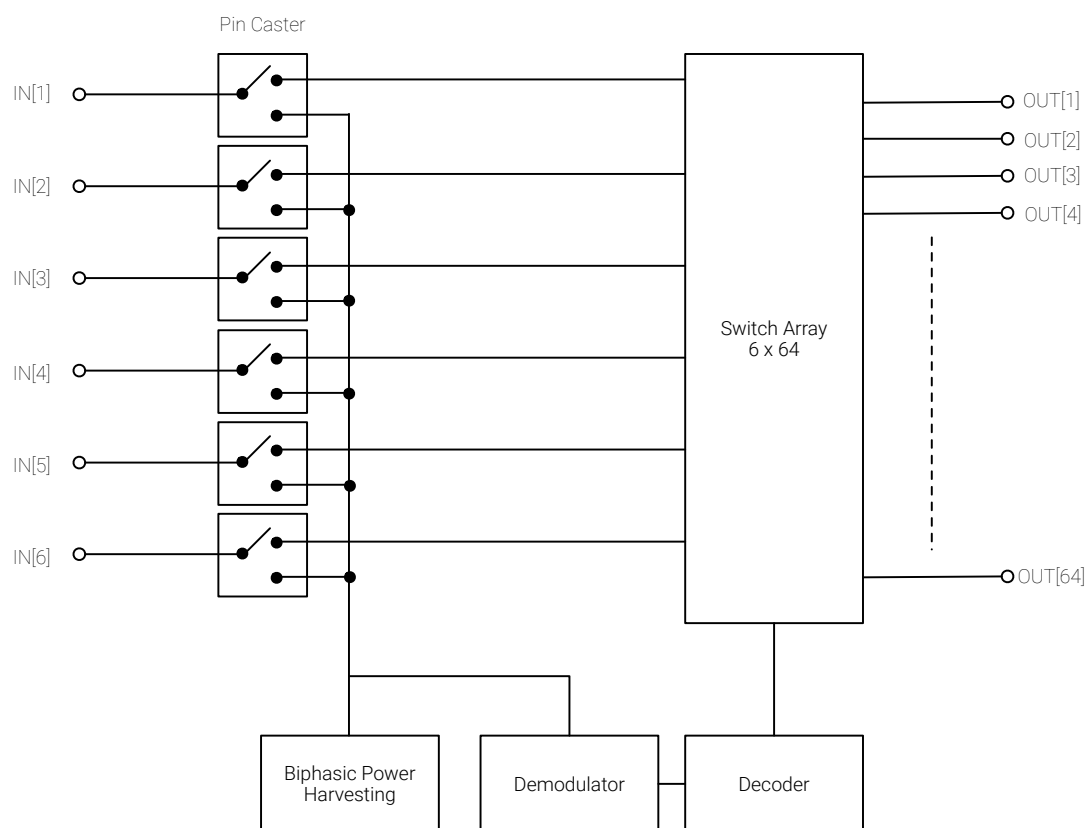


Figure 4-2 The proposed architecture of XPAND.

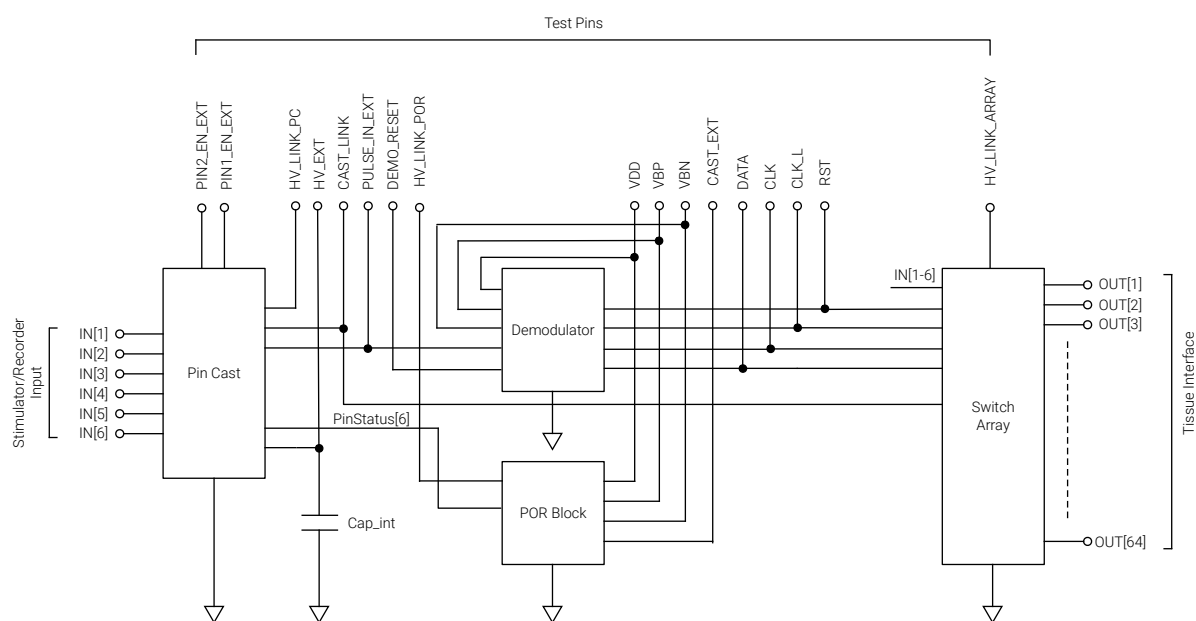


Figure 4-3 The actual XPAND architecture implemented on chip.

4.3 Layout

During the layout phase, it is important to consider density, device matching, parasitic generation and isolation. XPAND incorporates high voltage power circuits, sensitive low voltage analogue circuits and standard core logic. Each of these circuit types is constrained differently and must mitigate risk of the aforementioned concerns. This is summarised in Table 4-1.

Table 4-1 Layout considerations with respect to core blocks.

	Density	Matching	Parasitic	Isolation
Switch Array	High	Low	Low	High
POR	Low	High	High	Low
Demodulator	Low	High	High	Low
Pin Cast	Low	Low	Low	High

4.3.1 Switch Array and Pin Cast

The use of high voltage devices made the layout fundamentally more complex, as they incorporate multiple wells that must be biased carefully and require additional routing. This presented challenges in ensuring reasonable switch cell density could be achieved to keep the 6 x 64 array area within budget (approx. 16mm²).

Optimisation was a fine balance of refining transistor width and finger numbers to achieve the required conductivity and geometric proportions. In addition to this, deep isolation n-wells and guard rings were shared where it made sense to do so. These decisions required continuous consideration at a semiconductor level to prevent undesirable parasitic formation that could lead to latch-up and poor performance.

A significant amount of care was given to the switch cell layout prior to full layout of the array as changes post layout were not feasible given the enormity of the layout, which was a fully manual task.

4.3.2 POR and Demodulator

Both the POR and demodulator contained ultra-low power and sensitive analogue circuits including the voltage reference, pulse width detectors, comparators and OTAs. There are numerous well documented layout techniques that were applied [97]. This included the use of dummy transistors to enhance device symmetry, careful attention to device alignment and overall symmetry.

4.3.3 Full Layout

In total, the layout of XPAND proved to be substantially more difficult than anticipated. Getting the layout to pass LVC and DRC was an enormous milestone. The complete layout is shown below in Figure 4-4.

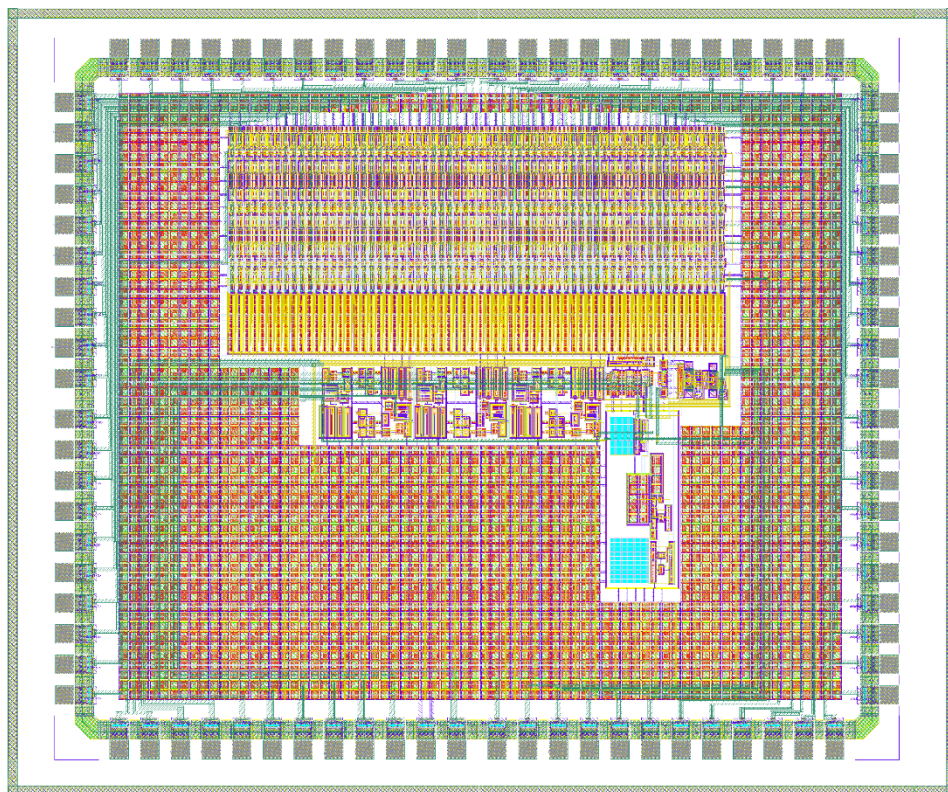


Figure 4-4 XPAND complete layout.

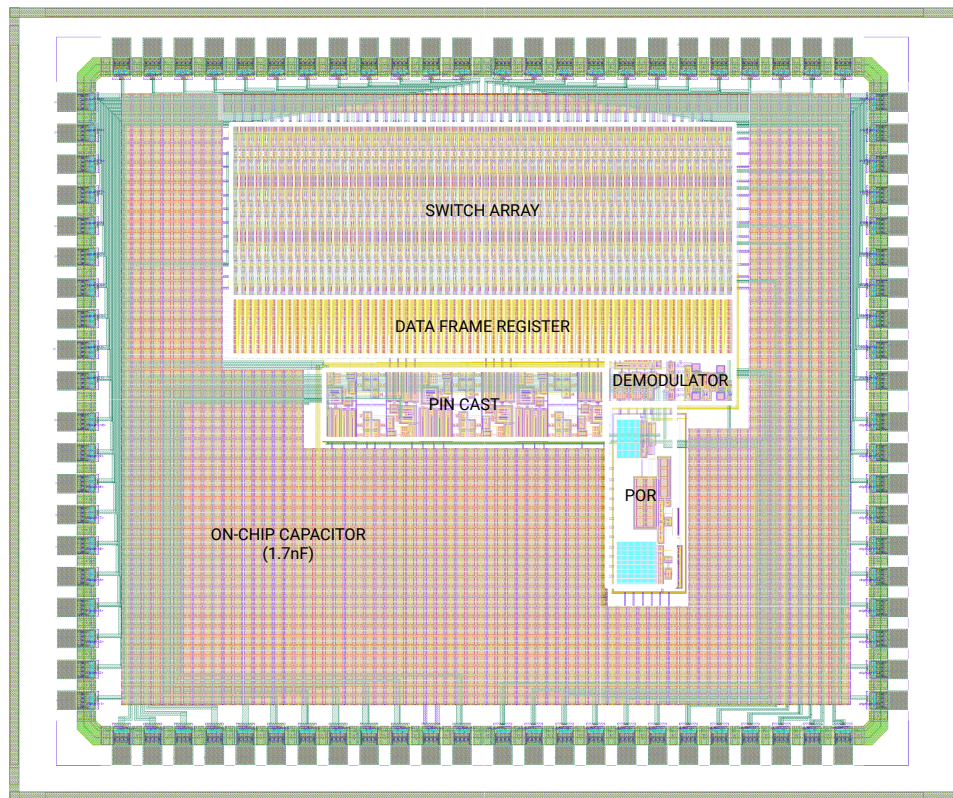


Figure 4-5 XPAND complete layout with major blocks overlaid.

What is somewhat abstracted from the layout, shown in Figure 4-5, is the vast metal wiring that was required to connect the system. This presented substantial challenges and rerouting major sections was a common occurrence. This layout gives an indication of how such a chip could scale with increases in input and output count.

4.4 Fabrication

Twenty devices were fabricated using the MOSIS multi-project wafer service. Since it would be prohibitively expensive to fabricate a chip on a single wafer, MOSIS aggregates designs from around the world that use a common process. A final chip is photographed in Figure 4-6. Once Layout Vs Schematic (LVS) and Design Rules Check (DRC) were complete, additional information was required. This process took approximately 3 months.

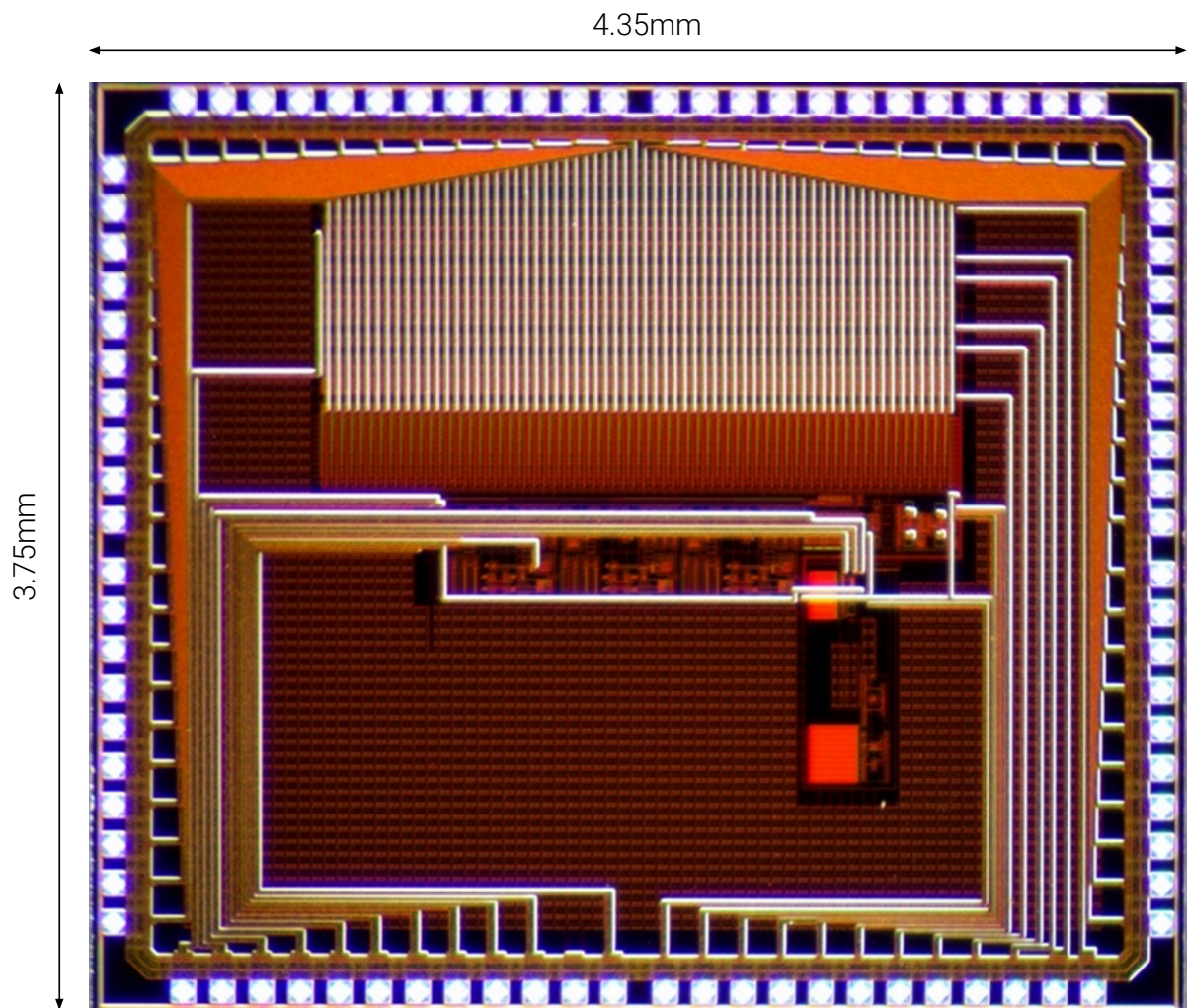


Figure 4-6 Photograph of the XPAND chip.

To test the chip, wire-bonding was needed to break out chip pads to a larger ceramic package to be soldered to a custom PCB testbed. This was first attempted using a manual ultrasonic wire-bonding machine but, due to equipment issues, was outsourced to the Melbourne Centre for Nanofabrication (MC^N). This final assembly is photographed in Figure 4-7, with a closeup of a fully wire-bonded chip shown in Figure 4-8.

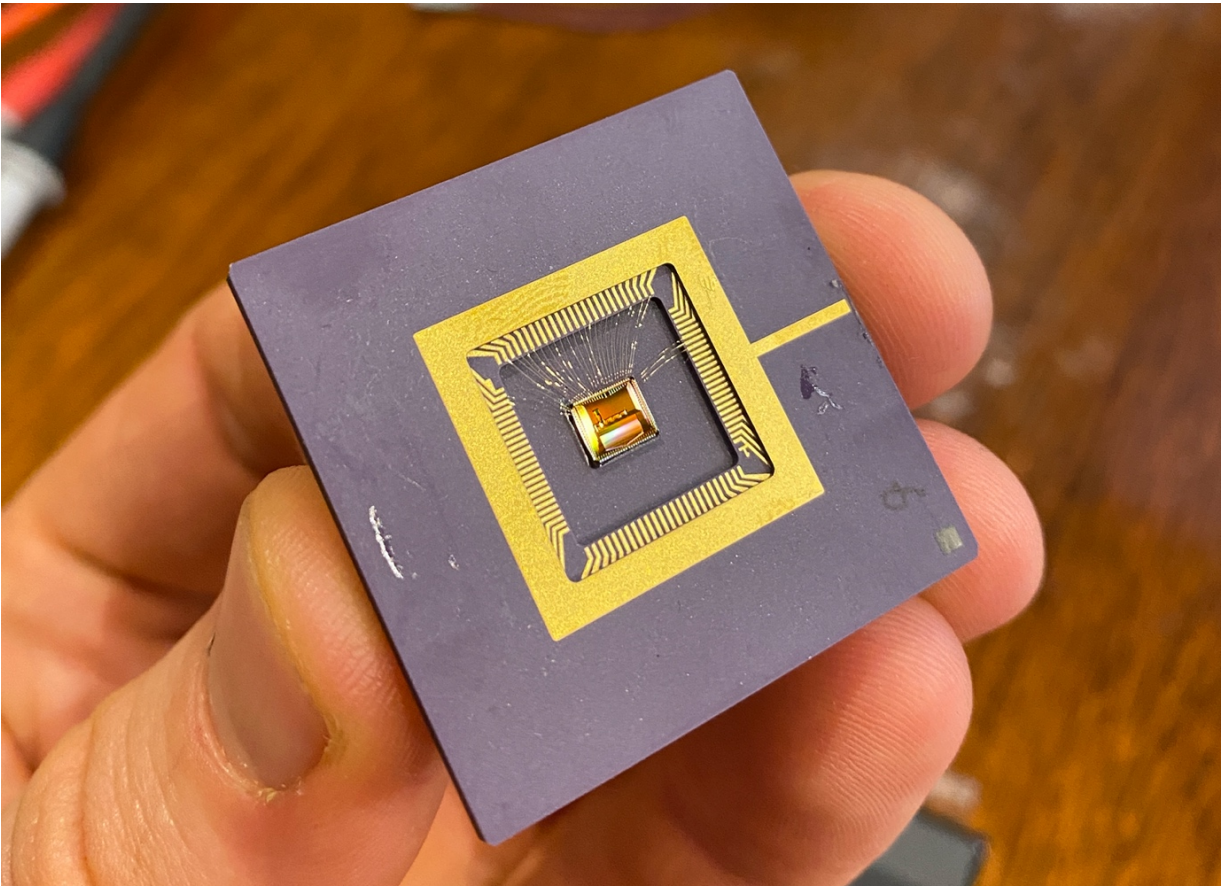


Figure 4-7 XPAND die affixed and ultrasonically wire bonded to package.

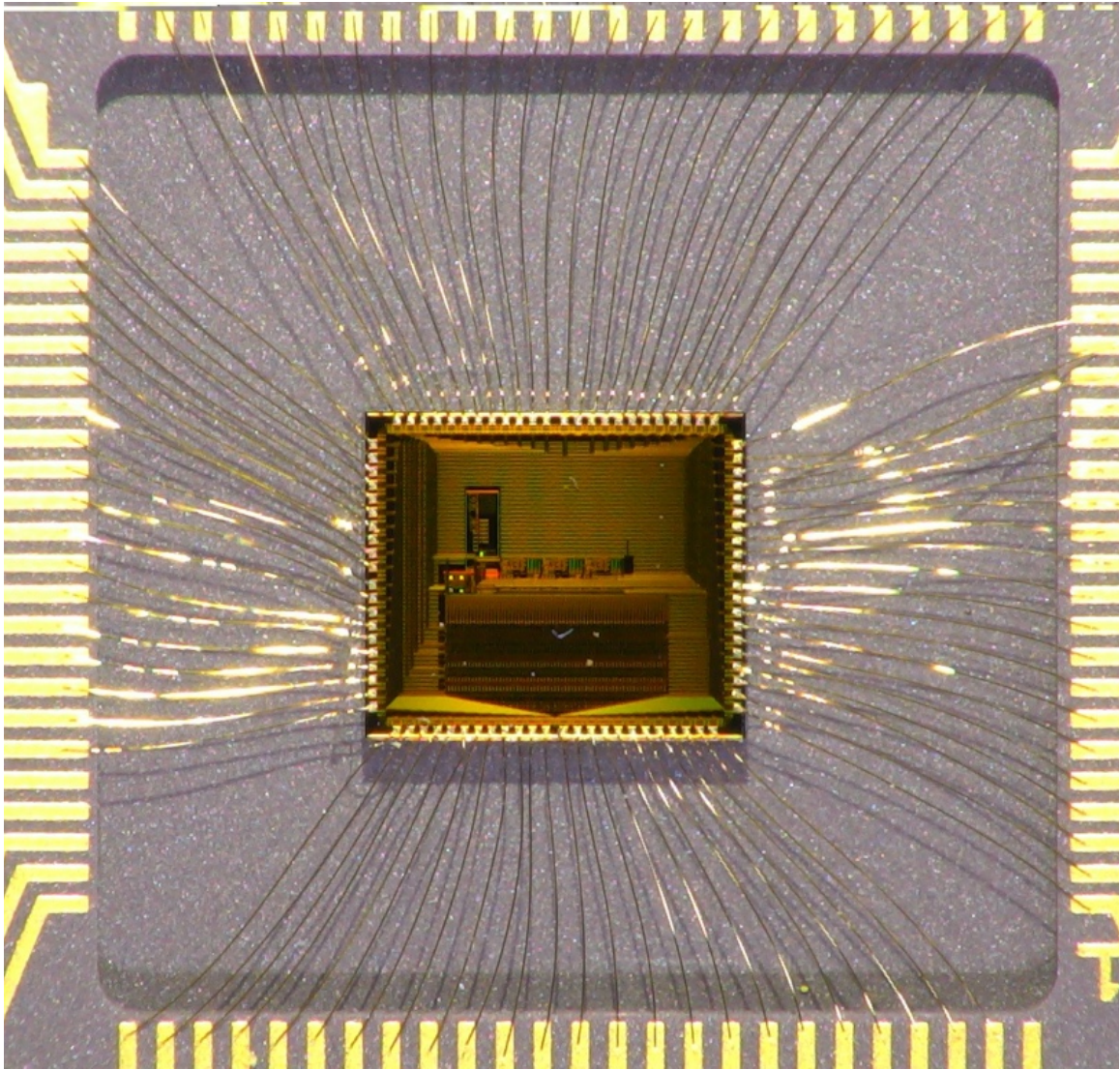


Figure 4-8 Photograph showing clearly the wire bonding.

4.5 Pin Mapping

The system as a whole is nested in nature, deriving all communication and power from any two input pins. Test pins were, therefore, very important to expose sub-circuit power i/o and associated control signals. As a probing station was not readily available, these test pads were broken out to the edge of the chip and, subsequently, ultrasonically wire bonded to the chip package. This strategy was exploited to the full extent possible but was ultimately limited by the number of package pads available for the chip size. Test PADS within the sub circuits would have been very ideal and facilitated greater diagnostic capability in the testing phase.

Pads – exposed metal contact points – on the chip are mapped to pads on the ceramic package. These are then mapped to pins on the ceramic package that are mapped to the test PCB board. Figure 4-9 shows the chip level pad assignment and the ceramic package. The complete XPAND mapping is outlined in Table 4-2.

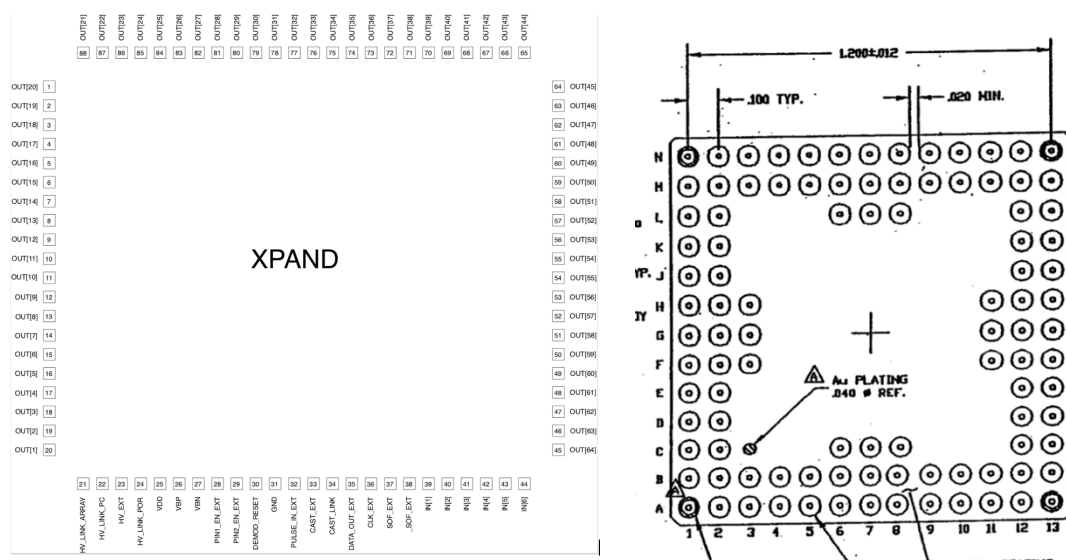


Figure 4-9 XPAND pin mapping shown (L) and ceramic pin mapping (R).

Table 4-2 Complete pin mapping from XPAND pad to ceramic pin.

XPAND PAD #	PACKAGE PIN	FUNCTION	cont..		
1	B2	OUT[20]Ca	34	N7	CAST_LINK
2	B1	OUT[19]	35	N8	DATA_OUT_EXT
3	C2	OUT[18]	36	M8	CLK_EXT
4	C1	OUT[17]	37	L8	SOF_EXT
5	D2	OUT[16]	38	N9	_SOF_EXT
6	D1	OUT[15]	39	M9	IN[1]
7	E2	OUT[14]	40	N10	IN[2]
8	E1	OUT[13]	41	M10	IN[3]
9	F3	OUT[12]	42	N11	IN[4]
10	F2	OUT[11]	43	N12	IN[5]
11	F1	OUT[10]	44	M11	IN[6]
12	G2	OUT[9]	45	M12	OUT[64]
13	G3	OUT[8]	46	M13	OUT[63]
14	G1	OUT[7]	47	L12	OUT[62]

15	H1	OUT[6]	48	L13	OUT[61]
16	H2	OUT[5]	49	K12	OUT[60]
17	H3	OUT[4]	50	K13	OUT[59]
18	J1	OUT[3]	51	J12	OUT[58]
19	J2	OUT[2]	52	J13	OUT[57]
20	K1	OUT[1]	53	M11	OUT[56]
21	M2	HV_LINK_ARRAY	54	H12	OUT[55]
22	N2	HV_LINK_PC	55	H13	OUT[54]
23	M3	HV_EXT	56	G12	OUT[53]
24	N3	HV_LINK_POR	57	G11	OUT[52]
25	M4	VDD	58	G13	OUT[51]
26	N4	VBP	59	F13	OUT[50]
27	M5	VBN	60	F12	OUT[49]
28	N5	PIN1_EN_EXT	61	F11	OUT[48]
29	L6	PIN2_EN_EXT	62	E13	OUT[47]
30	M6	DEMODO_RESET	63	E12	OUT[46]
31	N6	GND	64	D13	OUT[45]
32	M7	PULSE_IN_EXT	65	B12	OUT[44]
33	L7	CAST_EXT			

The mapping as related to the functional components of the XPAND are shown in Table 4-3.

Table 4-3 Functional description of each Pin.

PIN NAME	DESCRIPTION
Switch I/O	
IN[X]	Stimulator Input Pins
OUT[X]	Tissue Interface
Control	
PULSE_IN_EXT	Pin Cast output pulse / Demodulator Input
PIN1_EN_EXT	Pin Cast 1 Rectifier Switch Gate
PIN2_EN_EXT	Pin Cast 2 Rectifier Switch Gate
CAST_LINK	Pin Cast Input to Switch Array and Pin Cast modules
CAST_EXT	Pin Cast Output from POR module
DEMODO_RESET	Demodulator Reset Signal
DATA	Switch Array Data Input
CLK	Switch Array Data Register Clock

CLK_L	Switch Array Data Buffer Clock (Configure array)
RST	Switch Array Data Register Reset
RST_L	Switch Array Data Buffer Reset
Power	
HV_EXT	Internal Capacitor Voltage (Rectified Output)
HV_LINK_POR	POR High Voltage Supply
HV_LINK_ARRAY	Switch Array High Voltage Supply
HV_LINK_PC	Pin Cast High Voltage Supply
VDD	3.3V Regulator Output
VBP	Voltage Reference PMOS Gate Voltage
VBN	Voltage Reference NMOS Gate Voltage
GND	Ground

In this section, we will explore each of the modules in their basic operating modes and the chapter will conclude in a demonstration of XPAND gating biphasic stimulation pulses whilst reading ECG.

4.6 Testing

Due to lab restrictions imposed during COVID-19 measures, testing of XPAND was performed using a temporary “lab” setup in a home environment. This was not really a limitation in terms of the testing performed but did require the assembly of ad hoc testing circuits and software to evaluate.

In this section, each of the major blocks is evaluated. Since XPAND is a highly nested design, key blocks were chosen and tested to see if they met key functional requirements. Finally, the XPAND chip is configured shown to successfully gate recording and stimulation signals.

4.6.1 POR Block

As discussed in Section 4.2, the Power on Reset (POR) block represents all the power on circuitry including the voltage reference and regulator. In this section, results of this block are presented.

4.6.1.1 Test 1: Static Power Consumption

The POR module is powered by the main capacitor, which is charged through the rectification of stimulation pulses. As discussed, the quiescent current consumption was necessarily kept as low as possible with a target of $<500\text{nA}$.

A precision, mains powered Digital Multimeter (Keysight 34470A) was used to measure current, whilst a handheld Multimeter (Fluke 179) measured voltage. The input voltage was generated using a Keysight E36313A power supply, which included accurate current supply limiting necessary (1mA limit). The use of battery powered and mains powered devices ensured isolation between the two measurement devices. Without isolation, at ultra-low currents being measured, leakage resulting in inaccurate results was possible. In addition, the current measurements were done separately as the meter had a finite input impedance, which at the current levels being measure is relevant; i.e., leakage from the multimeter could increase current being measured.

Within the XPAND, static power consumption is dominated by the current sources in the OTA and the reference, which together form the voltage regulator. A mirror of ratio 1:2 was applied from the reference to the OTA and the reference target current was 100nA . Based on this, the stable consumption of the complete regulator was theoretically 330nA .

The device under test (DUT) is shown in Figure 4-10, with a schematic of the regulator shown in Figure 4-11.

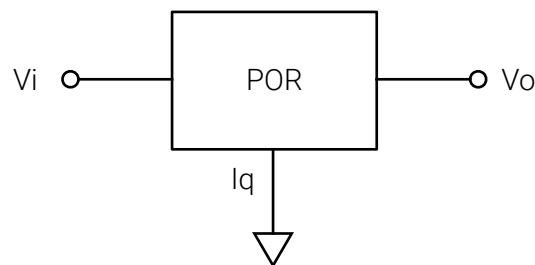


Figure 4-10 The basic Power On Reset functional block with respect to complete regulator circuit.

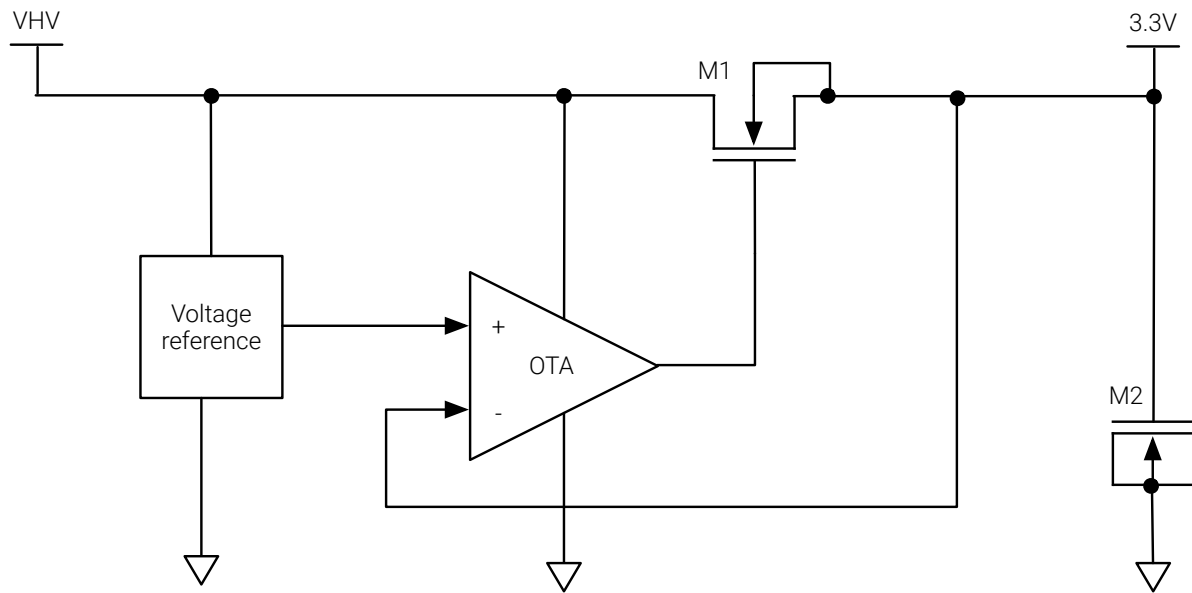


Figure 4-11 Linear regulator functional diagram.

Results of static current consumption testing are summarised in Table 4-4. This shows less than expected consumption but good consistency from device to device.

Table 4-4 I-V measurement results for ultra-low power regulator.

Vi (V)		Chip No. (Measured)			Simulated
		1	2	3	
9	Vo (V)	3.493	3.465	3.485	3.35
	Iq(nA)	200	185	239	353
8	Vo (V)	3.492	3.465	3.486	3.35
	Iq (nA)	80	88	85	310
7	Vo (V)	3.491	3.471	3.486	3.35
	Iq (nA)	58	65	64	258

Measurements of the chip showed favourably low consumption of 58nA at 7V as compared with simulations of 258nA with the quiescent current dropping as expected with lower supply levels.

4.6.1.2 Test 2: Regulator Start-Up Stability

The E36313A utilises supply current limiting and ramping. This provided a useful ramp to show the switch on voltage, which was measured to be 6.71V. The regulator dropout voltage is simply a function of the OTA's maximum output swing relative to the supply and the threshold voltage of the NMOS transistor M2.

A step of 10V was applied to the input of the POR to measure the stability as shown in Figure 4-12. The purpose of this was to look for overshoot and oscillation on start-up, which would be indicative of instability in the regulator.

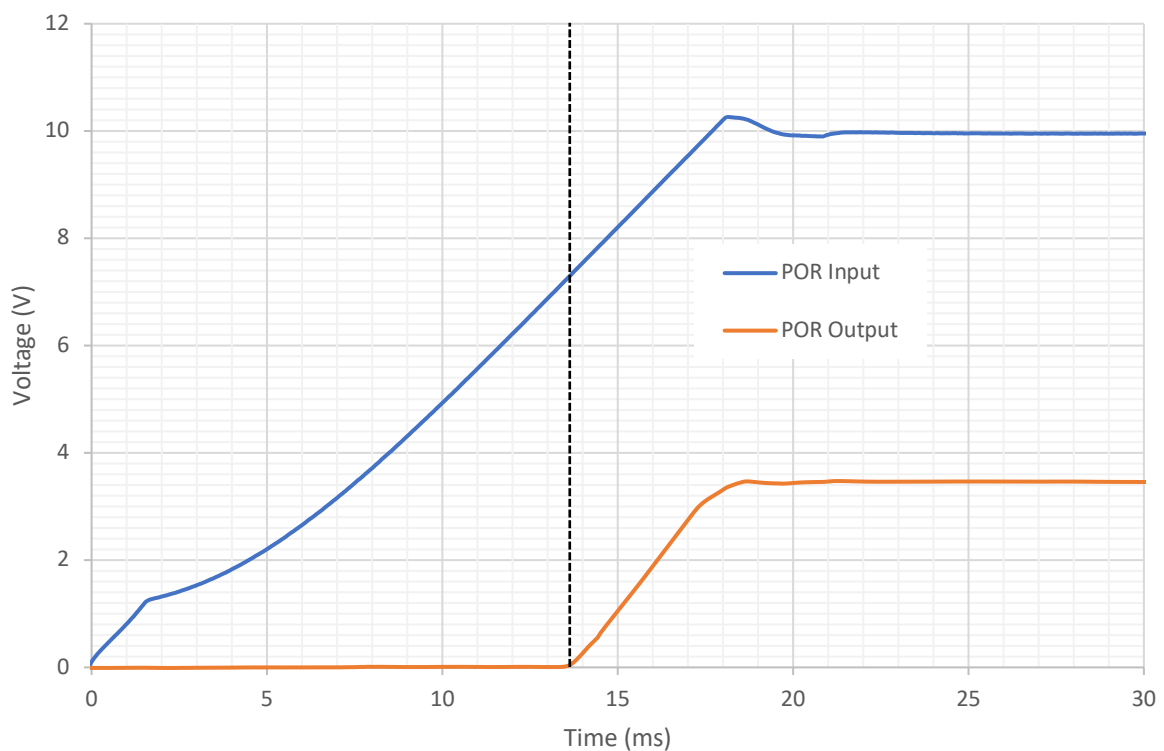


Figure 4-12 The regulator start-up as a function of ramped input voltage.

To better understand the stability of the regulator, a large 47uF capacitor was placed across the power supply near XPAND and a mechanical switch used to connect. This effectively

bypassed the power supply current limit to understand if stability were affected by very fast switch on transients. This is presented in Figure 4-13, where the output of the regulator is shown to give 4ms rise time with only marginal overshoot.

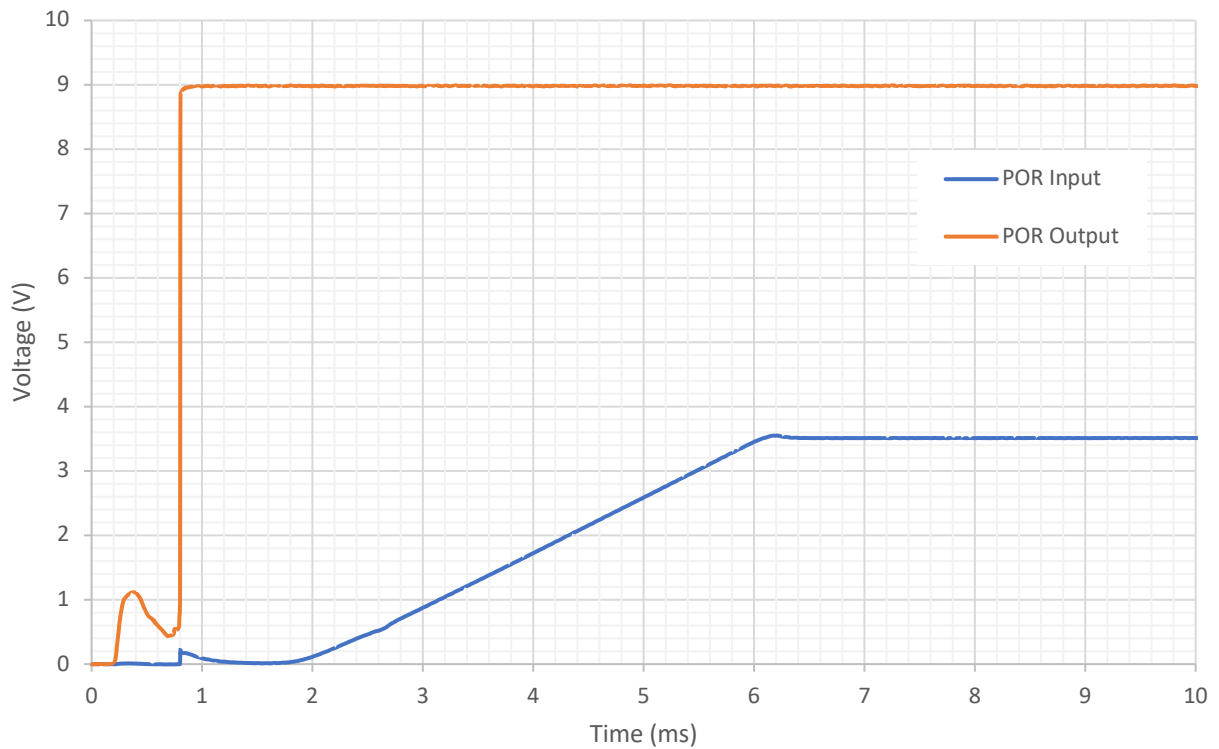


Figure 4-13 Regulated output voltage as a function of instantaneous input voltage.

4.6.1.3 Test 3: On-Chip Capacitance

The large internal capacitor of XPAND was measured using the Keysight 34470A DMM. The capacitance was found to be equal to 1.7nF for all chips to the limits of measurement accuracy.

In terms of optimising the on-chip capacitor, the target was simply to maximise its value in the available area. In earlier calculations, an estimate of 100pF was the basis of design. However, a larger chip area was obtained and every bit of available space was utilised. This capacitance was optimised using the gate of many high voltage NMOS devices whose gate capacitance to overall device size was the greatest of all devices available.

4.6.2 Demodulator

The demodulator is responsible for taking a single pulse stream and demodulating this into data and control signals used to configure and program the Switch Array. In essence, the demodulator consists of two pulse width comparators and associated logic. One is used to detect a Start of Frame (SOF) and End of Frame (EOF) events whilst the other is used to compare ISI and IPG intervals contained within the SOF to that of the SOF IPG.

As a probing station was not available, external chip pads were used to break out as many signals as possible. However, these pads were quickly exhausted and not all signals of importance could be broken out. This included many nested within the demodulator. Signals available are summarised below in Figure 4-14.

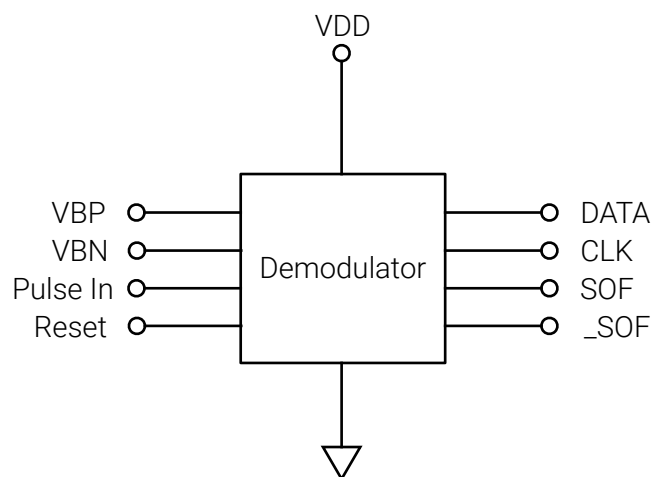


Figure 4-14 Demodulator functional block.

4.6.2.1 Test 4: SOF/EOF Frame Detection and Clock Generation

The first step to testing the demodulator was checking the frame detection circuit was working as expected. Figure 4-15 shows a simplified schematic of the circuit.

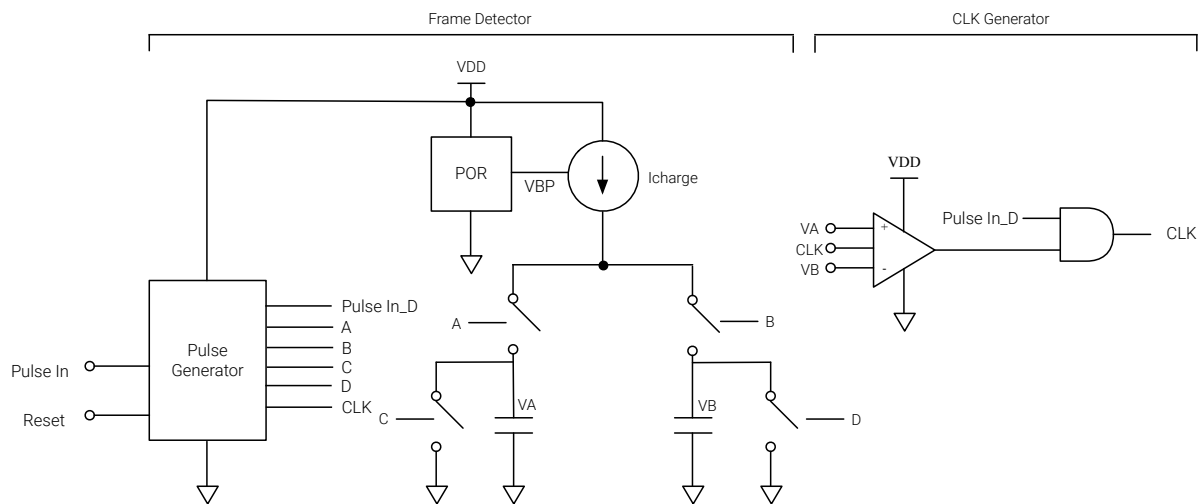


Figure 4-15 Simplified diagram of the frame detection circuit.

With power to the demodulator being derived from the internal POR module supplied with 10V via an external source, a general purpose microcontroller (Arduino Duo) was connected to the demodulator Pulse In and Reset pins and programmed to generate a pulse width modulated data stream to simulate a rectified biphasic source. The stimulus pulse stream parameters are summarised in Table 4-5.

Table 4-5 Stimulus pulse parameters

SOF	Pulse Width (us)
Pulse Width	100
Interphase Gap (Data PW Set)	10
Inter Stimulus Interval	10
Data	
Pulse Width	10
Interphase Gap	10
Inter Stimulus Interval	50

The pulse stream and CLK were captured using a portable oscilloscope (Digilent Analog Discovery 2). Results of the frame detection test are shown in Figure 4-16. The CLK out signal

is the Pulse Train shown in orange, which is gated by the SOF and EOF. The data demodulator was shown to successfully detect SOF and EOF events and gate the Pulse Signal as intended. However, additional external supply decoupling across the output of the SOF was required to stabilise the digital supply rails.

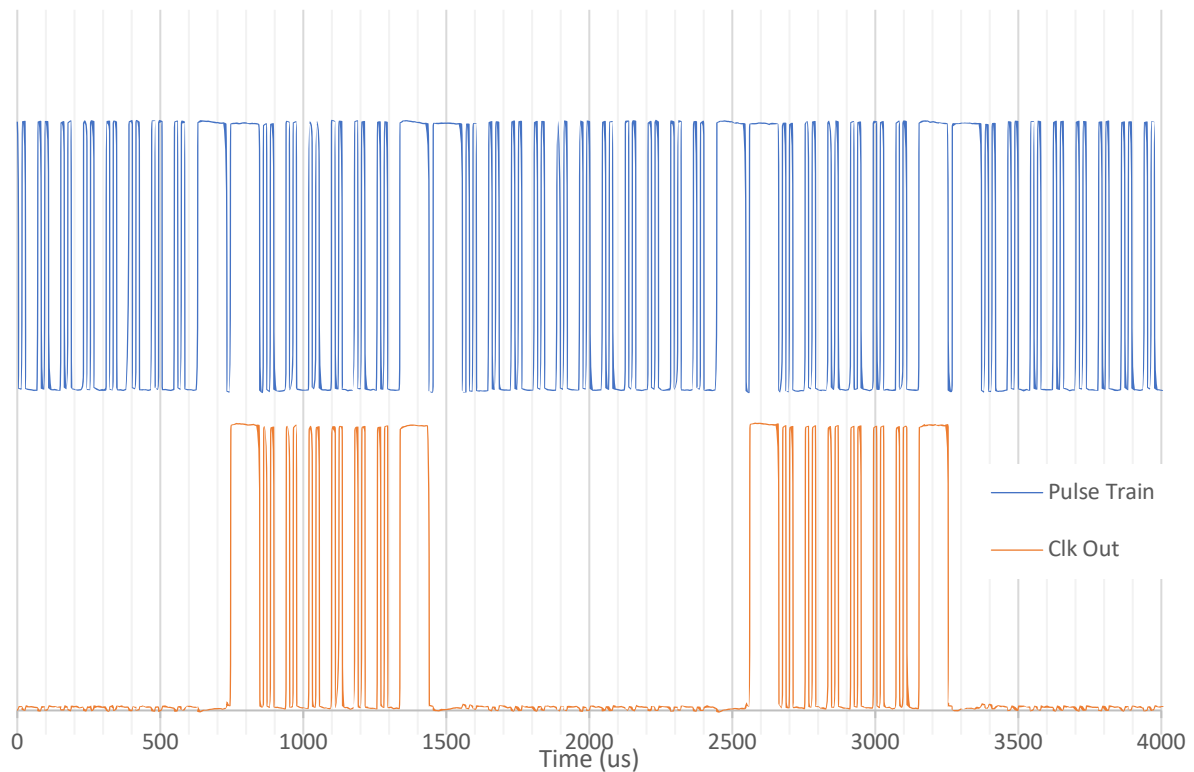


Figure 4-16 Successful detection of SOF and EOF as demonstrated by the gated CLK output signal.

Fluctuations due to digital logic transients created noise that disturbed the demodulator current generation and, as such, its ability to reliably detect pulse widths. This was not identified in the simulation and came as a surprise, as the digital logic operating at relatively low speeds with clean digital input lines was expected to consume very little dynamic power. Nevertheless, the issue was resolved with the use of external decoupling on the VDD line and when this was applied the circuit was able to detect SOF and EOF. This is problematic as an external decoupling capacitor is not desirable.

4.6.2.2 Test 5: Data Demodulation

Data demodulation is achieved in much the same way as SOF and EOF detection. That is, it is based around the use of a pulse width comparator but with different associated logic. The interstimulus interval of the SOF pulse sets the width of comparison and all subsequent interstimulus and interphase gap widths are compared. This part was nested well within the demodulator with no exposed pins. The circuit being tested in this section is shown in Figure 4-17.

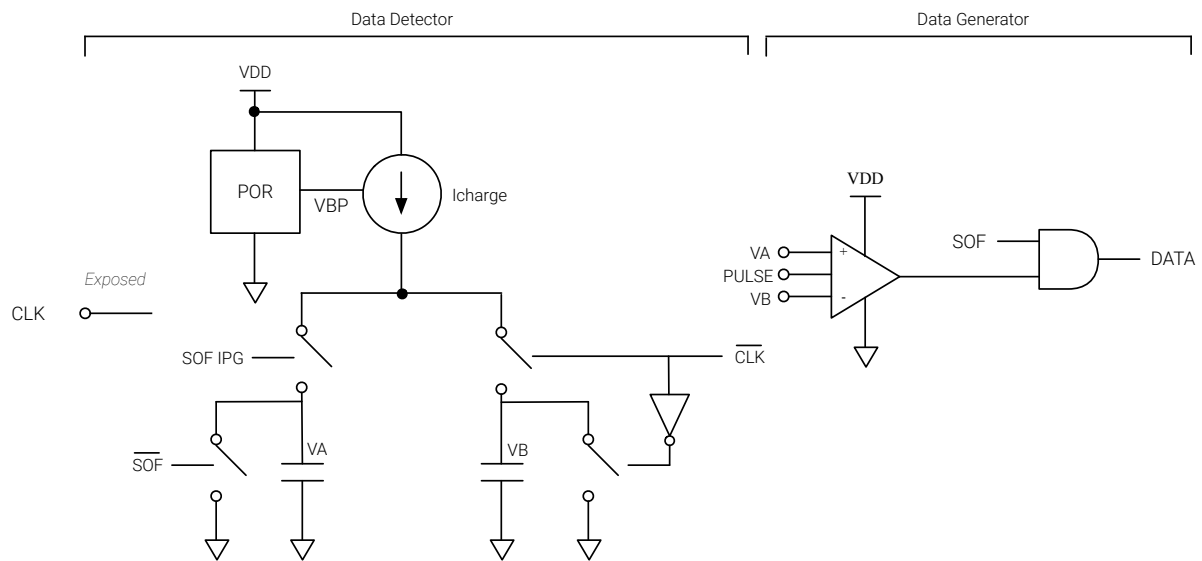


Figure 4-17 Simplified diagram of the data detection circuit.

The test procedure was the same as for frame detection with the exception that the DATA output was observed and not the CLK. A broad variety of pulse parameters was attempted to no avail. Next, manual adjustment of the bias voltage was attempted to fine tune the current source (which also required application of the 3.3 V from an external source rather than POR. Still, no data could be recovered. One possible cause was that the CLK line was not sufficiently delayed.

Recall in Section 3.5.2 the description of a starved inverter delay unit to ensure latching occurs prior to the reset of VB voltage. This was measured by comparing the Pulse Generated from the microcontroller and the gated CLK output from the SOF detection. Shown in Figure 4-18, a 1us delay consistent with simulation and more than sufficient to ensure the comparator checks prior to reset.

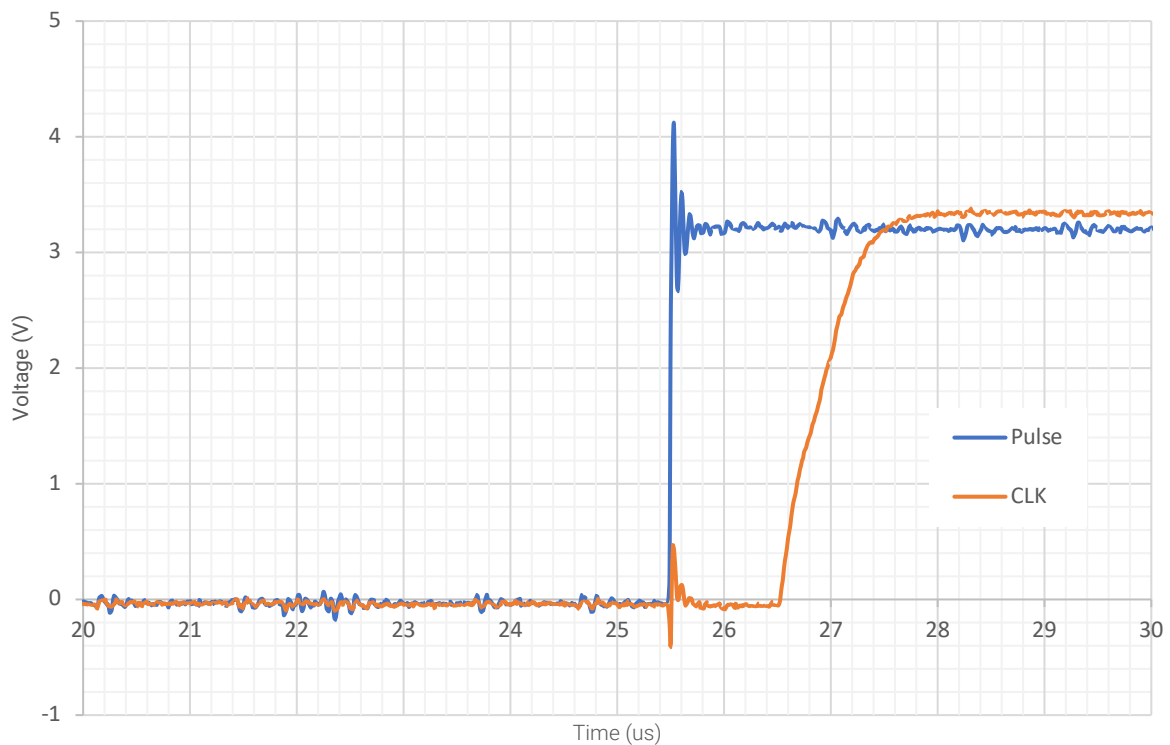


Figure 4-18 Current started inverter successfully delaying signal by 1us.

Unfortunately, a clear answer to why the data decoder was not operating as expected could not be determined and, without test pads inside the chip, could not be solved.

4.6.3 Pin Casting

Of all modules, the Pin Casting was the most nested and challenging to simulate and design. What proved most difficult was understanding the start-up state and modelling the biphasic current generator accurately with respect to the substrate and ground connections of the input devices. To perform this testing a biphasic current source designed by the author (as part of the Australian Bionic Eye Project) was utilised [107].

4.6.3.1 Test 6: Rectification

The first evaluation of the Pin Casting circuit was the rectification of input biphasic current pulses. The experimental setup is shown in Figure 4-19. The stimulator was configured to deliver 100uA pulses with a PW and IPG of 500us and a stimulation rate of 250 pulses per second (pps), which is equivalent to an ISI of 2ms.

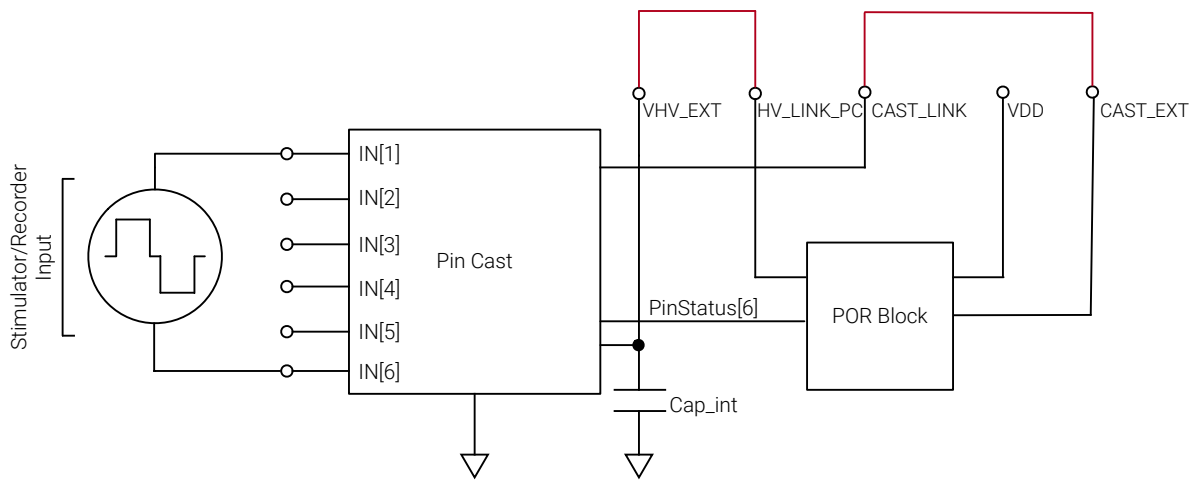


Figure 4-19 Experimental setup to test rectification within XPAND.

Figure 4-20 shows VHV_EXT climb close to the compliance voltage of the stimulator, which is approximately 10V. As expected, XPAND will charge to the stimulator compliance voltage minus the threshold of the MOS diodes. Substantial noise can be seen on the VDD lines, which in the measurements below are not decoupled with an additional external capacitor.

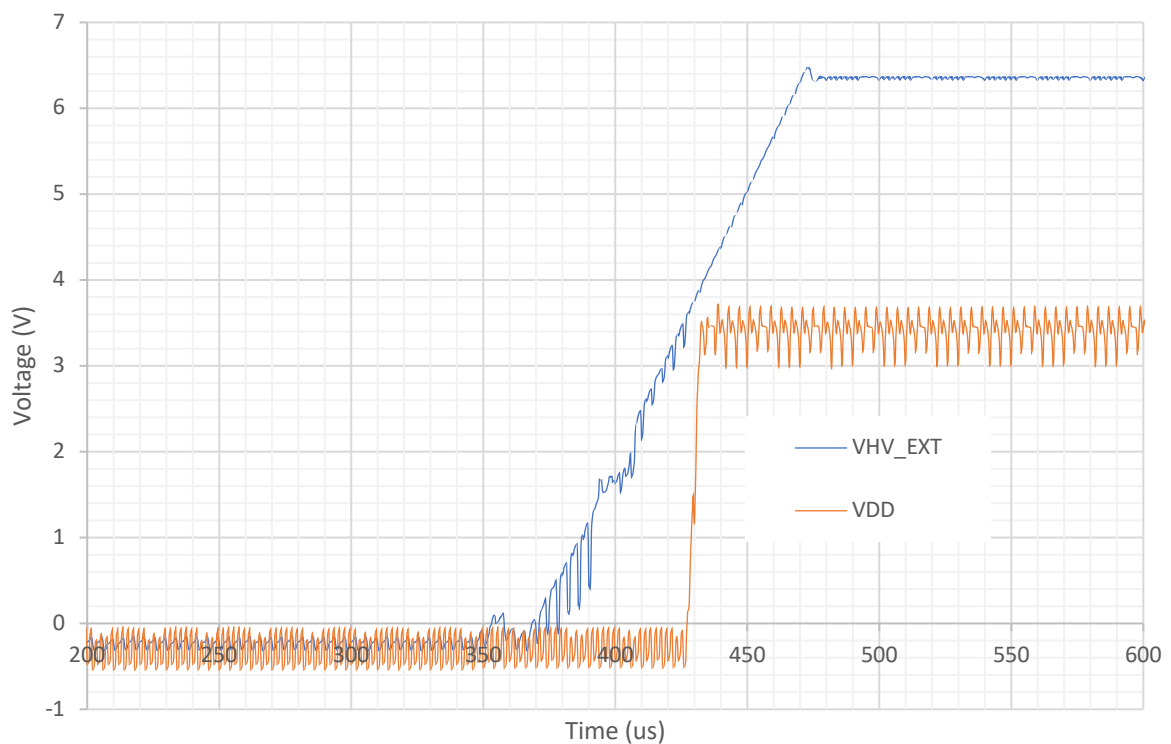


Figure 4-20 Rectification and switch on of 3.3V regulator.

4.6.3.2 Test 7: Rectification Leakage

To further understand the leakage of the rectifier, a digital pulse train with a pulse width of 20us applied every 200us via a 50k resistor. The equivalent circuit is shown in Figure 4-21.

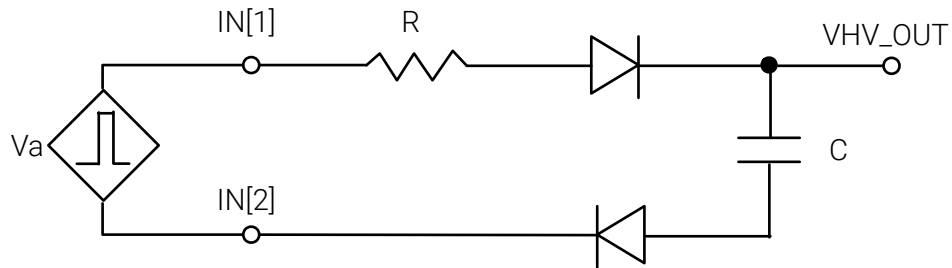


Figure 4-21 Rectification of a 5V square wave.

In this model, the charge delivered in each pulse (when it is starting), will be approximately

$$Q_{\text{injected}} = \frac{V_a}{R} \times PW. \quad (4-1)$$

For $R=51k$, Pulse Width = 20us and $V_a = 3.3V$, this is approximately 1.29nC.

Now, the internal capacitor was measured to be 1.7nF and the oscilloscope measurement probes have an input capacitance of 24pF (marginal increase in the overall capacitance). Based on this, we would expect to see in an ideal case a voltage increase of $Q = CV$. For $Q = 1.29nC$ and $C = 1.7nF$, the increase in voltage should be 700mV.

What was measured and is shown in Figure 4-22 is approximately 180mV. This highlights an inefficiency in charge injection.

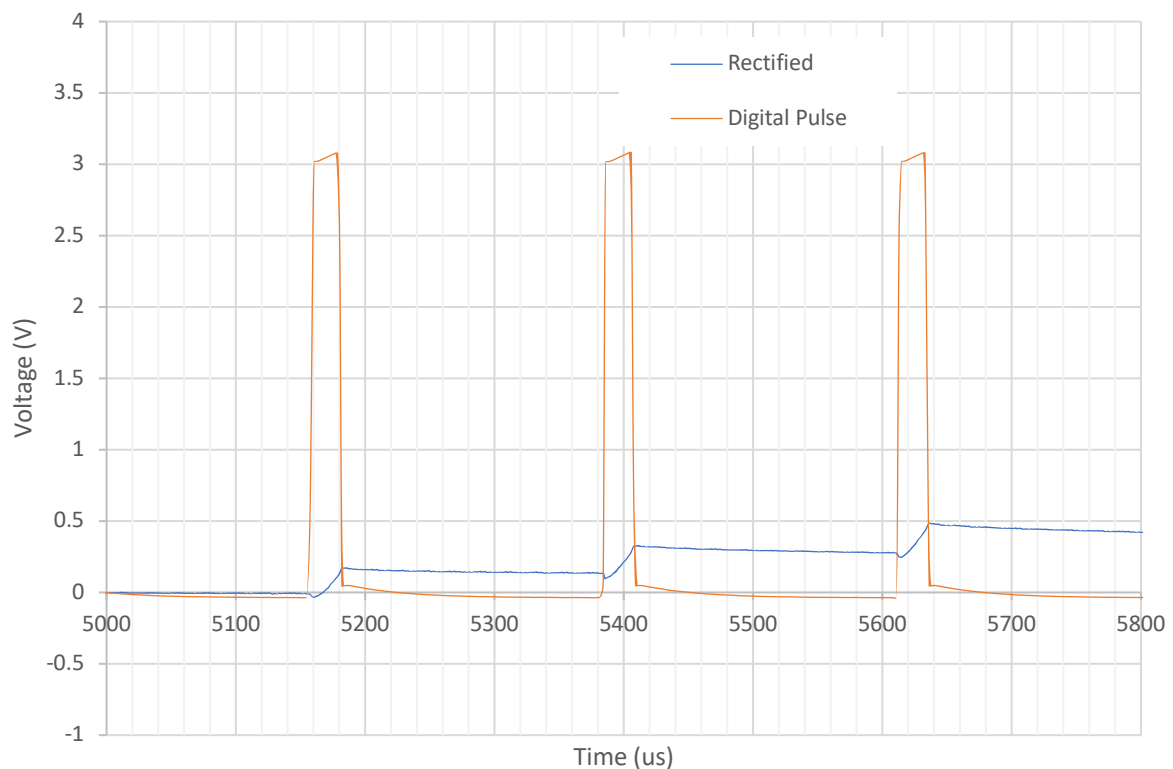


Figure 4-22 Rectification of single pulses with 51k limiting resistor.

While the inefficiency of the rectifier is not ideal, it is also not a major issue for the operation of XPAND so long as the leakage is low. As shown in Figure 4-22 the leakage resulted in a drop of approximately 30mV over a period of 200us. For a 1.7nF capacitor, this is approximately equal to a leakage current of around 255nA.

4.6.4 Switch Array

The switch array is responsible for routing any six of the input lines to any of the 64 output lines. In total, 6 x 64 (384) switches are needed to achieve this and hence a corresponding number of bits must be loaded to configure the state of each of the switches in the array. This is achieved using a shift register with loading buffer that required 768 D-Latches in total. The circuit being testing in this section is shown in Figure 4-23.

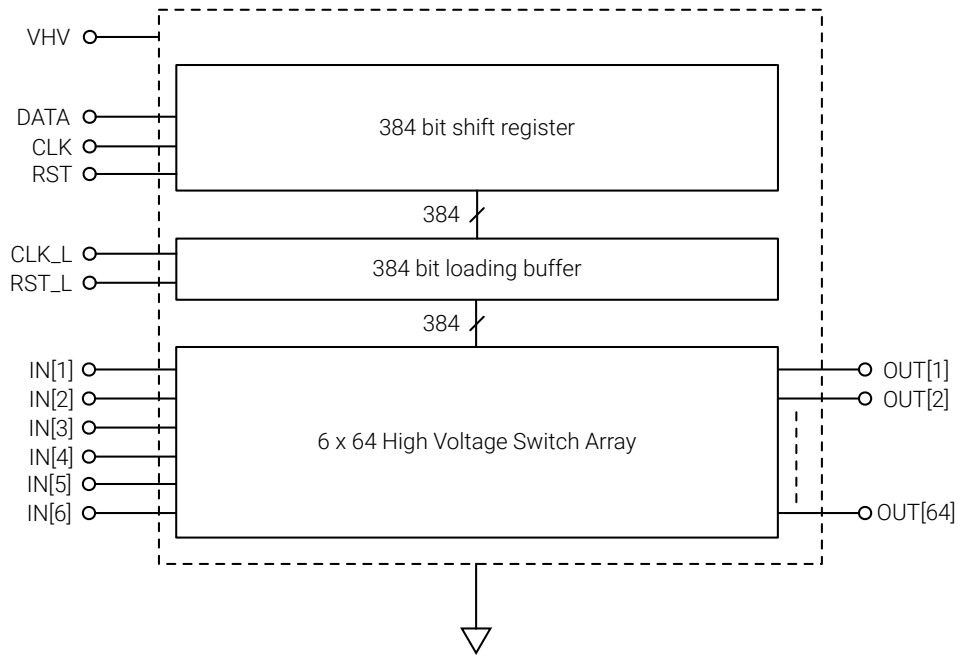


Figure 4-23 Switch array module in XPAND with respect to external pins.

To evaluate performance, the switch array was powered using a high voltage supply 10V, whilst a general-purpose microcontroller (Arduino Duo) was used to generate the control signals used to program the array.

The array register is arranged as shown in Figure 4-24, which shows the last bits of the register.

O[2]						O[1]					
I[1]	I[2]	I[3]	I[4]	I[5]	I[6]	I[1]	I[2]	I[3]	I[4]	I[5]	I[6]
373	374	375	376	377	378	379	380	381	382	383	384

Figure 4-24 Last bits of the 384 bit shift register.

The order in which the bits are serialised and clocked is in the reverse of the natural configuration. However, the first bits that enter the register are actually, from a programming sense, the first of the array programmed.

In this section, basic functionality was first established by gating a test signal through the switch. The switch characteristics were then measured. Finally, biphasic stimulation pulses and ECG signals were gated.

4.6.4.1 Test 8: Switch Array Basic Functionality

The first test involved switching a single cell on and off (gating) with a signal generator connected as shown in Figure 4-25. The signal generator is set to deliver a sine wave at 3V bias with an amplitude of 1V and frequency of 1kHz. This was simply a test tone to check the switch array addressing and basic operation of the test cell.

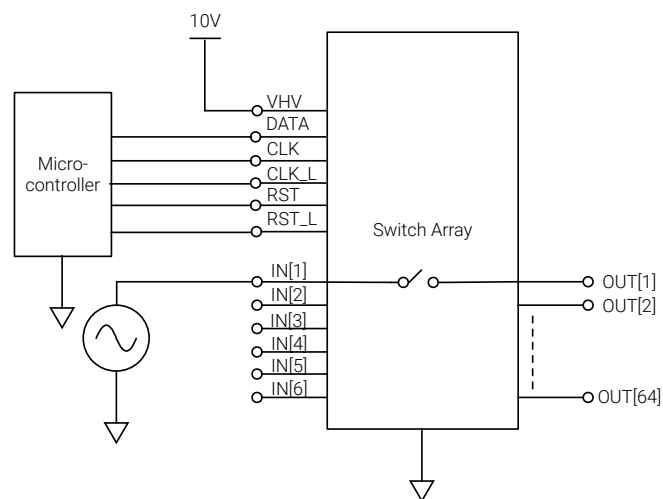


Figure 4-25 Sine wave being gated by single switch on XPAND.

For reference, the switch cell is shown in Figure 4-26.

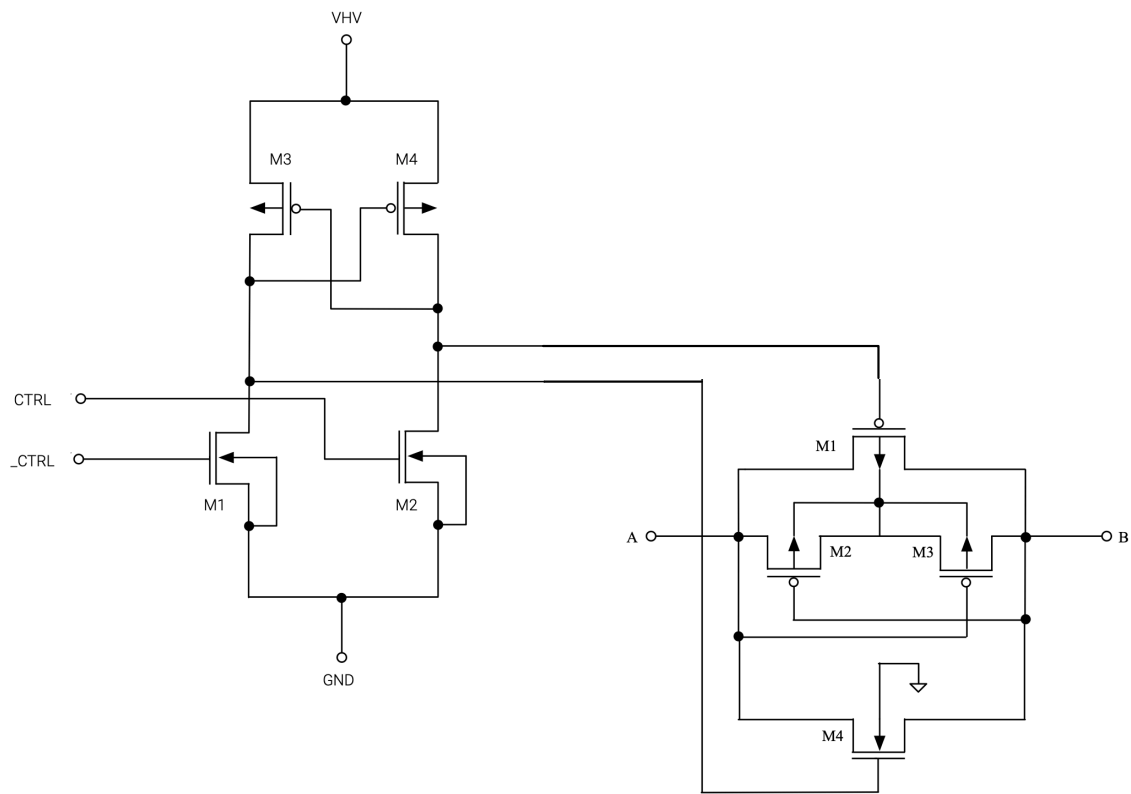


Figure 4-26 The complete transistor level schematic of the switch cell.

A single switch cell state ($I[1],O[1]$) was toggled by clocking in a 1 and loading to turn on, then clocking in a 0 to turn off. This is shown in Figure 4-27 where a single data bit is corresponding to the cell is clocked in and then loaded to turn the cell on.

Figure 4-28 shows a close-up image of the 1kHz signal being switched off. This successfully demonstrated basic operation of the switch array.

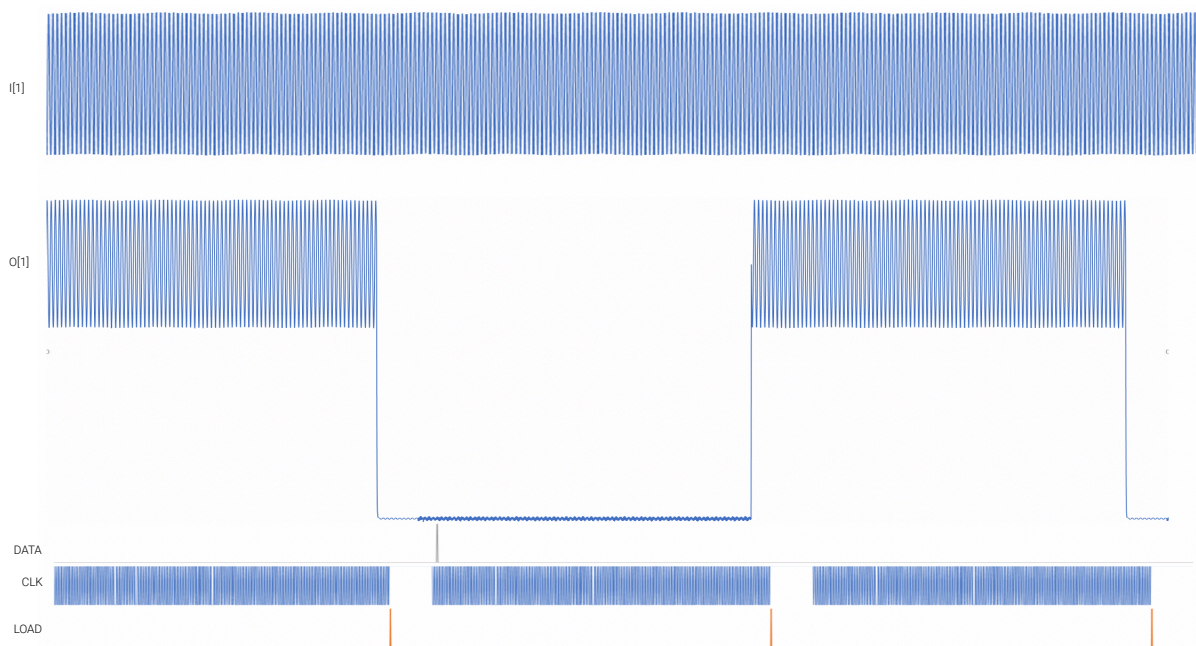


Figure 4-27 Single switch gating 1V sine wave (biased at 3V) on and off by loading 384 bit commands.

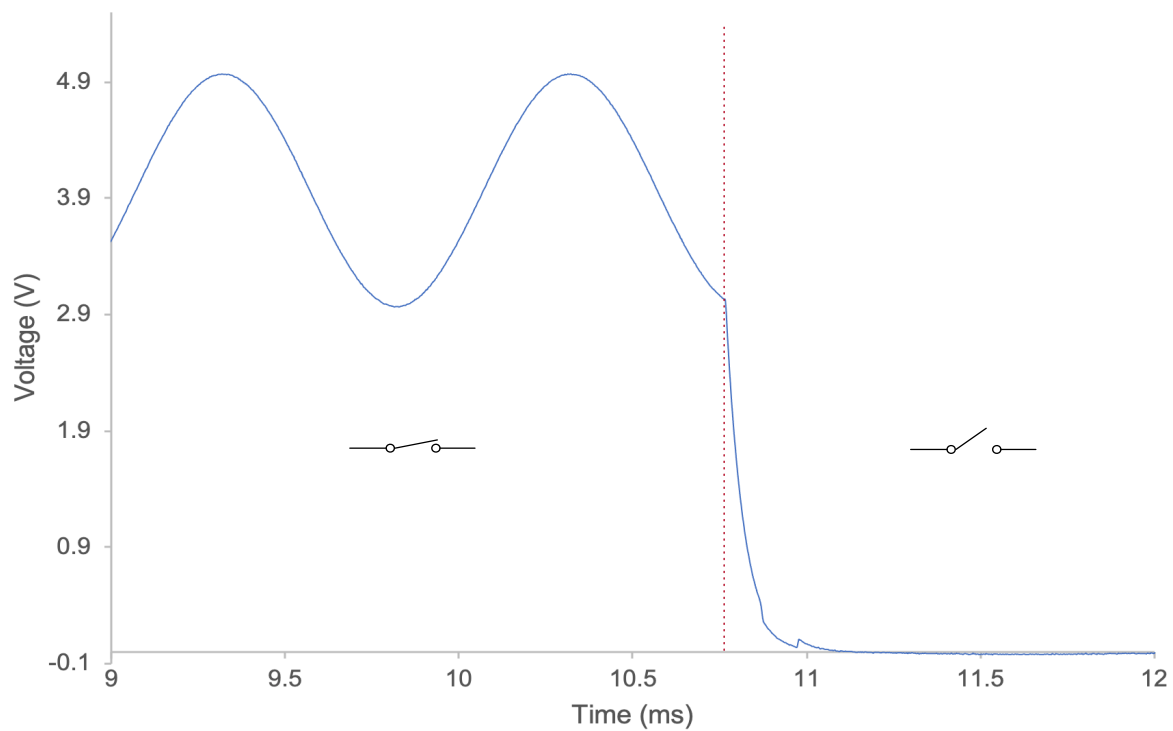


Figure 4-28 Gating 1kHz 1V sinewave biased at 3V.

4.6.4.2 Test 9: Switch Cell On Resistance

To test the on resistance of the switches for different signal levels, two switches within the array were turned on, and with a power supply on one side controlling the “signal level”, a multimeter was used to measure the impedance. The experimental setup is shown in Figure 4-29 and Figure 4-30. It was important to verify that the impedance was approximately equal measured from both sides.

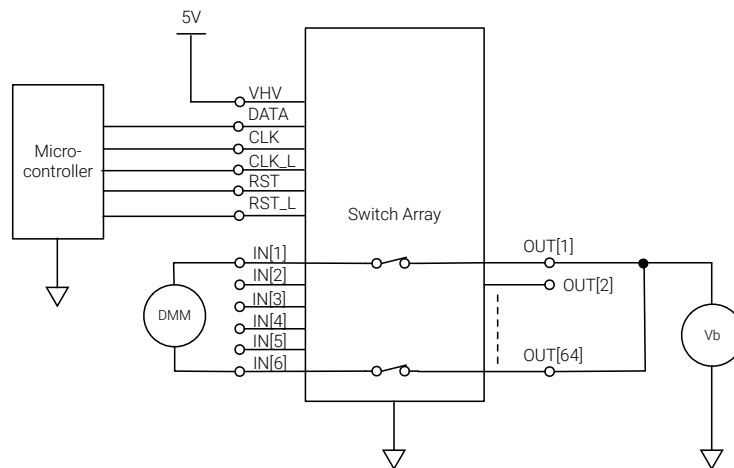


Figure 4-29 Experimental setup to measure on resistance of switches with bias applied to output.

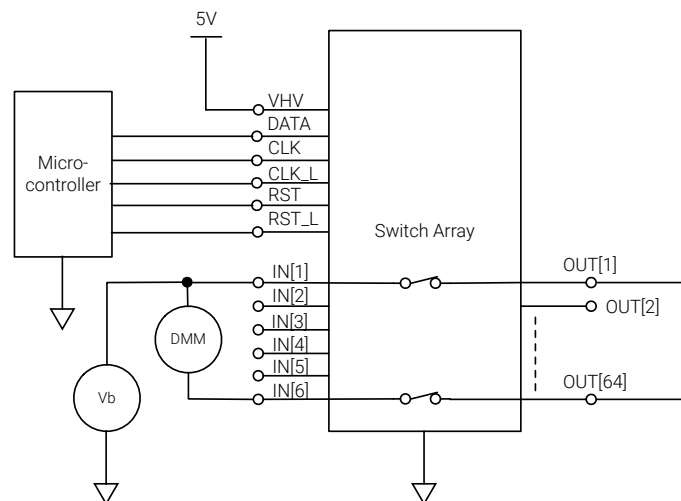


Figure 4-30 Experimental setup to measure on resistance of switches with bias applied to input.

The resistance of the switch was measured for signal voltages of 0 to 10V. Figure 4-31 shows the resistances measured in both configurations.

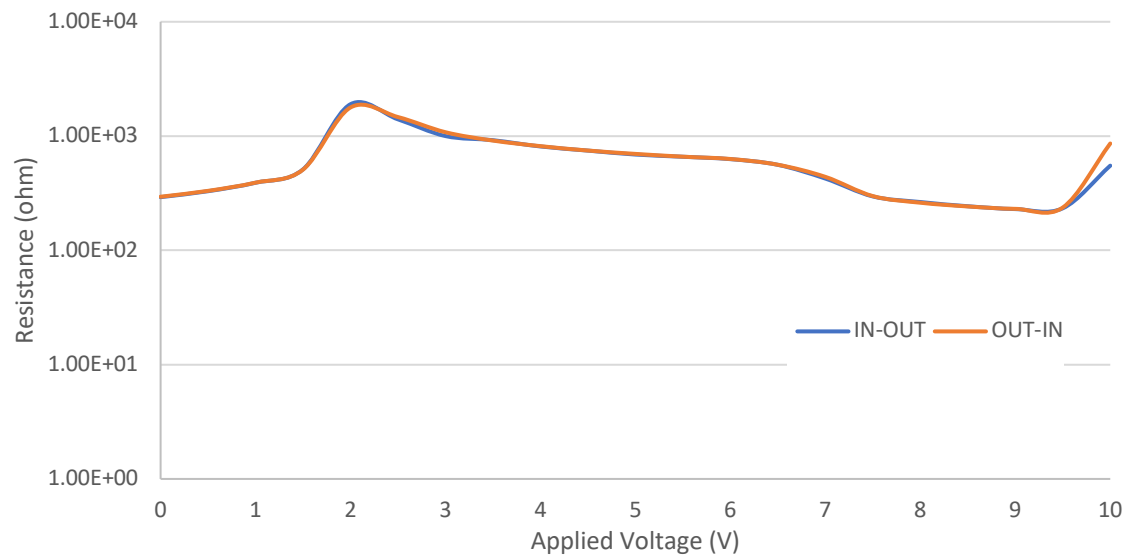


Figure 4-31 On resistance with 0-10V applied to both IN and OUT.

These results were contrasted to simulated values and showed good correspondence as shown in Figure 4-32.

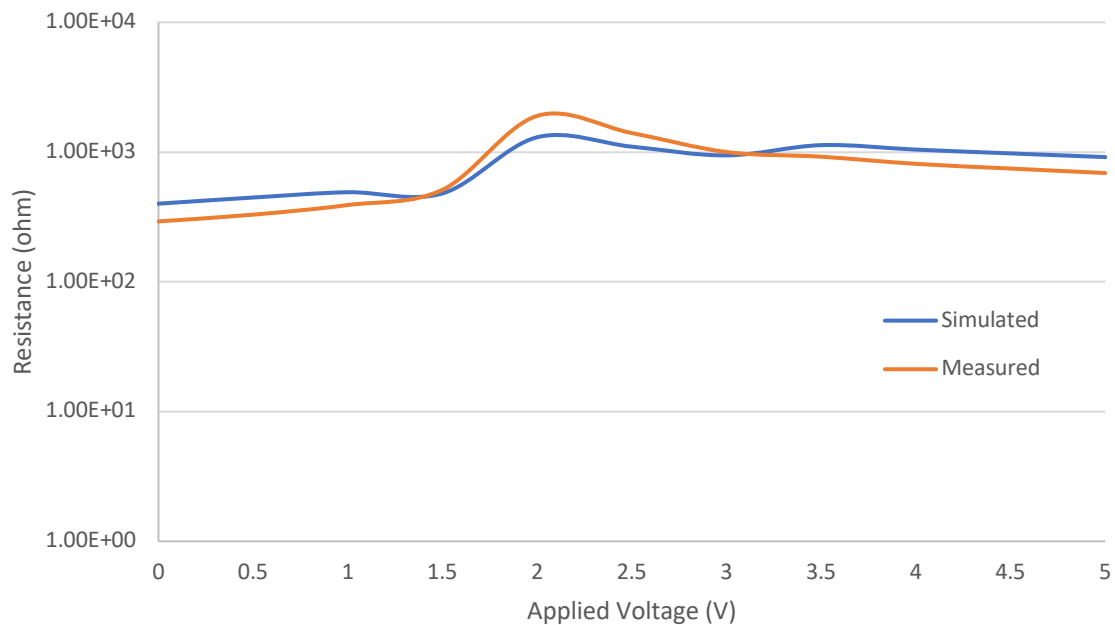


Figure 4-32 Comparison of on resistance for simulated and measured resistances.

4.6.4.3 Test 10: Simultaneous Recording and Stimulation Through XPAND

The final test conducted for XPAND involved simultaneously stimulating and recording through the XPAND switch array. Due to issues of demodulation reported previously, XPAND power and communication were delivered through a lab power and microcontroller.

The experimental setup is shown in Figure 4-33 and included:

- A commercial wireless brain and heart monitoring system (Seer Sense, Seer Medical, Melbourne, Australia)
- A research grade stimulation system (neuroBi, Bionics Institute, Melbourne, Australia)
- Custom software to coordinate configuration of XPAND and stimulation signals.

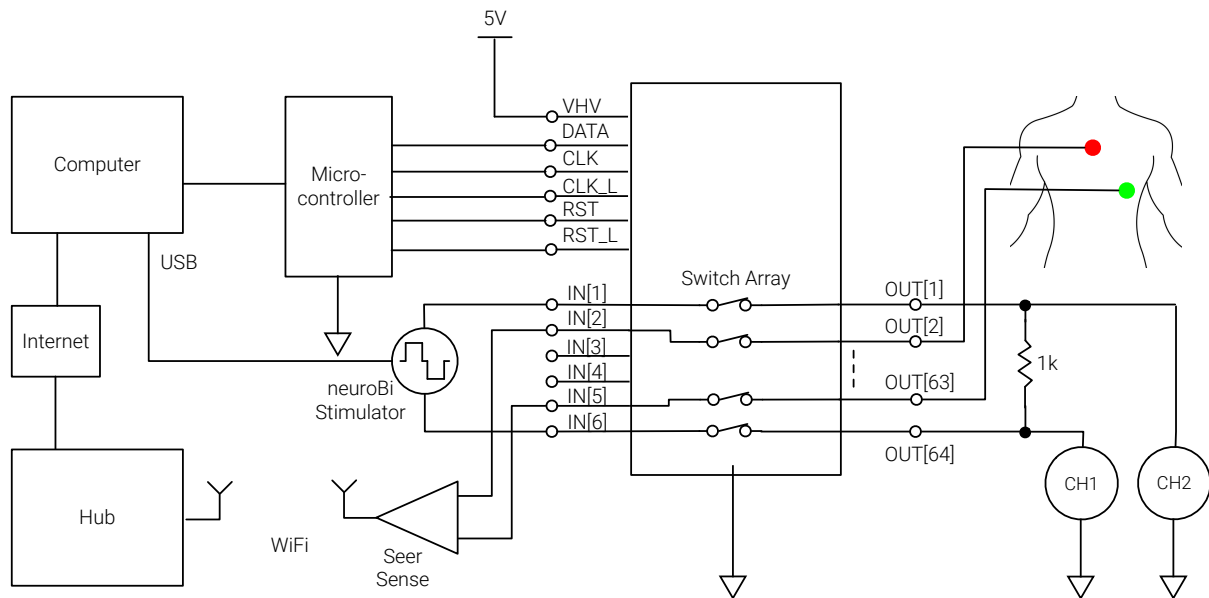


Figure 4-33 Complete experimental setup for simultaneous ECG and biphasic current stimulation.

(IN[1],OUT[1]), (IN[2], OUT[2]), (IN[5],OUT[63]), (IN[6], OUT[64]) were toggled on and off every 40ms. Both biphasic stimulation pulses and ECG signals were simultaneously toggled through XPAND. Results were very pleasing and show good transmission through the switches. Additionally, when the switches are turned off, the isolation was very good with no observable leakage in this state.

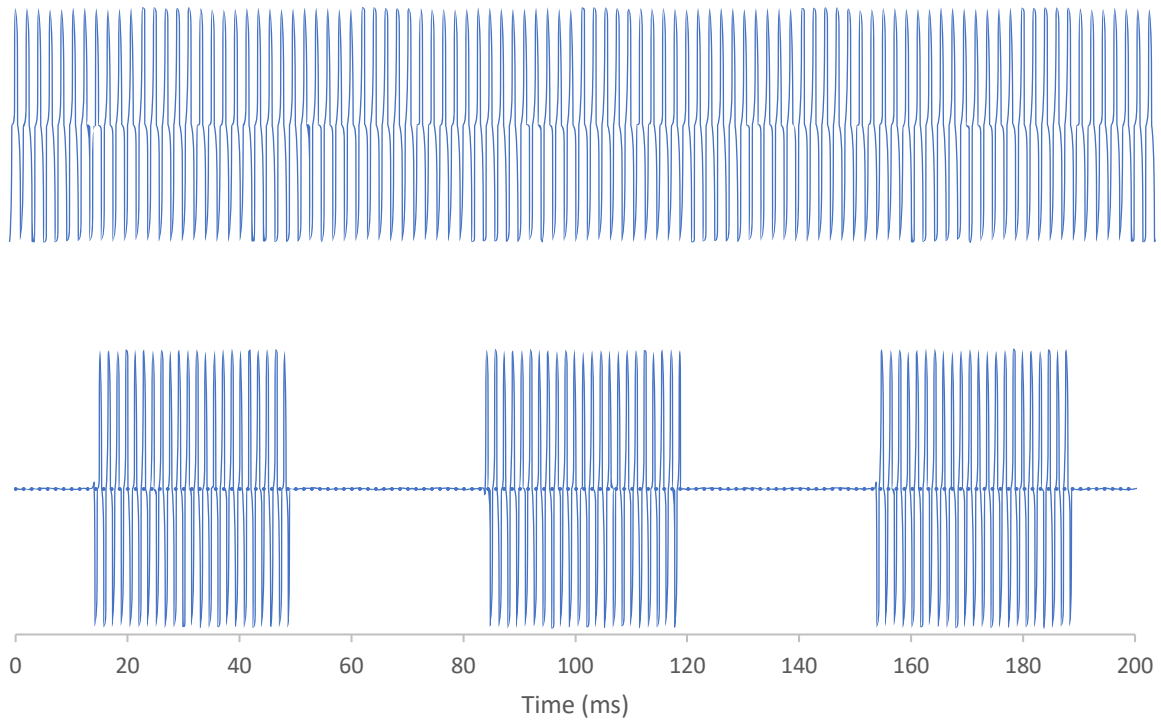


Figure 4-34 Gated biphasic current pulses.



Figure 4-35 Gated ECG signals.



Figure 4-36 Photograph of the simultaneous recording and stimulation experiment.

5 Conclusions and future work

This thesis began with an exploration of the status quo in epilepsy diagnostics, treatment and management, which highlighted the need for novel therapies beyond pharmaceuticals and surgical intervention. One of the most promising approaches to emerge is the use of electrical stimulation applied to deep brain structures, seizure foci and the peripheral nervous system to modulate neural activity and abate seizures.

While several implantable devices have now reached market, they are limited in electrode count, functionality and flexibility. This presents a challenge in addressing a condition with heterogenous aetiology where optimal stimulation target and pulse parameters will change from patient to patient. It was this realisation that led to what became the core of this thesis: the design and development of a standalone integrated circuit to seamlessly expand the electrode count of existing commercial stimulators.

A novel architecture was proposed using a high voltage CMOS process, and the conceptual framework around how such a system would work was discussed in Chapters 2 and 3. The design of this architecture centres around the constraint of needing to derive all power and communication purely through biphasic stimulation pulses, and the additional requirement that any two input pins can be used for this purpose. A biphasic two-wire protocol and a pin casting topology was developed to address these constraints.

The requirements of the chip, named XPAND, were highly unusual and created substantial design challenges along the way requiring novel approaches at the system architecture, component and semiconductor device levels. This made almost every aspect of the development difficult, from architecture through to layout and finally testing. Key challenges include, but are not limited to:

- Difficulty defining and simulating start-up state for current driven circuits due to convergence issues
- Ultra-low quiescent current consumption requirement
- An undefined ground connection

- Above and below supply terminal voltages
- The need for no interference of stimulation and recording signals when not being used for power and communication
- The need for high voltage (>3.3V) stimulation signal transmission.
- Purely configured and controlled through asynchronous logic driven by the biphasic pulses.

Because of the challenges above, the circuit was highly nested in nature and it was very difficult to compartmentalise the design into discrete blocks.

After simulating XPAND, the layout and fabrication was completed, and XPAND was tested. All blocks except for the Data Demodulator were shown to work, and XPAND was able to simultaneously gate biphasic stimulation pulses and ECG recording through its internal switch array. It was unfortunate that test pins were not created for the Data Demodulator, however there was a limit in the available test pins, and it was assumed that if the data frame detection was functional so too would be the data demodulator. Ideally a probing station would have been used (and probing pads included), but this equipment was not available.

XPAND could be improved and simplified in many ways. The flexibility and redundancy goals were so large that highly nested and complex solutions were required along with more exotic process technology. A commercial version of this chip would need to simplify this architecture to ensure more robust and reliable performance. A low voltage standard CMOS process could be considered if requirements were re-evaluated. This would have the benefit of reducing leakage and chip size substantially and the drawback of reducing the on-chip capacitance. That said, the regulator would no longer be needed leaving only the demodulation circuit with a non-zero quiescent consumption. Stimulation voltage requirements could be re-assessed for microarray applications where far less charge is delivered, otherwise more sophisticated floating gate circuits could be explored to pass stimulation signals beyond supply voltage.

Much has changed in the landscape of neurotechnology since the commencement of this research project. Most notably, companies like Neuralink have emerged with the aim to deliver clinically viable high-density interfaces for both stimulation and recording of the brain. Such

systems will likely still rely on a central implant for power and data. If many “threads” are scattered throughout the brain this presents the new challenge of how to route high density wire bundles to each.

One option to overcome this challenge would be to place an IC that includes stimulation and recording circuitry on the stem of electrode threads remote to the central implant unit. A two wire AC interface would be needed here, as DC supply lines would present an unacceptable risk. However, for clinical applications, there is a question as to whether it is about recording and stimulating all of the electrodes or whether it is about recording and stimulating the right electrodes at the right time.

A four-wire interface based instead on the biphasic protocol established in this thesis would offer a number of advantages. The two lines not used for power and communication can be routed in any way to either a recorder or a stimulator based inside the main unit where there is much more space to optimise performance and flexibility. The chip would also likely be a lot smaller and far less complex to design. Importantly, it would provide access to many electrodes through very few wires that use charged balanced signalling, and with the addition of a decoder to minimise configuration data time this could be done very quickly in comparison to the frequencies of the signals of interest. This is perhaps the most relevant and interesting application of XPAND as we enter an era of high-density electrode interfaces.

As more and more devices for the treatment of neurological conditions such as epilepsy begin to reach the market, technologies like XPAND offer value by bridging the gap of the unknown and undefined with flexibility rather than redesign. Sometimes flexibility in system design is considered lazy engineering where not enough research and effort to establish the requirements has been made. This is not the case for brain interfaces, where a different set of requirements exists for each individual. No two brains are the same and every brain evolves over time. Perhaps the future neural interfaces will exhibit the same type of plasticity and learn how to be useful - just as the brain does.

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