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Negative Capacitance in Hydrogen-Terminated Diamond Devices

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Surfaces and interfaces can dominate charge carrier transport dynamics in electronic devices, impeding realisation of a material's full potential. Here, we investigate transport in a two-terminal diamond device comprising of a conductive channel defined by a hydrogen-terminated diamond surface, bridging two TiC contacts. Negative capacitance at low AC frequencies is observed and correlates well with the transient response to a voltage step. The magnitude of the negative capacitance was found to increase linearly with the TiC contact/H-terminated channel perimeter normalised to the channel length, indicating that negative capacitance is a result of the injected charge carrier trapping occurring at this interface. Finally, the surface charge distribution was imaged by monitoring the photoluminescence of the nitrogen vacancy centers incorporated below the active device layer. A strong charge accumulation near the TiC contact/H-terminated channel interface is observed and could be correlated directly with the non-Ohmic behaviour observed from DC electrical measurements.

I. INTRODUCTION

Negative capacitance is an unconventional carrier transport-related phenomenon that has been previously observed in organic light emitting diodes [1–3], perovskite solar cell diodes [4], forward biased diodes [5–7], and quantum wells [8, 9]. Recently, there is significant interest in utilizing negative capacitance to fabricate low-power fast switching field effect transistors (FETs) with sub-60 mV/decade subthreshold voltage swing [10, 11]. A negative contribution to the measured capacitance can arise when the time-derivative of the relaxation current in response to a voltage step is non-monotonic or positive-valued (i.e., $\frac{d\delta I(t)}{dt} > 0$). This response may involve charge carrier recombination or charge trapping at interfaces and/or junctions. The theoretical framework developed by Ershov *et al.*, links the current transient response to the frequency domain via a Fourier transform [13]. For example, an arbitrary relaxation current transient response may be modelled by a sum of exponential decays:

$$I(t) = \sum_{i=1} I_{0,i} \exp(-t/\tau_i), \tag{1}$$

where $I_{0,i}$ is the saturation current and τ_i is the time constant. A real device may be characterised by more than one exponential decay depending on the types of traps and interfaces present. The corresponding frequency-dependent capacitance is then:

$$C(\omega) = C_0 + \sum_{i=1} \frac{\alpha_i \tau_i}{1 + \omega^2 \tau_i^2}, \tag{2}$$

where C_0 is the geometrical capacitance, α_i is a proportionality factor that scales with $I_{0,i}$, and ω is the angular frequency of the AC test signal. The value of α_i can be negative and may lead to a negative capacitance if the associated relaxation capacitance is greater than the geometric capacitance.

In this work, we observe negative capacitance in hydrogen terminated diamond devices. With innovations in crystal growth and fabrication protocols, diamond has become a promising material for high power electronics as it offers high breakdown voltage, high thermal conductivity, and improved reliability [14]. In addition, the two-dimensional p-type conductive channel formed by H-termination offers a unique platform for fabricating FETs for high frequency applications [15]. However, the surface conductivity of the H-terminated channel is found to be highly dependent on the surface quality [16], suggesting that recombination and trapping at interfaces and junctions may play a critical role. In order to successfully leverage diamond's outstanding properties, we study charge carrier transport dynamics and find that the properties of diamond devices exhibiting negative capacitance can be tuned by varying the device geometry.

Here, we fabricate two-terminal devices connected by a conductive H-terminated channel, and investigate charge carrier dynamics and recombination kinetics through a combination of electrical and optical techniques. The magnitude of the negative capacitance is found to be linearly dependent on the perimeter of the TiC contact/H-terminated channel interface, normalised with respect to the channel length, indicating that the origin of the negative capacitance is due to charge injection and capturing from interface states at this junction. We also exploit the optical response of the nitrogen vacancy (NV) centers incorporated into the diamond below the active device region to report on near-surface changes in band bending during normal device operation [19–21]. NV imaging

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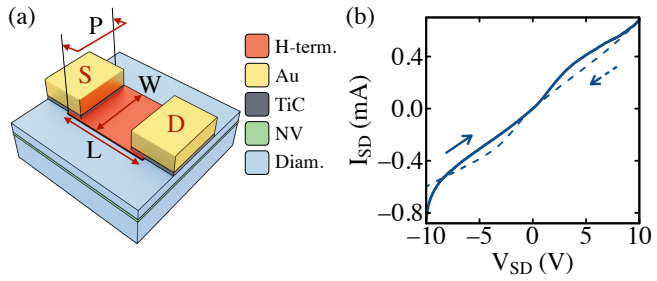

FIG. 1. (a) Illustration of a two-terminal H-terminated diamond device exhibiting negative capacitance studied in this work. (b) I−V characteristics of a typical device (device #1) measured in the dark. Arrows indicate voltage sweep direction.

confirms that junctions are formed at these interfaces. These insights can be leveraged to further optimise diamond based electronic devices.

II. EXPERIMENTAL DETAILS

A set of two-terminal H-terminated devices with different device geometries (see [22] for photograph of the fabricated devices) were investigated using the same fabrication process detailed in previous work [20]. Briefly, Ti/Pt/Au contacts were defined by photo-lithography and e-beam evaporation. A 600°C anneal was utilized to form a conductive TiC layer that is expected to extend approximately 15 nm into the diamond [20]. This conductive graphitic layer pins the Fermi level at the diamond/metal interface and reduces the barrier height to approximately 0.39 − 0.55 eV [23–25]. As a result, a good Ohmic contact is expected to form [17, 18].

These contacts were then connected via a H-terminated conductive surface channel in an otherwise O-terminated diamond. The lower electron affinity of the H-terminated channel leads to efficient charge transfer from the diamond to acceptor species absorbed on the surface, resulting in hole conduction through the channel on the application of a potential difference [26]. Devices with a variety of channel widths, W, and channel lengths, L, were fabricated and measured. The device geometry is indicated in Fig. 1(a) and the list of parameters are presented in Table I.

The electrical properties of the H-terminated devices in the dark were characterised by DC I−V measurements (Keithley 487), followed by AC impedance measurements utilising a LCR meter (HP 4284A) with an AC bias amplitude of 100 mV_{RMS}. Open and short calibrations were performed prior to device measurements to correct for the effects of stray external measurement circuit impedances. Current transients were recorded using a 16 bit analog-to-digital (A/D) converter from the output of a Femto DLPCA-200 low noise current amplifier in response to a square pulse supplied by an Agilent 33210A arbitrary waveform generator.

Prior to device fabrication, a layer of near-surface NV centers was formed by N implantation (10 keV, 10^{13} cm^{-2}) followed by high temperature annealing in vacuum and acid cleaning [27]. This resulted in a mean NV layer depth of approximately 17.5 nm below the surface [20]. A 532 nm laser excited NV photoluminescence (PL) was spectrally filtered and collected on a CCD camera. Recombination kinetics at the NV are extremely sensitive to band bending [20, 21]. In our devices, the NV PL intensity is proportional to the charge distribution at the diamond surface. Details on the imaging set-up are provided in Ref. [20]. Although a photocurrent was generated during optical measurements, the major features of the electrical characteristics were not modified as confirmed by in-situ impedance measurements (as was shown in [22]). Likewise, the presence of the NV centers and the accompanying implantation damage did not affect the electrical characteristics of the devices as confirmed with unimplanted devices in [22].

III. RESULTS

The I−V characteristics of device #1 is shown in Fig. 1(b) exhibiting slight non-linearity. Hysteretic behaviour is also observed when the bias is swept in the opposite direction. A similar non-linear and hysteretic behaviour was observed in all devices, suggesting that charge traps and the presence of junctions play a significant role in their operation. We note that long-term current drifts due to charge trapping is also observed. In the following, we seek to gain further insights into these effects by performing AC electrical measurements and correlating the results with the device's geometric parameters, as well as NV PL wide-field imaging to spatially resolve the band bending.

A. Negative capacitance

Figure 2 (a)−(d) presents the C−V characteristics of device #1 for various AC probe frequencies. Most notably, at low frequencies, the capacitance is negative and displays a near-symmetrical peak centred around zero.

Device	W (µm)	L (µm)	P (µm)	W×L (µm^2)	P/L
#1	100	10	144	1000	34.4
#2	15	20	30	300	1.5
#3	55	200	200	11000	1.0
#4	55	40	220	2200	5.5
#5	55	20	180	1100	9.0

TABLE I. Summary of the fabricated device geometries investigated in this work. The width, W, and length, L, of the H-terminated channel and the perimeter, P, of the TiC contact/H-terminated channel interface are considered (see definitions in Fig. 1(a)).

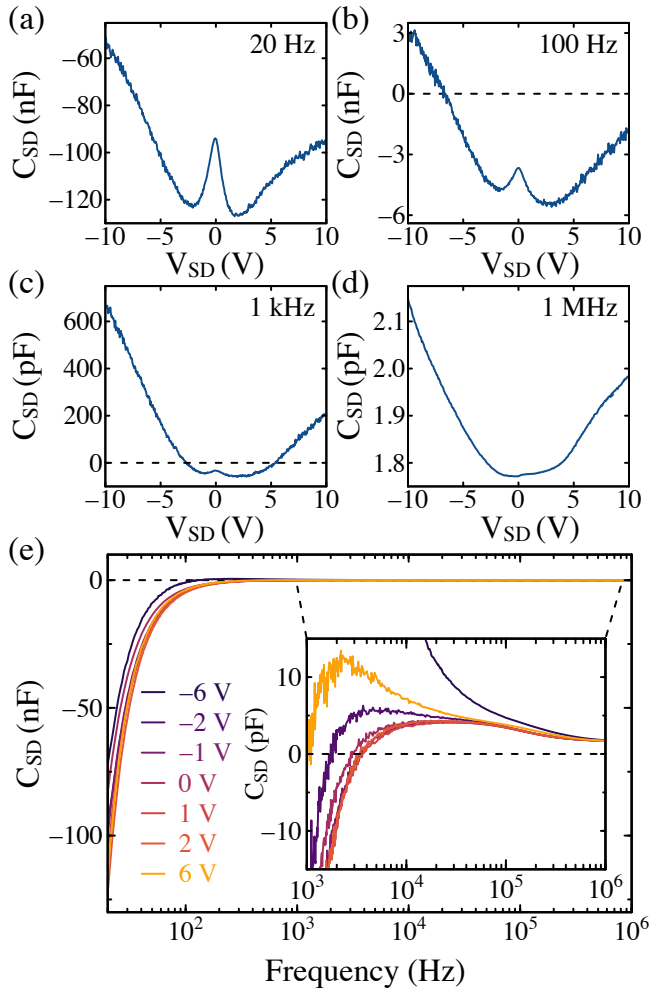

FIG. 2. C−V characteristics of device #1 at f = (a) 20 Hz, (b) 100 Hz, (c) 1 kHz, and (d) 1 MHz. (e) C−f characteristics at various biases. The inset highlights the transition from negative to positive capacitance occurring in the kilohertz regime. In addition, the capacitance returns back to its geometrical capacitance value as the measurement frequency is increased regardless of applied voltage.

Despite the expectation of Ohmic contacts, this observed behaviour is more characteristic of back-to-back rectifying barriers in which the C−V characteristics of the reversed biased junction (i.e., C $\propto$ $V^{-1/2}$) dominates over the forward biased junction for one polarity of the voltage applied [29]. Thus, the asymmetry observed in the C−V characteristics, especially under large biases, can qualitatively describe the extent of asymmetry of the metal contacts [28]. As with the I−V curve (Fig. 1(a)), a slight hysteresis is observed in the C−V traces (omitted for clarity). As the test AC frequency or applied bias increases, the capacitance value slowly crosses back to positive values. At high AC frequencies, the capacitance becomes less sensitive to the applied bias. This also corresponds to a decrease in the amplitude of the central C−V peak until it completely disappears at 1 MHz.

The C−f characteristics at various applied biases is presented in Fig. 2(e). We note that this measurement was performed separately to those in Fig. 2(a)−(d), resulting in slightly different measured values owing to long term drifts. The inset in Fig. 2(e) highlights the high frequency region where the capacitance value changes sign. This occurs in the kilohertz regime and depends on the applied bias. At high frequencies, the capacitance saturates to its geometric capacitance, C_0 [13], but is attenuated by series resistance at higher AC frequencies [3, 30].

In the ideal case where no charge traps are present, the measured capacitance should be independent of frequency [10]. Charge traps can contribute to the measured capacitance if the AC frequency is slower than its time constant. Since charge trapping dynamics plays a fundamental role in negative capacitance for these devices, time domain current transients were recorded in response to a voltage step. Fig. 3(a) shows the transient response to a 100 mV voltage step from V_{SD} = 0.9 V. An inverse Laplace transform algorithm [31] was used to extract the time constants of the transient (Eq. 1) and the reconstructed double-exponential current transient is shown in Fig. 3(a) (solid line). A minimum of two exponentials were required to adequately reconstruct the measured current transients. The time constant for the first exponential, τ_1, was found to be independent of the applied voltage and always ranged from approximately 0.20 − 0.25 s for all devices studied. In contrast, the

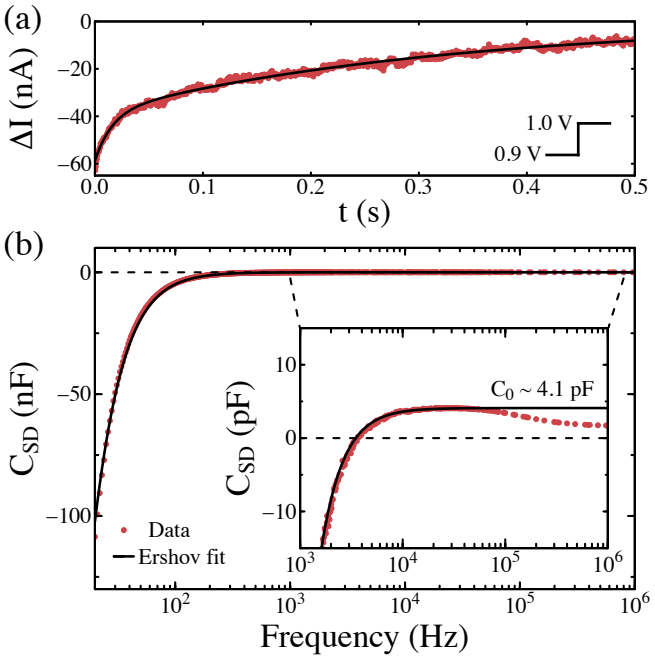

FIG. 3. (a) Current transient response resulting from a 100 mV voltage step from V_{SD} = 0.9 V and fit (solid line) to the experimental data using Eq. 1. (b) C−f curve reproduced from Fig. 2(e). The solid line is a reconstruction of the C−f response using the parameters extracted from Fig. 3(a) using Eq. 2.

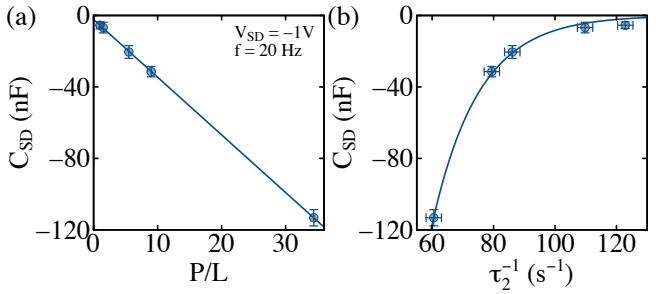

FIG. 4. (a) Negative capacitance measured at f = 20 Hz and V_{SD} = −1 V as a function of the contact perimeter normalised to the channel length, P/L. The solid line in (a) is a linear fit to the experimental data. (b) Measured negative capacitance as a function of the inverse second time constant, τ_2^{-1}, extracted from the current transients. The solid line is an exponential fit to the data.

time constant of the second exponential, τ_2, was found to vary with the applied voltage and varies significantly from device to device, which will be discussed further below. These time constants were then used to calculate the C−f curve via Eq. 2 and is plotted in Fig. 3(b) (solid line). This C−f curve agrees excellently with the measured C−f curve (shaded symbol), validating Eq. 1−2. The discrepancy at higher AC frequencies is a result of the series resistance, which is estimated to be around 8.8 kΩ at 1 MHz, giving a geometric capacitance of approximately 4.1 pF for device #1.

For voltages greater than approximately ±1.5 V, the current transients did not exhibit the characteristic positive-valued time-derivative responsible for negative capacitance even though a negative capacitance is observed in Fig. 2 at these voltages [22]. In this large voltage regime, Ershov's model breaks down, suggesting that the current transient may be dominated by some other mechanism and requires further investigation.

B. Device geometry dependence

To investigate the origin of the negative capacitance further, we compare its magnitude measured at 20 Hz between devices with different geometries. Fig. 4(a) shows the negative capacitance measured at V_{SD} = −1 V plotted as a function of the ratio between the contact perimeter normalised to the channel length, P/L (see Fig. 1(a)). A clear linear correlation between the negative capacitance magnitude and P/L is observed. Similar trends were observed up to 80 Hz. Beyond this frequency, where some capacitance values are positive, no such dependence was observed. In addition, the magnitude of the negative capacitance showed no dependence on the channel area, W×L (see supplementary material in [22]), suggesting that it is not affected by any charge trapping (from N implantation damage in this case) along the channel, but only at the contact/channel interface. This was further confirmed with measurements on devices without the NV layer [22].

In the time domain, the capacitance corresponding to the inverse of the second time constant for each device is shown in Fig. 4(b) measured at 20 Hz. A slower trapping time constant corresponds to a larger negative capacitance magnitude following an exponential dependence (solid line). As the measurement AC frequency is slower than τ_2^{-1}, the charge traps at the interface can follow the AC probe frequency and contribute to the measured capacitance response with a negative-valued contribution. In contrast, a positive-valued capacitance is expected to be observed for a fast trapping time constant as the charge traps can no longer participate and contribute to the measured capacitance.

C. Band bending mapping

Lastly, to better understand the operation of the device, recombination at the embedded NV layer was inferred from PL measurements under 532 nm laser illumination while the diamond device was biased. Fig. 5(a) and (b) show the normalised PL difference maps at V_{SD} = 10 V and −10 V, respectively. The maps are normalised and subtracted with respect to the PL obtained under zero bias (i.e., $\Delta PL = PL_V/PL_0 - 1$). A clear change in the PL intensity is observed. The NV center can exist in the NV^0 and NV^- charge state so the ratio between the NV^- and NV^0 population is a sensitive probe of the Fermi level position, which can be modulated by band bending with surface charges. Therefore, a negative ΔPL value corresponds to an increase in the band bending relative to its position at zero bias as the NV^0 becomes the dominate charge state [20, 21]. Likewise, a positive ΔPL value indicates a decrease in the band bending relative to its position at zero bias.

To analyse the relative changes in band bending near the contact/channel interface, a line cut (dotted line in Fig. 5(a)−(b)) of the PL map is plotted in Fig. 5(c) and (d) for V_{SD} = 10 V and V_{SD} = −10 V, respectively, along with additional line cuts taken at various biases. When a positive bias is applied across the contacts (Fig. 5(a)), the left contact junction is under reverse bias while the right contact junction is under forward bias. This is represented with a simplified energy band diagram in Fig. 5(e) for a metal-semiconductor-metal (MSM) junction in a back-to-back Schottky barrier configuration. Under reverse bias, the band bending increases relative to its zero bias position (i.e., Δ PL < 0), whereas the band bending decreases under forward bias (i.e., Δ PL > 0).

A change in the polarity of the applied bias between the contacts is clearly reflected in the change of sign in ΔPL. In addition, the forward biased contact displays a larger ΔPL magnitude than the reverse biased contact by about a factor of 2. Near the contact/channel interface indicated by the vertical grey dotted lines in Fig. 5(c) and

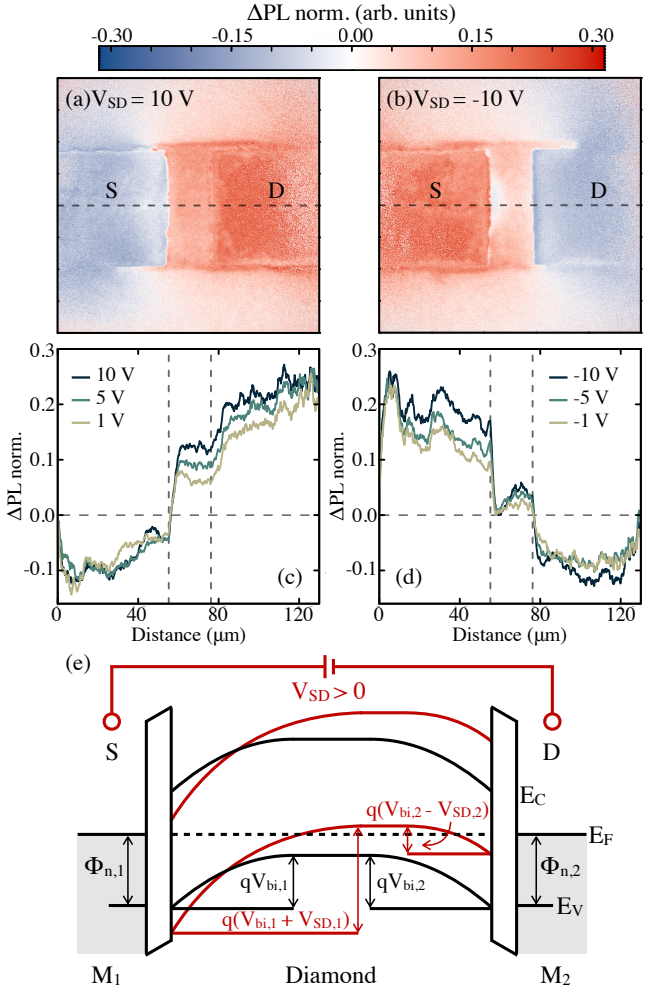

FIG. 5. Normalised PL difference ($\Delta PL = PL_V/PL_0 - 1$) for (a) $V_{SD} = 10$ V and (b) $V_{SD} = -10$ V. Profile of the normalised PL difference taken along the black dashed line in (a) and (b) for (c) positive voltages and (d) negative voltages. The grey vertical dotted lines indicate the H-terminated channel. (e) Schematic of the energy band diagram of a metal-semiconductor-metal structure in a back-to-back Schottky configuration, where $V_{bi,1}$ ($V_{bi,2}$) and $\Phi_{n,1}$ ($\Phi_{n,2}$) are the built-in potential and barrier height at the metal contact/H-terminated surface interface, respectively, and $V_{SD} = V_{SD,1} + V_{SD,2}$.

(d), a measurable decrease in PL by about 17% near the reverse biased contact for $V_{SD} = 10$ V was observed. A similar magnitude change is observed for $V_{SD} = -10$ V. In the conductive channel itself, a non-zero positive ΔPL is observed independent of the bias polarity, although its magnitude is significantly larger when a positive bias is applied. Such behaviour is not apparent in the electrical measurements, but may be a result of the band bending introduced by the H-terminated surface. Nonetheless, both electrical and optical measurements suggest the presence of junctions at the contact/channel interface with associated potential barriers that vary significantly under an applied bias and give rise to negative capacitance.

IV. CONCLUSION

In conclusion, we have observed negative capacitance in two-terminal H-terminated diamond devices, which can be explained adequately using Ershov's model and considering the device operates in a back-to-back Schottky barrier configuration. Physically, the origin of negative capacitance arises from the charge trapping of injected charge carriers at the TiC contact/H-terminated channel interface and is therefore strongly dependent on the contact/channel interface perimeter. Although further spectroscopic information is required to gain insight into the atomic nature of these defects, this work demonstrates that negative capacitance can be tailored to a specific application with appropriate changes to the device geometry. The NV layer incorporated for device characterisation together with impedance spectroscopy was shown to be a rapid and effective way to image the band bending near the contact interface of the device and evaluate the junction quality, which can be employed to optimise device function for the demands of future diamond devices.

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